查询AM26C31C供应商

 Meet or Exceed the Requirements of TIA/EIA-422-B and ITU Recommendation V.11

- Low Power, I_{CC} = 100 μA Typ
- Operate From a Single 5-V Supply
- High Speed, t_{PLH} = t_{PHL} = 7 ns Typ
- Low Pulse Distortion, t_{sk(p)} = 0.5 ns Typ
- High Output Impedance in Power-Off Conditions
- Improved Replacement for AM26LS31

description

The AM26C31C, AM26C31I, and AM26C31M are four complementary-output line drivers designed to meet the requirements of TIA/EIA-422-B and ITU (formerly CCITT). The 3-state outputs have high-current capability for driving balanced lines, such as twisted-pair or parallel-wire transmission lines, and they provide the high-impedance state in the power-off condition. The enable function is common to all four drivers and offers the choice of an active-high or active-low enable input. BiCMOS circuitry reduces power consumption without sacrificing speed.

The AM26C31C is characterized for operation from 0°C to 70°C, the AM26C31I is characterized for operation from -40°C to 85°C, and the AM26C31M is characterized for operation from -55°C to 125°C.

WW.DZSC.

捷多邦,专业AM26@31C,AM26C34時AM26C31M QUADRUPLE DIFFERENTIAL LINE DRIVERS

SLLS103G - DECEMBER 1990 - REVISED SEPTEMBER 1998

AM26C31C, AM26C31ID, DB [†] , OR N PACKAGE AM26C31MJ OR W PACKAGE (TOP VIEW)									
1A [1Y [1Z [2Z [2Y [2A [1 2 3 4 5 6 7	16 15 14 13 12 11	V _{CC} 4A 4Y 4Z G 3Z						
GND [8	9	3A						





SC CO FUNCTION TABLE (each driver)							
INPUT	ENA	BLES	OUTPUTS				
Α	G	G	Y	Z			
Н	Н	Х	Н	L			
L	Н	Х	L	Н			
Н	Х	L	Н	L			
L	Х	L	L	Н			
Х	L	н	Z	Z			

H = high level, L = low level, X = irrelevant, Z = high impedance (off)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



SLLS103G – DECEMBER 1990 – REVISED SEPTEMBER 1998

logic symbol[†]



logic diagram (positive logic) 4 G 12 G 2 1 1Y 1A 3 1Z 6 2Y 7 2A 5 2Z 10 3Y 9 3A 11 3Z 14 4Y 15 4A 13 4Z

[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

The terminal numbers shown are for the D, DB, J, N, and W packages.

schematics of inputs and outputs





SLLS103G - DECEMBER 1990 - REVISED SEPTEMBER 1998

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, Vcc (see Note 1)	
Input voltage range, V ₁	
Differential input voltage range, VID	
Output voltage range, Vo	
Input or output clamp current, IIK or IOK	±20 mA
Output current, I _O	±150 mA
V _{CC} current	
GND current	
Continuous total power dissipation	See Dissipation Rating Table
Storage temperature range, T _{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values, except differential output voltage (VOD), are with respect to the network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25^{\circ}C$ POWER RATING	DERATING FACTOR ABOVE T _A = 25°C	T _A = 70°C POWER RATING	T _A = 85°C POWER RATING	T _A = 125°C POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW	_
DB	781 mW	6.2 mW/°C	502 mW	409 mW	—
N	1150 mW	9.2 mW/°C	736 mW	598 mW	—
FK	1375 mW	11 mW/°C	—	—	275 mW
J	1375 mW	11 mW/°C	—	—	275 mW
W	1000 mW	8.0 mW/°C	—	—	200 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V _{CC}		4.5	5	5.5	V
Differential input voltage, VID			±7		V
High-level input voltage, VIH	igh-level input voltage, VIH 2			V	
Low-level input voltage, VIL				0.8	V
High-level output current, IOH				-20	mA
Low-level output current, IOL		20 m		mA	
	AM26C31C	0		70	
Operating free-air temperature, T _A	AM26C31I	-40		85	°C
	AM26C31M	-55		125	



SLLS103G - DECEMBER 1990 - REVISED SEPTEMBER 1998

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		AM26C31C AM26C31I			UNIT	
				MIN	TYP†	MAX		
VOH	High-level output voltage	$I_{O} = -20 \text{ mA}$		2.4	3.4		V	
V _{OL}	Low-level output voltage	l _O = 20 mA			0.2	0.4	V	
IVOD	Differential output voltage magnitude			2	3.1		V	
$\Delta V_{OD} $	Change in magnitude of differential output voltage‡	D: 100.0	See Figure 1			±0.4	V	
Voc	Common-mode output voltage	KL = 100.02,				3	V	
	Change in magnitude of common-mode output voltage‡					±0.4	V	
Ц	Input current	$V_{I} = V_{CC} \text{ or } GND$				±1	μA	
1.0.0	Driver output current with power off	$V_{CC} = 0,$	VO = 6 V			100		
'O(off)		$V_{CC} = 0,$	$V_{O} = -0.25 V$			-100	μΑ	
los	Driver output short-circuit current	AO = 0		-30		-150	mA	
1	Lisk impedance off state output ourrest	V _O = 2.5 V				20	μA	
IOZ	Hign-impedance off-state output current	Vo = 0.5 V				-20	μA	
		IO = 0,	$V_I = 0 V \text{ or } 5 V$			100	μA	
ICC	Quiescent supply current	IO = 0, See Note 2	V _I = 2.4 V or 0.5 V,		1.5	3	mA	
Ci	Input capacitance				6		pF	

[†] All typical values are at $V_{CC} = 5 \text{ V}$ and $T_A = 25^{\circ}\text{C}$.

[‡] Δ|V_{OD}| and Δ|V_{OC}| are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.

NOTE 2: This parameter is measured per input. All other inputs are at 0 or 5 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CO	TEST CONDITIONS		AM26C31C AM26C31I										
				MIN	түр†	MAX									
^t PLH	Propagation delay time, low- to high-level output			3	7	12	ns								
^t PHL	Propagation delay time, high- to low-level output	S1 is open, See Fig	S1 is open,	S1 is open,	S1 is open,	S1 is open,	S1 is open,	S1 is open,	S1 is open,	S1 is open,	See Figure 2	3	7	12	ns
^t sk(p)	Pulse skew time (tpLH - tpHL)				0.5	4	ns								
tr(OD), tf(OD)	Differential output rise and fall times	S1 is open,	See Figure 3		5	10	ns								
^t PZH	Output enable time to high level		1 is closed, See Figure 4		10	19	ns								
^t PZL	Output enable time to low level				10	19	ns								
^t PHZ	Output disable time from high level	STISCIOSED, SEE			7	16	ns								
^t PLZ	Output disable time from low level				7	16	ns								
C _{pd}	Power dissipation capacitance (each driver) (see Note 3)	S1 is open,	See Figure 2		170		pF								

[†] All typical values are at $V_{CC} = 5$ V and $T_A = 25^{\circ}C$.

NOTE 3: C_{pd} is used to estimate the switching losses according to $P_D = C_{pd} \times V_{CC}^2 \times f$, where f is the switching frequency.



SLLS103G - DECEMBER 1990 - REVISED SEPTEMBER 1998

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

DADAMETED		TEST CONDITIONS	A	LINUT		
	PARAMETER			TYP†	MAX	
∨он	High-level output voltage	I _O = -20 mA	2.2	3.4		V
VOL	Low-level output voltage	I _O = 20 mA		0.2	0.4	V
IVODI	Differential output voltage magnitude		2	3.1		V
$\Delta V_{OD} $	Change in magnitude of differential output voltage [‡]	R_L = 100 Ω, See Figure 1			±0.4	V
Voc	Common-mode output voltage				3	V
	Change in magnitude of common-mode output voltage [‡]				±0.4	V
Ц	Input current	$V_{I} = V_{CC}$ or GND			±1	μΑ
	Driver output current with newer off	$V_{CC} = 0, \qquad V_{O} = 6 V$			100	
O(off)	Driver output current with power on	$V_{CC} = 0, \qquad V_{O} = -0.25 V$			-100	μΑ
los	Driver output short-circuit current	$V_{O} = 0$			-170	mA
	High impodence off state output ourrest	$V_{O} = 2.5 V$			20	μΑ
'OZ	High-Impedance off-state output current	V _O = 0.5 V			-20	μA
	Quieseest supply surrent	$I_{O} = 0,$ $V_{I} = 0 V \text{ or } 5 V$			100	μA
	Quiescent supply current	$I_{O} = 0,$ $V_{I} = 2.4 \text{ V or } 0.5 \text{ V},$ See Note 2			3.2	mA
Ci	Input capacitance			6		pF

[†] All typical values are at $V_{CC} = 5$ V and $T_A = 25^{\circ}C$.

[‡] Δ|V_{OD}| and Δ|V_{OC}| are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level

NOTE 2: This parameter is measured per input. All other inputs are at 0 V or 5 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST	TEST CONDITIONS		AM26C31M		
		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
^t PLH	Propagation delay time, low- to high-level output				7	12	ns
^t PHL	Propagation delay time, high- to low-level output	S1 is open,	See Figure 2		6.5	12	ns
^t sk(p)	Pulse skew time (tpLH - tpHL)				0.5	4	ns
tr(OD), tf(OD)	Differential output rise and fall times	S1 is open,	See Figure 3		5	12	ns
^t PZH	Output enable time to high level				10	19	ns
tPZL	Output enable time to low level	S1 is closed, See Figure 4			10	19	ns
^t PHZ	Output disable time from high level				7	16	ns
t _{PLZ}	Output disable time from low level				7	16	ns
C _{pd}	Power dissipation capacitance (each driver) (see Note 3)	S1 is open,	See Figure 2		100		pF

[†] All typical values are at V_{CC} = 5 V and T_A = 25°C. NOTE 3: C_{pd} is used to estimate the switching losses according to P_D = C_{pd} × V_{CC}² × f, where f is the switching frequency.



SLLS103G - DECEMBER 1990 - REVISED SEPTEMBER 1998

PARAMETER MEASUREMENT INFORMATION







^tPLH

NOTES: A. C1, C2, and C3 include probe and jig capacitance. B. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, duty cycle \leq 50%, and t_f t_f \leq 6 ns.

tPHL-

Figure 2. Propagation Delay Time and Skew Waveforms and Test Circuit



SLLS103G - DECEMBER 1990 - REVISED SEPTEMBER 1998



PARAMETER MEASUREMENT INFORMATION

NOTES: A. C1, C2, and C3 include probe and jig capacitance.

B. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, duty cycle \leq 50%, and t_r, t_f \leq 6 ns.

Figure 3. Differential Output Rise and Fall Time Waveforms and Test Circuit



SLLS103G - DECEMBER 1990 - REVISED SEPTEMBER 1998



NOTES: A. C1, C2, and C3 includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, duty cycle \leq 50%, t_r < 6 ns, and t_f < 6 ns.
- C. Each enable is tested separately.

Figure 4. Output Enable and Disable Time Waveforms and Test Circuit



SLLS103G - DECEMBER 1990 - REVISED SEPTEMBER 1998



Figure 5



IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.

Copyright © 1998, Texas Instruments Incorporated