GaAs MMIC VSAT Power Amplifier 2.0W 14.0 - 14.5 GHz

Features

- High Linear Gain: 22 dB Typ.
- High Saturated Output Power: +33 dBm Typ.
- High Power Added Efficiency: 22% Typ.
- High P_{1dB}: 32 dBm Typ.
- 50Ω Input/Output Broadband Matched
- Integrated Output Power Detector
- High Performance Ceramic Bolt Down Package

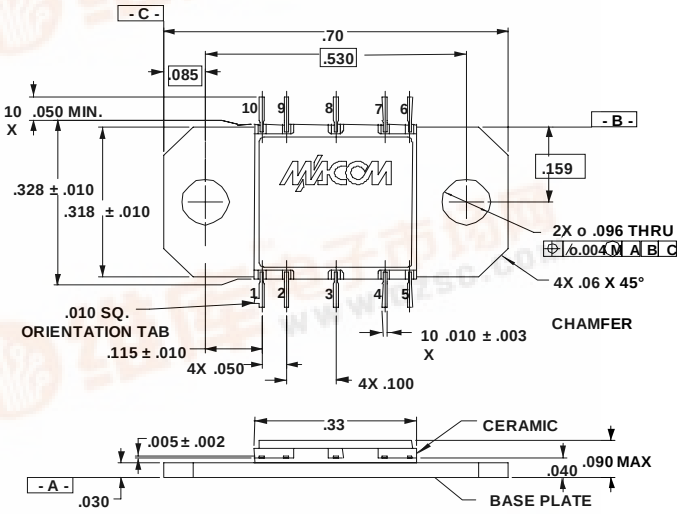
Description

M/A-COM's AM42-0007 is a three-stage MMIC linear power amplifier in a ceramic bolt down style hermetic package. The AM42-0007 employs a fully matched chip with internally decoupled Gate and Drain bias networks and an ouput power detector. The AM42-0007 is designed to be operated from a constant voltage Drain supply.

The AM42-0007 is designed for use as an output stage or a driver, in applications for VSAT systems. This design is fully monolithic and requires a minimum of external components.

M/A-COM's AM42-0007 is fabricated using a mature 0.5 micron GaAs MESFET process. The process features full passivation for increased performance and reliability. This product is 100% RF tested to ensure compliance to performance specifications.

CR-15



Notes: (unless otherwise specified)
1. Dimensions are in inches.
2. Tolerance: .XXX = ± 0.005
.XX = ± 0.010

Ordering Information

Part Number	Package
AM42-0007	Ceramic Bolt Down Package

Electrical Specifications: T_C = +25°C, VDD = +9V, VGG = -5.0V, Z_0 = 50Ω, Frequency = 14.0-14.5 GHz

Parameter	Abbv.	Test Conditions	Units	Min.	Typ.	Max.
Linear Gain	G_L	$P_{IN} \leq 0$ dBm	dB	19	22	—
Input VSWR	$VSWR_{IN}$	$P_{IN} \leq 0$ dBm	—	—	2.5:1	2.7:1
Output VSWR	$VSWR_{OUT}$	$P_{IN} \leq 0$ dBm	—	—	2.7:1	—
Saturated Output Power	P_{SAT}	P_{IN} = +14 dBm	dBm	—	33	—
Output Power @	P_{1dB}	—	dBm	31	32	—
Output IP_3	IP_3	(Refer to Note 1)	dBm	—	41	—
Power Added Efficiency	PAE	P_{IN} = +14 dBm	%	—	22	—
Bias Currents	I_{GG}	P_{IN} = +14 dBm	mA		18	25
Thermal Resistance	θ_{JC}	25°C Heat Sink	°C/W	—	9.5	—
Detector Output Voltage	V_{det}	R_L=10KΩ, P_{OUT} =+31dBm	V	—	+3.5	—

IP_3 is measured with two +24 dBm output tones @ 1 MHz spacing.

■ **North America:** Tel. (800) 366-2266, Fax (800) 618-8883
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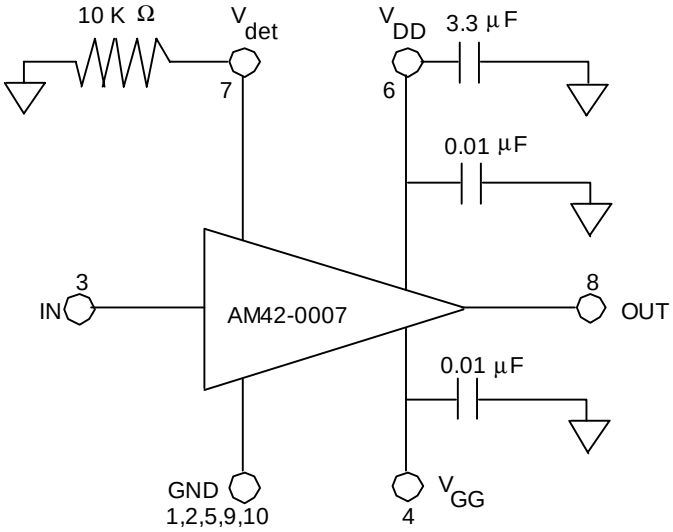
■ **Europe:** Tel. +44 (1344) 869 595, Fax+44 (1344) 300 020

Absolute Maximum Ratings[1,2,3,4]

Parameter	Absolute Maximum
V_{DD}	12 Volts
V_{GG}	-10 Volts
Power Dissipation	13.2 W
RF Input Power	+23 dBm
Channel Temperature	150°C
Storage Temperature	-65°C to +150°C
I_{ds}	2100 mA

1. Operation of this device outside any of these limits may cause permanent damage.
2. Case Temperature (T_C) = +25°C.
3. Nominal bias is obtained by first connecting -5 volts to pin 4 (V_{GG}), followed by connection +9 volts to pin 6 (V_{DD}). Note sequence.
4. RF ground and thermal interface is the flange (case bottom). Adequate heat sinking is required.
5. No dc bias voltage appears at the RF ports.
6. The dc resistance at the input port is an open circuit and at the ouput port is a short circuit.
7. For optimum IP_3 performance, the V_{DD} bypass capacitors should be placed within 0.5 inches of pin 6.

Typical Bias Configuration[3,4,7]



Pin Configuration

Pin No.	Pin Name	Description
1	GND	DC and RF Ground
2	GND	DC and RF Ground
3	IN	RF Input
4	V_{GG}	Gate Supply
5	GND	DC and RF Ground
6	V_{DD}	Voltage Drain Supply
7	V_{det}	Output Power Detector
8	OUT	RF Output
9	GND	DC and RF Ground
10	GND	DC and RF Ground

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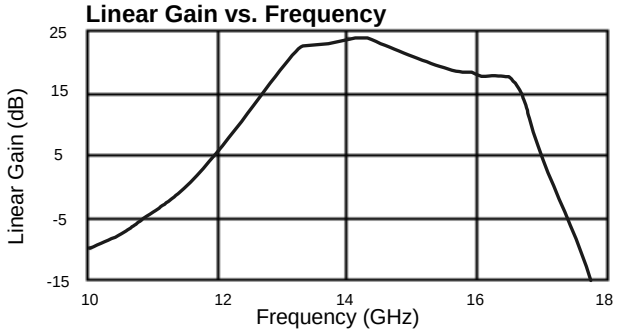
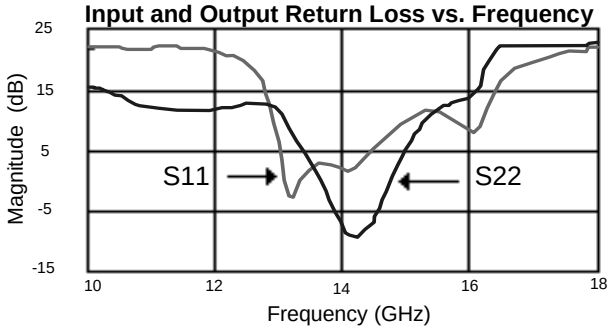
Typical Performance @ +25°C

Test Conditions are listed in the section "Electrical Specifications".

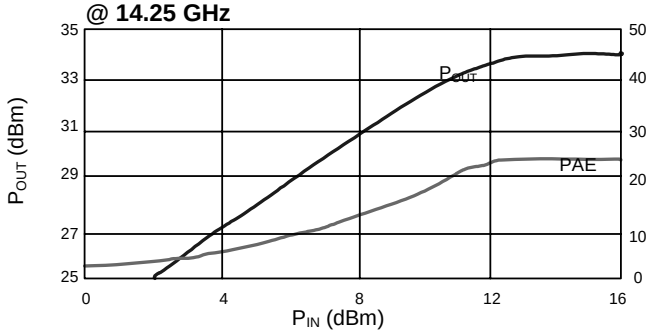
Linear Gain vs. Frequency



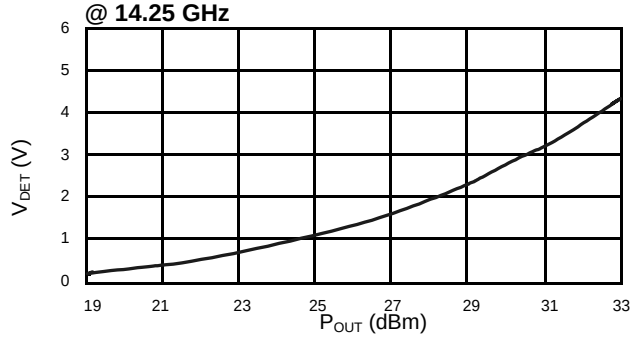
Input and Output Return Loss vs. Frequency



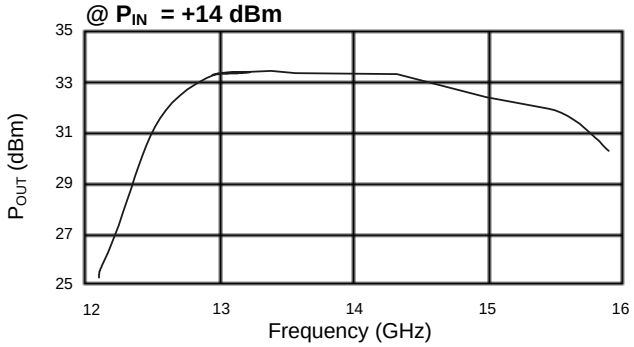
Output Power vs. Input Power @ 14.25 GHz



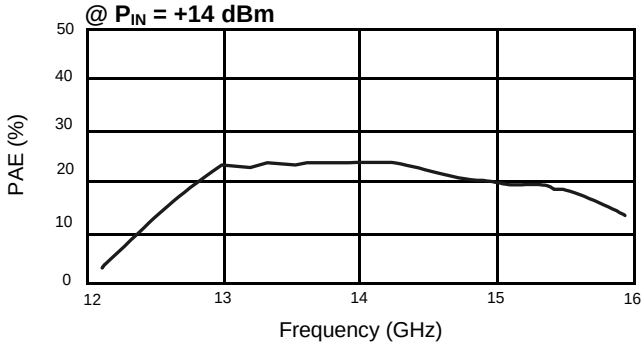
Detector Voltage vs. Output Power @ 14.25 GHz



Output Power vs. Frequency @ P_{IN} = +14 dBm



Power Added Efficiency vs. Frequency @ P_{IN} = +14 dBm



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