Designing A High-Voltage Non-Isolated Buck-Boost Converter with the Si9121DY

Nitin Kalje

INTRODUCTION

The Si9121DY is a non-isolated buck-boost converter IC, operating from a wide input voltage range of –10 to –60 V with minimal external components. This polarity inverter converts –48 V to +5 V or +3.3 V, making it suitable for applications including digital phones and ISDN power supplies. A non-isolated buck-boost design with the Si9121 eliminates the need for an expensive transformer, while its integrated low on-resistance MOSFET driver, floating feedback error amplifier, fixed-frequency oscillator, output voltage sensing resistor divider, and depletion mode MOSFET for start up/V_{CC} regulation reduce the external component count to less than 10. Current-mode control technology achieves good line transient response, making the Si9121DY suitable for the high source impedance environment. Other features include the under-voltage lock out, programmable soft start, pulse by pulse current limit, hiccup mode with negligible power delivery and dissipation during continuous short circuit conditions, automatic recovery from hiccup after fault removal, and over temperature shutdown. The Si9121 is available in a narrow body SO-8 package and allows power dissipation of up to 1.25 W.

DEVICE OPERATION

The Si9121DY uses a current-mode flyback topology to convert the –48-V input to a +5-V or +3.3-V output. As shown in Figure 1, the inductor stores energy during switch-on time, while the output capacitor supports the load current. Since the current in an inductor cannot change instantaneously, the voltage across it reverses to maintain a constant current when the main switch turns off. The reverse voltage is clamped to (V_O + V_D), and the inductor is discharged through the diode, output capacitor, and load.

The energy stored and discharged to the load is proportional to the square of the peak inductor current. At full load, the circuit can be designed to operate in a continuous conduction mode to reduce the peak and RMS currents in the MOSFET switch and an inductor. Operation is in discontinuous mode at lower loads. The constant volt-second product determines the operating duty cycle in continuous conduction mode while the amount of energy needed to be stored in the inductor determines the duty cycle in discontinuous conduction mode.

The peak and average inductor currents for continuous mode operation are:

$$I_{L(AVG)} = \frac{I_{OUT}}{\sqrt{1-\delta}} \quad (1)$$

$$I_{L(PK)} = \frac{I_{OUT}}{\sqrt{1-\delta}} + \frac{\Delta I_L}{2} \quad (2)$$

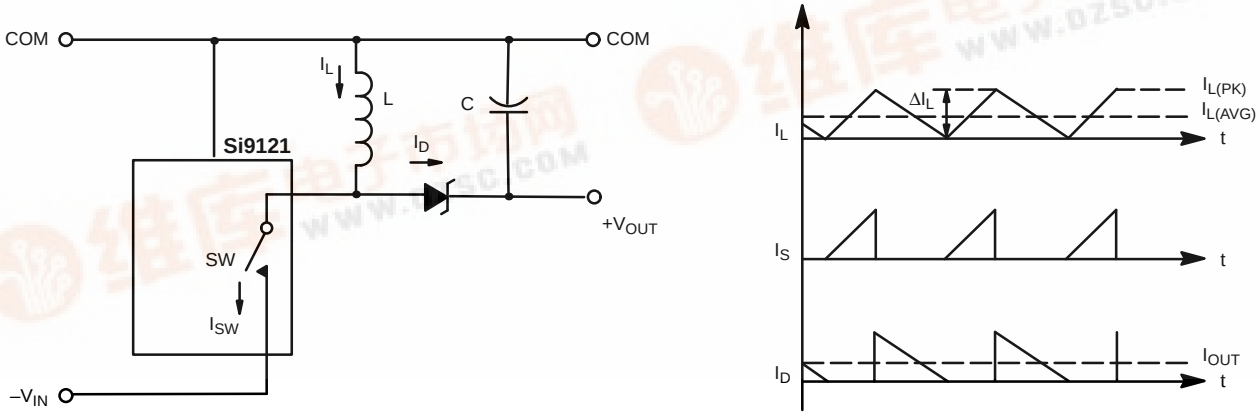


FIGURE 1. Buck-Boost Converter

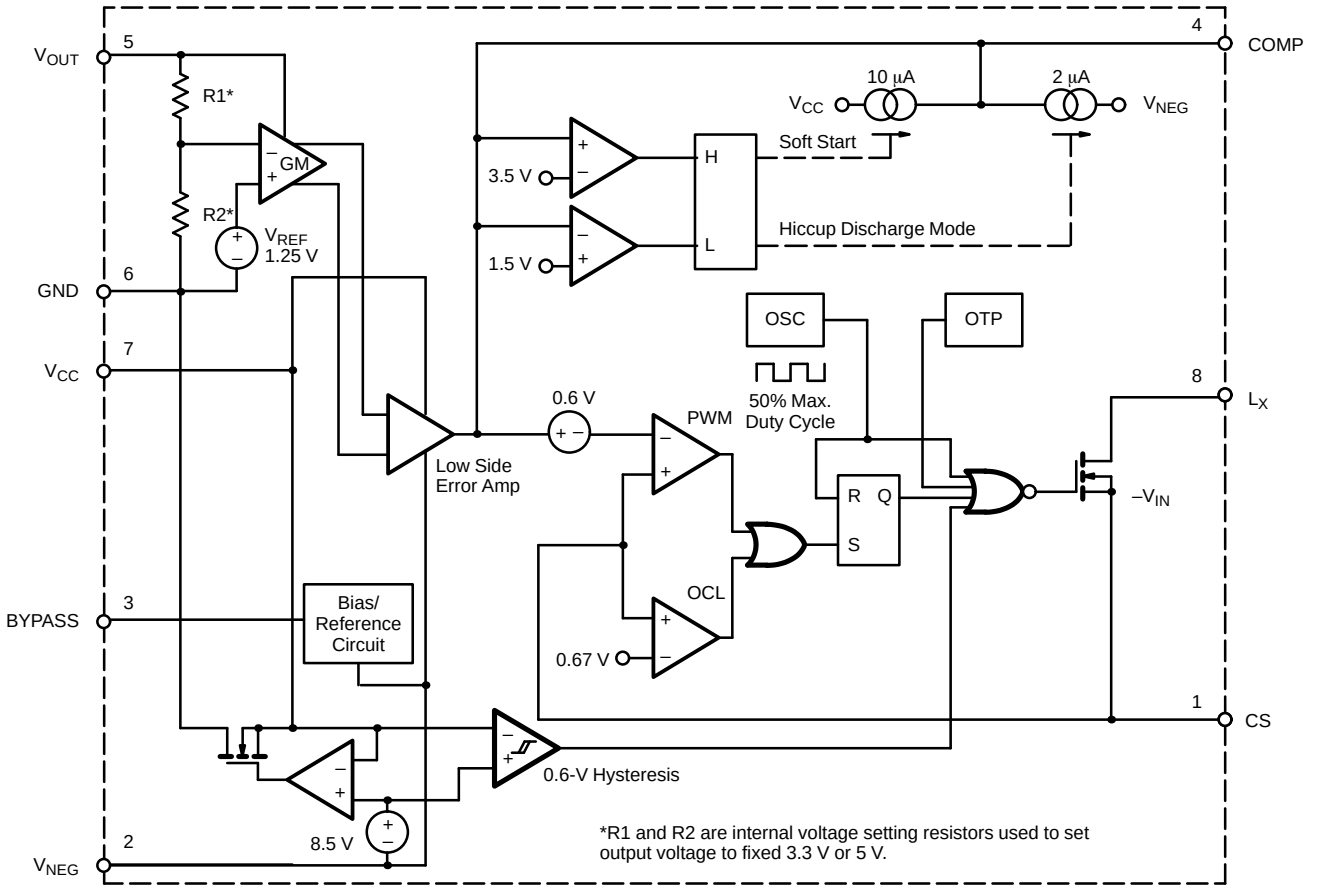


FIGURE 2. Detailed Block Diagram

DESIGN AND COMPONENT SELECTION GUIDELINES

The following sections provide an outline of considerations for designing a buck-boost converter using the Si9121DY. The component selection is based on the 100-kHz operating frequency to achieve maximum efficiency. An inductor, input/output filter, a tantalum or low-cost aluminum capacitor, a Schottky diode, and a few resistors/capacitors are required for a complete solution.

Inductor

Selection of the inductor is based on the inductance value, the maximum temperature rise of the coil at maximum load current, and peak saturating current. The temperature rise is related to the power dissipation and/or efficiency. The higher inductance value drives the converter in continuous mode operation, reducing the RMS currents but at the same time increasing the size of the inductor for the same current handling capability. To find a balance, select a load current ($I_{O(min)}$) that is slightly lower than the operating load current at which the converter begins continuous current mode operation at a nominal line. Use the following equation to calculate the inductance:

$$L_{MIN} = \frac{(V_{OUT} + V_D)\ (1 - \delta)^2}{2\ I_{OMIN}\ F_{SW}} \quad (3)$$

$$\delta = \frac{(V_{OUT} + V_F)}{(V_{IN} - V_{SW}) + (V_{OUT} + V_F)} \quad (4)$$

Where,

L_{MIN} = min Inductance for continuous conduction mode operation at V_{IN} and I_{OUT} (H)

$I_{O(min)}$ = min load current required for in continuous conduction mode (A)

V_{OUT} = Output voltage (V)

V_{IN} = Nominal Input voltage (V)

V_F = Diode Forward drop at I_O (V)

V_{SW} = Voltage drop across MOSFET + current sense resistor at I_O (V)

F_{SW} = Switching frequency (Hz)

δ= Duty Cycle

During start-up, the inductor on-current can reach the threshold current limit, $I_{PK\_LIMIT} = V_{CS}/R_{SENSE}$. For efficient energy storage and transfer, the inductor must be operated below its saturating flux density. Make sure that the peak saturating inductor current I_{SAT} is more than the worst-case threshold current limit. Use the follow equation to calculate:

$$I_{SAT} > \frac{0.77}{R_{SENSE}} \quad (5)$$

Output Capacitor

In the buck-boost converter, both the input and output capacitor currents are pulsating or discontinuous. Obviously, to achieve acceptable ripple performance, a much higher capacitance and lower equivalent series resistance (ESR) are needed at both input and output to support these pulsating currents. In continuous current mode, the amount of capacitance needed is a function of the output load and the switching frequency, for a given pk-pk ripple caused by loss of charges (ΔV_{OC}). Use following equation to choose the capacitor value C_{OUT} for continuous conduction mode operation.

$$C_{OUT} \geq \frac{I_{OMAX} \times \frac{V_{OUT}+V_F}{(V_{INMIN}-V_{SW})+(V_{OUT}+V_F)}}{F_{SW} \times \Delta V_{OC}} \quad (6)$$

The input impedance of the capacitor (ESR at a switching frequency) causes the output voltage to drop when the output load current is supplied by the capacitor. In continuous current mode, the ESR needed to limit the pk-pk ripple to ΔV_{OESR} can be calculated using equation 7.

$$ESR \leq \frac{\Delta V_{OESR}}{I_{L(PEAK)}}$$

or

$$ESR \leq \frac{\Delta V_{OESR}}{\frac{I_O}{1-\delta_{MAX}} + \frac{\Delta I_L}{2}} \quad (7)$$

Where,

$$\Delta I_L = \frac{V_{INMIN} \times \delta_{MAX}}{L \times F_{SW}}$$

The available output ripple is sum of the two ripple components ΔV_{OC} and ΔV_{OESR}.

Total $\Delta V_{O(pk-pk)} = \Delta V_{OC} + \Delta V_{OESR}$

COMPENSATION/SOFT START NETWORK

To reduce the number of external components, the Si9121DY uses the same external components for multiple functions. While selecting the R2, C7, and C8 network for lead lag compensation, the soft-start action sequence needs to be considered as well (Figure 3). At start-up, once the V_{CC} reaches above UVLO threshold, the COMP steps up to 1.5 V. The R2, C7, C8 combination at the COMP start charging with 10-μA of current. During this period, the duty cycle slowly opens up with the voltage rise at error output (COMP), and output starts rising during time t1 (Figure 3). During this period, the amount of energy delivered to charge the output capacitor and support the load current depends on the inductance and peak current passing through it. This continues until the output V_{OUT} reaches approximately 2.5 V, at which point the soft-start charging current increases to 25 μA. The soft start charging current passing through resistor R2 shoots up the error amplifier output voltage to $V_{C\text{-}pk}$, where the OCL comparator limits the maximum current in the inductor during on time. Care must be taken to keep $V_{C\text{-}pk}$ below 3.5 V. If V_{COMP} exceeds an upper threshold (approximately 3.5 V), the timer is started. This will discharge the compensation network capacitor and the converter will unintentionally enter into hiccup mode. Use the following equation to determine the resistor value R2.

$$R2 \leq \frac{V_{C\_PK}-1.5}{25\ \mu A}$$

The output capacitor and the load resistor R_L introduce the power stage pole (fp1). This pole causes gain rollover at a rate of 20db/decade.

$$f_{P1} = \frac{1}{2\pi\ C_{OUT}\ R_L} \quad (8)$$

The low frequency zero (fz1) should be placed before the power stage low-frequency pole (fp1) introduced by output capacitor and the load resistor R_L. Placing the fz1 as early as possible on the frequency scale maintains the low frequency gain.

$$f_{Z1} = \frac{1}{2\ \pi\ R7\ \left(\frac{C7\ C8}{C7+C8}\right)} \quad (9)$$

The capacitor ESR introduces zero at the frequency where the impedance offered by the ESR is equal to the capacitive impedance. At this frequency, the gain tends to go flat.

$$f_{Z-ESR} = \frac{1}{2\pi\ C_{OUT} \times ESR} \quad (10)$$

The high frequency error amplifier pole (fp2) is needed to make the compensation independent of the output capacitor's ESR and to eliminate high-frequency noise spikes.

$$f_{p2} \leq f_{Z-ESR}$$

and,

$$f_{p2} = \frac{1}{2\ \pi\ R7C8} \quad (11)$$

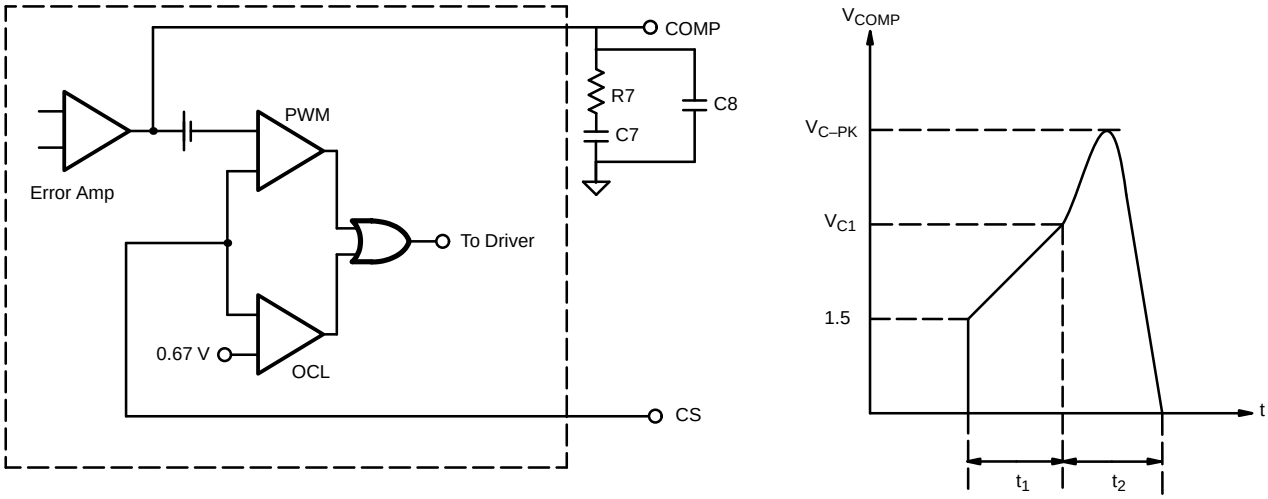
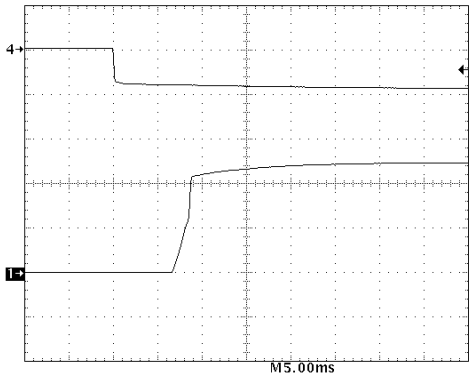


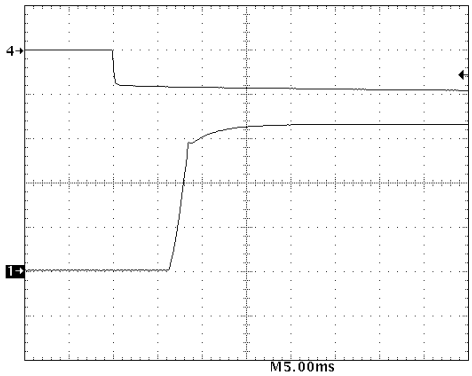
FIGURE 3. Start-Up Sequence V_{COMP}

Refer to Figures 4 and 5 to observe the turn on with the R2, C7, C8 values from the typical application circuit of Figure 6.



Ch 1 = V_{OUT} (2 V/div
Ch 4 = V_{IN} (50 V/div)

FIGURE 4. Turn On—Si9121DB–5



Ch 1 = V_{OUT} (1 V/div
Ch 4 = V_{IN} (50 V/div)

FIGURE 5. Turn On—Si9121DB–3

Diode

The output rectifier diode should be chosen carefully to maintain high-efficiency operation. The forward break down voltage (V_F) is a more significant factor for low output voltages, especially the 3.3-V_{OUT}. Up to 15% efficiency can be lost in the high V_F of the rectifier if this is not chosen carefully. The output diode is forward biased when the MOSFET switch turns off and provides a path for the inductor current. This means the peak current through the diode is quite high, even if the average current is same as the load current I_O. A lower forward drop at high peak currents, lower reverse recovery current/times, and a high reverse breakdown voltage V_{RRM} are key criteria for a good rectifier. The higher reverse recovery current of the rectifier can increase the power dissipation in the MOSFET significantly since the MOSFET is hard switched from high input voltages. A Schottky rectifier is recommended because of its low forward drop V_F and zero reverse recovery resulting from the absence of minority carrier conduction.

Select a Schottky diode with peak reverse voltage $V_{RRM} \geq V_{IN(MAX)} + V_{O(MAX)}$ and average forward current of $I_{F(AVG)} \geq I_{OUT}$.

Current Sense Resistor R_{SENSE}

The Si9121DY has two integrated comparators. The PWM comparator, which is relatively slow, performs the current mode control function by comparing the output of the error amplifier with the current in the inductor. The over current limit (OCL) comparator is a faster channel to the output driver and has a 100-ns typical propagation time.

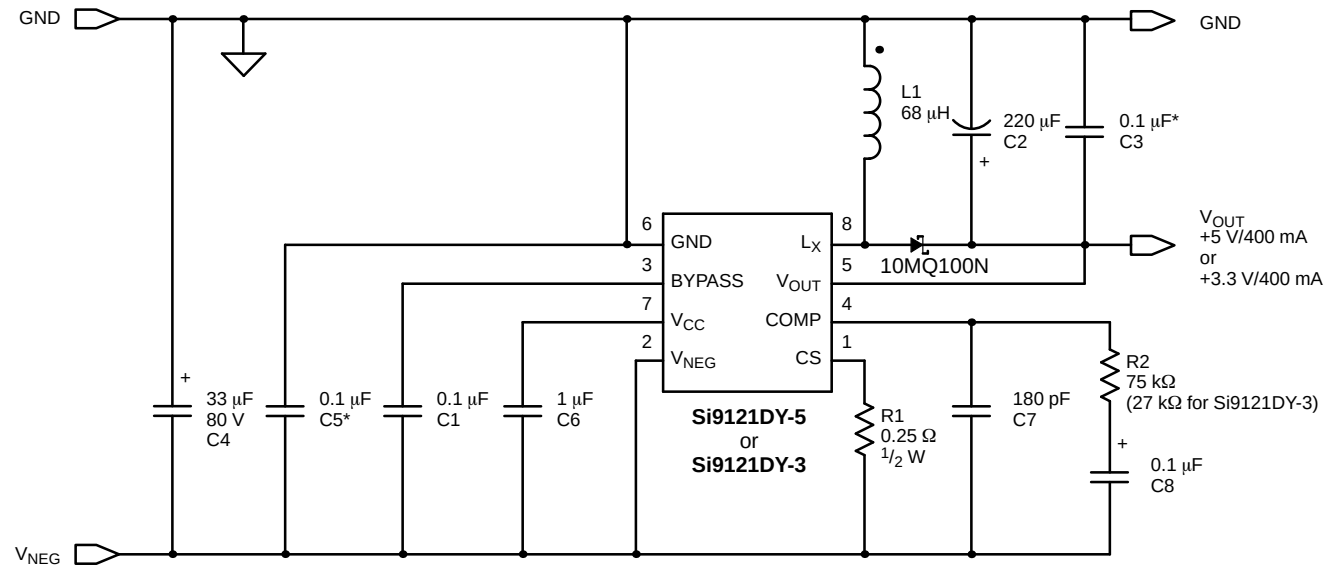


FIGURE 6. Typical Applications Circuit

With the current sense resistor in the inductor current path at turn on, a voltage signal which is proportional to the inductor current is available to control the switch-on period. This signal is used by both the PWM as well as the OCL comparator. The selection of an R_{SENSE} resistor value is based on the allowable peak current in the inductor before saturation and the energy delivery capacity of the converter to charge the output capacitor, while supporting the load current during converter switch-on. A 0.25-Ω resistor value is recommended for avoiding a hiccup condition during turn-on when charging a 220-uF output filter capacitor and supporting the 400-mA-output load. Higher resistor values can be used for lower output capacitance and/or a lower output load. The low inductance WSL series resistors from Vishay are recommended to reduce the turn-on current spike at the CS pin and prevent premature cycle termination.

POWER LOSS CONSIDERATIONS

The Si9121DY is provided in an 8-pin SOIC package for low junction-to-ambient thermal resistance and higher power dissipation (up to 1.25 W at room temperature). Sources of power losses in the Si9121DY include the MOSFET on-resistance/cross conduction switching losses (P_{SW}), quiescent current losses in operating the oscillator and control/drive circuit, and the voltage drop across the V_{CC} regulator ($P_{QUISCENT}$).

$$P_t = P_{SW} + P_{QUISCENT}$$

Power losses can be estimated by using the following equation:

$$P_{SW} = I^2_{RMS\_SW} \times R_{DSON} + \frac{(V_{IN} \times I_{L(AVG)})\ (t_r + t_f)\ F_{SW}}{2} \quad (12)$$

$$P_{quiscent} = V_{in} \times I_{GND} + (V_{IN} + V_{OUT})\ I_{OUT\_IC} \quad (13)$$

Where,

I_{RMS_SW} = RMS current in MOSFET (A)

$r_{DS(on)}$ = On resistance of MOSFET at operating junction temperature. (Ω)

$I_{L(avg)}$ = Average inductor current (A) (see Equation 1)

t_r, t_f = Rise and fall time of drain (sec)

I_{GND}, I_{OUT_IC} = GND supply current and V_{OUT} supply current (A) — (see Si9121DY data sheet)

And the junction temperature

$$T_J\ (°C) = 100\ P_t + T_A$$

To achieve good operating lifetime and reliability, the maximum junction temperature should be kept below 125°C.

Another major power loss occurs in the rectifier diode. The power loss in the diode is equal to the product of the output current (I_O) and the forward voltage drop at $I_{L(PK)}/_2$.

$$P_{DIODE} = V_F \times I_O$$

Where,

V_F = Forward voltage drop at $I_{L(pk)}/_2$

Inductor power loss $P_L = I^2_{LRMS} \times R_L$

Where, R_L is the dc resistance.

The ac resistance losses of bare copper wire thinner than 28 AWG can be neglected since the ac ripple current in the inductor is not significant for continuous conduction mode.

Power loss in sense resistor $P_{SENSE} = I^2_{RMS\_SW} \times R_{SENSE}$

P_M = Power loss in capacitor ESR and PCB traces

Total converter power loss $P_{TOTAL} = P_t + P_{DIODE} + P_L + P_M$

OTHER APPLICATIONS

A high-efficiency buck-boost converter needs to account for every milliwatt power dissipation. There are many ways to achieve high efficiency at lower power levels, such as reducing the switching frequency, but at the cost of a larger form factor. The fixed 100-kHz switching frequency used in the Si9121DY provides an optimal balance between size and efficiency.

Another way of reducing power losses is to apply the V_{CC} voltage externally, instead of deriving it from V_{IN} through internal V_{CC} regulator.

When power is first applied during start-up, the Si9121DY will draw a constant current. The magnitude of this current is determined by a high-voltage depletion MOSFET device which is connected between V_{GND} and V_{CC}. This start-up circuitry provides initial power to the IC by charging an external bypass capacitance connected to the V_{CC} pin. The constant current is disabled when V_{CC} exceeds 9.5 V(max). Adding another winding on the inductor can generate an external V_{CC}. See Figure 7 for an application schematic.

When the MOSFET switch turns on, the transformer phasing induces the voltage across the V_{CC} winding N_S such that the diode D2 is reverse biased. When the mosfet switch turns off, the voltage across the inductor's main windings Np and $N_S$changes the polarity, making the diode forward-biased. The voltage across N_S is proportional to $V_{OUT} + V_{D2}$. The externally generated V_{CC} must be in the range of 9.5 V to 12 V.

Use equations 14, 15 and 16 to calculate the required number of turns for the V_{CC} winding for a given V_{OUT}. A 12-V zener placed between V_{CC} and V_{NEG} is recommended to keep the V_{CC} below its absolute maximum rating.

$$N_S = \frac{N_P\ (V_{CC} + V_{D2})}{(V_{OUT} + V_{DI})} \qquad (14)$$

or

$$N_S = 1.9\ N_P \quad \text{(for Si9121–5)} \qquad (15)$$

$$N_S = 2.87\ N_P \quad \text{(for Si9121–3)} \qquad (16)$$

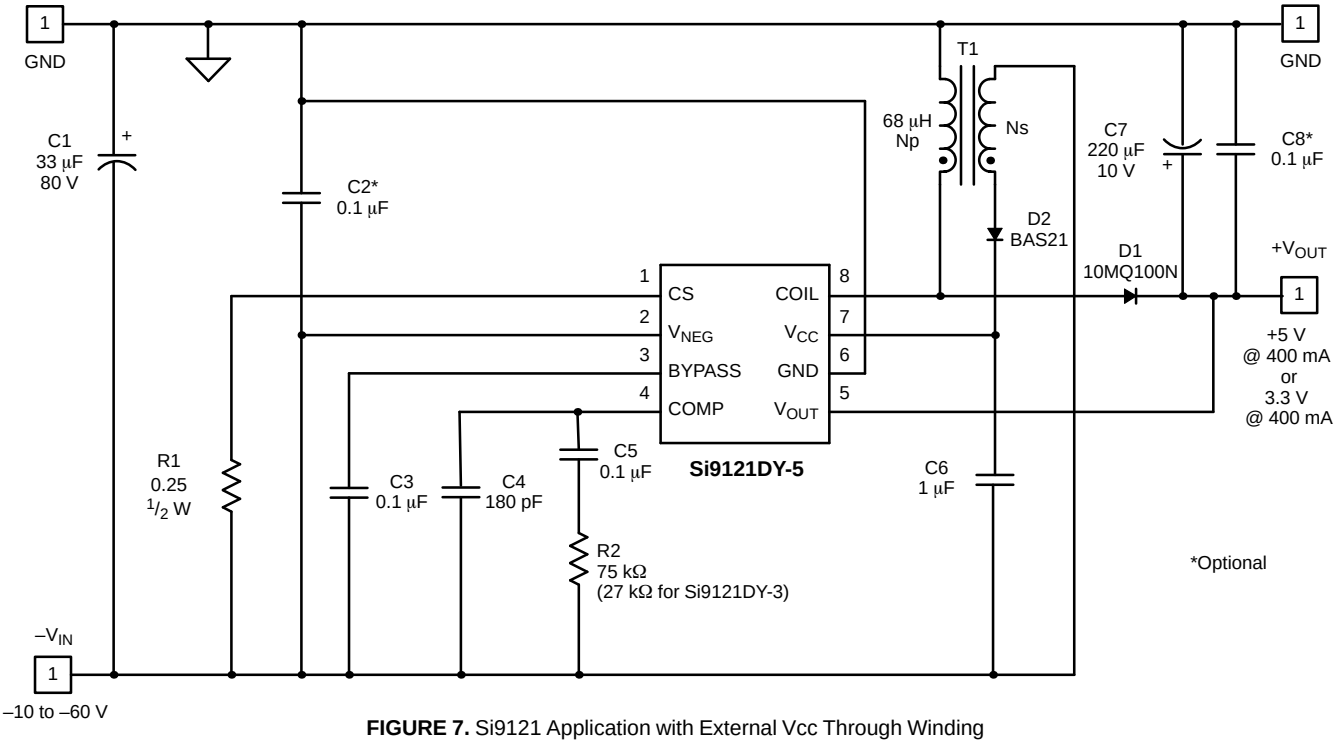


FIGURE 7. Si9121 Application with External Vcc Through Winding

Rectifier diode D2 should be a fast recovery switching signal diode with a reverse blocking voltage rating greater than or equal to V_{RRM}, as calculated from equations 17 and 18.

$$V_{RRM} > 1.9\ V_{INMAX} + V_{CC} \quad \text{(for Si9121–5)} \qquad (17)$$

$$V_{RRM} > 2.87\ V_{INMAX} + V_{CC} \quad \text{(for Si9121–3)} \qquad (18)$$

The BAS21 from Lite On is recommended (Figure 7). Refer to Figures 8 and 9 to observe the efficiency improvement after using an additional winding for the external V_{CC}.

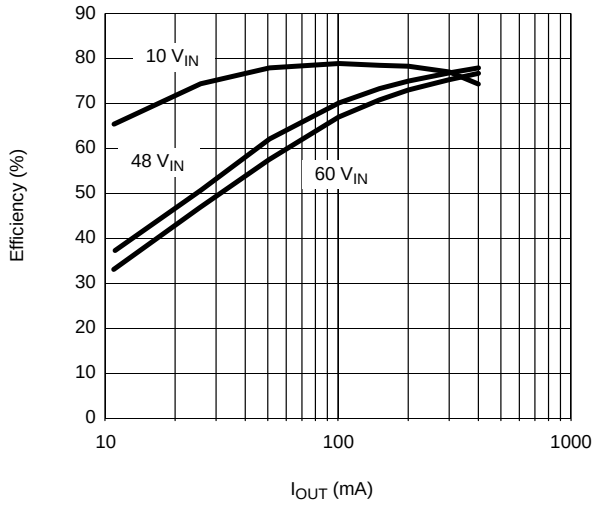


FIGURE 8. Efficiency—Si9121-5 (Without V_{CC} Winding)

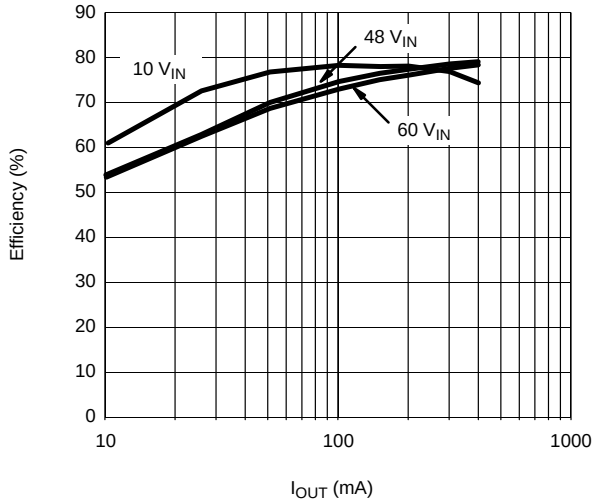


FIGURE 9. Efficiency—Si9121-5 (With V_{CC} Winding)