AN8816SB

4ch. Linear Driver IC for CD/CD-ROM

■ Overview

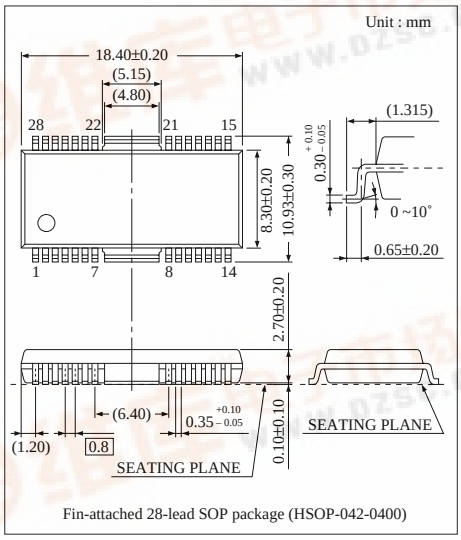
The AN8816SB is a 4ch. driver using the power operational amplifier method. It employs the surface mounting type package superior in radiation characteristics.

■ Features

- Wide output D-range is available regardless of reference voltage on the system
- Setting of driver input/output gain enabled by external resistance
- 2ch. independently controllable PC (Power Cut) feature built-in
- Thermal shut down circuit (with hysteresis) built-in
- Proper heat of IC controllable by separating the output supply and setting each independently for 2ch.
- Construction of 5V supply enabled by external PNP Tr
- Accessary operational amplifier built-in
- Relatively easy pattern design by separating and concentrating the input line and output line

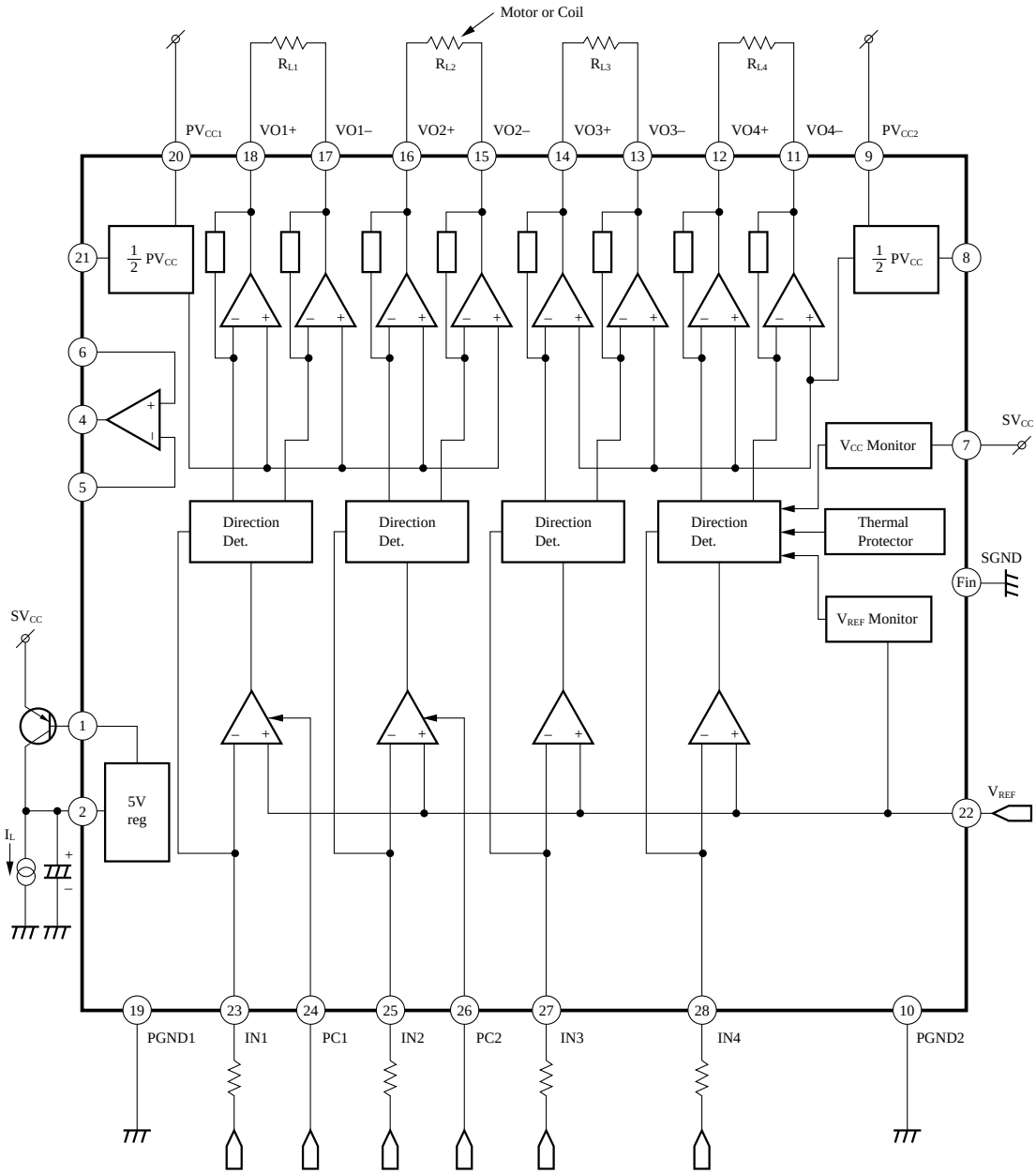
■ Application

Actuator for CD/CD-ROM, motor driver



Fin-attached 28-lead SOP package (HSOP-042-0400)

■ Block Diagram



■ Absolute Maximum Ratings (Ta=25˚C)

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{CC}	18	V
Supply Current	I_{CC}	—	mA
Power Dissipation Note)	P_D	3141	mW
Operating Ambient Temperature	T_{opr}	–30 ~ + 85	˚C
Storage Temperature	T_{stg}	–55 ~ + 150	˚C

Note) For surface mounting on 100 × 80 × 1.6 mm double face glass epoxy board.

■ Recommended Operating Range (Ta=25˚C)

Parameter	Symbol	Range
Operating Supply Voltage Range	SV_{CC} Note)	5.5V ~ 14V
	PV_{CC1}, PV_{CC2}	

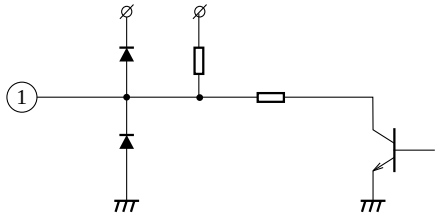
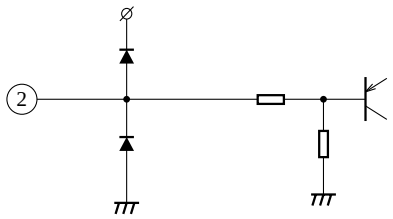
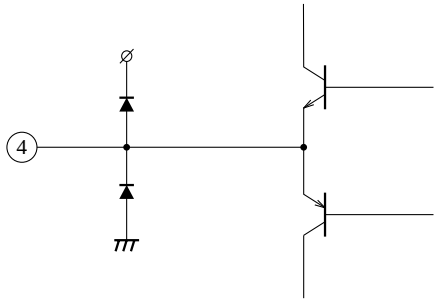
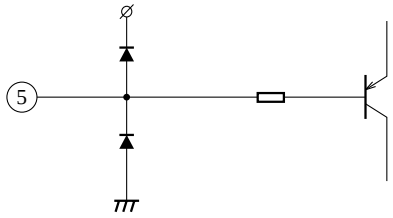
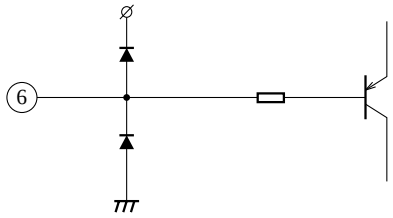
Note) Set SV_{CC} to the maximum electric potential.

■ Electrical Characteristics (Ta=25˚C)

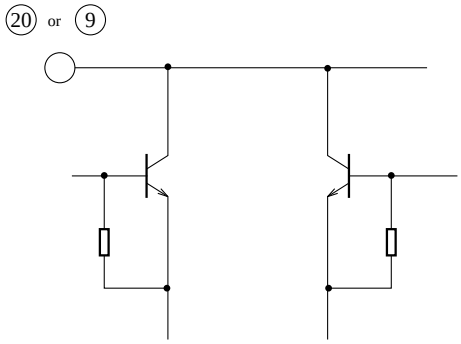
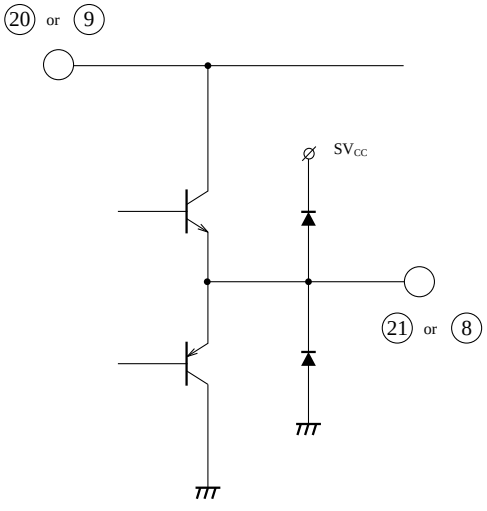
Parameter	Symbol	Condition	min.	typ.	max.	Unit
Total Circuit Current	I_{tot}	$PV_{CC1} = PV_{CC2} = SV_{CC} = 8V$	5	10	15	mA
Drivers 1 to 4						
Input Offset Voltage	V_{IOF}	$PV_{CC1} = PV_{CC2} = SV_{CC} = 8V$, $R_L = 8\Omega$, $R_{IN} = 10k\Omega$	–10	—	10	mV
Output Offset Voltage	V_{OOF}	$PV_{CC1} = PV_{CC2} = SV_{CC} = 8V$, $R_L = 8\Omega$, $R_{IN} = 10k\Omega$	–50	—	50	mV
Gain	G	$PV_{CC1} = PV_{CC2} = SV_{CC} = 8V$, $R_L = 8\Omega$, $R_{IN} = 10k\Omega$	18	20	22	dB
Maximum Output Amplitude (+)	V_{L+}	$PV_{CC1} = PV_{CC2} = SV_{CC} = 8V$, $R_L = 8\Omega$, $R_{IN} = 10k\Omega$	4.4	5.0	—	V
Maximum Output Amplitude (–)	V_{L-}	$PV_{CC1} = PV_{CC2} = SV_{CC} = 8V$, $R_L = 8\Omega$, $R_{IN} = 10k\Omega$	—	–5.0	–4.4	V
Threshold H	V_{PCH}	$PV_{CC1} = PV_{CC2} = SV_{CC} = 8V$, $R_L = 8\Omega$, $R_{IN} = 10k\Omega$	2.0	—	—	V
Threshold L	V_{PCL}	$PV_{CC1} = PV_{CC2} = SV_{CC} = 8V$, $R_L = 8\Omega$, $R_{IN} = 10k\Omega$	—	—	0.3	V
Reset Circuit						
Reset Operation Release Supply Voltage	V_{RST}	$I_{IN} = 10\mu A$, $R_{IN} = 10k\Omega$	3.0	3.2	3.3	V
V_{REF} Detection	V_{REF}		2.0	—	—	V
5V Regulator						
Output Voltage	V_{REG}	$PV_{CC1} = PV_{CC2} = SV_{CC} = 8V$	4.75	5.0	5.25	V
Output Load Fluctuation	DV_R	$PV_{CC1} = PV_{CC2} = SV_{CC} = 8V$	–50	—	50	mV
Supply Voltage Fluctuation	DV_V	$PV_{CC1} = PV_{CC2} = SV_{CC}$ = 8V~12V	–5	—	5	mV
OP Amp.						
Input Offset Voltage	V_{OF}	$PV_{CC1} = PV_{CC2} = SV_{CC} = 8V$	–5	—	5	mV
Input Bias Current	I_{BOP}	$PV_{CC1} = PV_{CC2} = SV_{CC} = 8V$	—	100	500	nA
High Level Output Voltage	V_{OH}	$PV_{CC1} = PV_{CC2} = SV_{CC} = 8V$	6.0	—	—	V
Low Level Output Voltage	V_{OL}	$PV_{CC1} = PV_{CC2} = SV_{CC} = 8V$	—	—	1.7	V
Output Drive Current Sink	I_{SIN}	$PV_{CC1} = PV_{CC2} = SV_{CC} = 8V$	2.0	—	—	mA
Output Drive Current Source	I_{SOU}	$PV_{CC1} = PV_{CC2} = SV_{CC} = 8V$	2.0	—	—	mA
Heat Protection Circuit						
Operation Temperature Equilibrium Value Note 1)	T_{THD}		(—)	(180)	(—)	˚C
Operation Temperature Hysteresis Width Note 1)	DT_{THD}		(—)	(45)	(—)	˚C

Note 1) Characteristic value in parentheses is a reference value for design but not a guaranteed value.

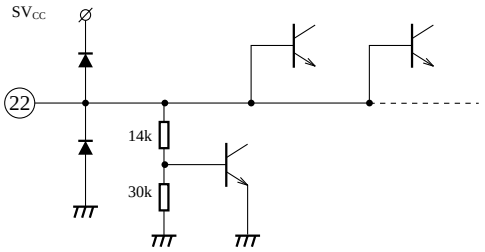
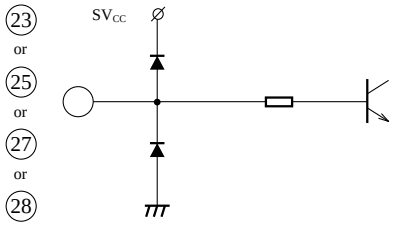
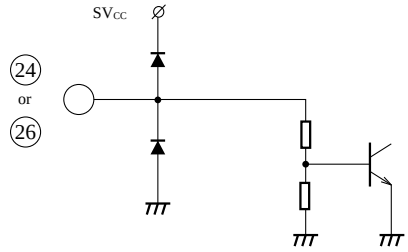
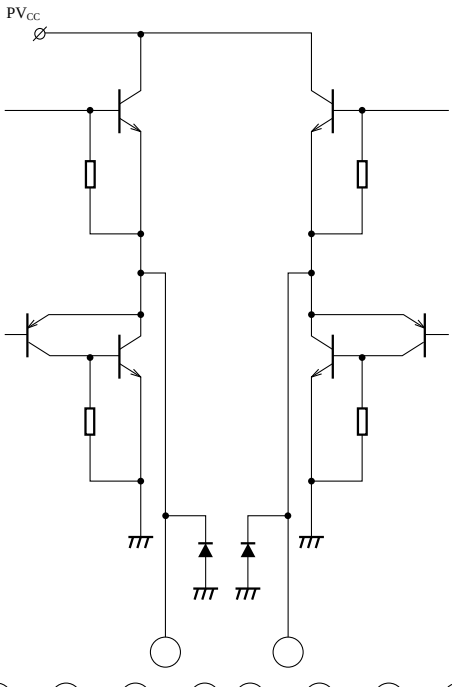
■ Pin Description

Pin No.	Symbol	I/O	Pin Description	Equivalent Circuit
1	TB	O	Output pin for controlling the power transistor base of 5V	
2	V_{MON}	I	Monitor input pin for 5V regulator output	
4	OPO	O	Output pin of op-amp.	
5	IN–	I	Inverting input pin of op-amp.	
6	IN+	I	Non-inverting input pin of op-amp.	
7	SV_{CC}	—	SV_{CC} pin for driver control circuit, not connected with power V_{CC} pin	

■ Pin Description (Cont.)

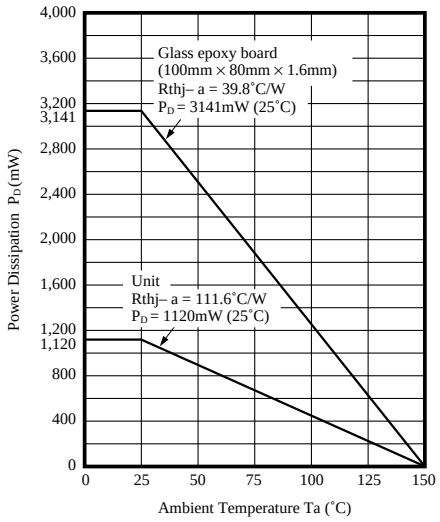
Pin No.	Symbol	I/O	Pin Description	Equivalent Circuit
Fin	SGND	—	SGND pin for driver control circuit	
20	$PV_{CC}1$	—	Power V_{CC} pin supplying the current flowing in output power transistors, 15, 16, 17, and 18	
9	$PV_{CC}2$	—	Power V_{CC} pin supplying the current flowing in output power transistors, 11, 12, 13, and 14	
19	PGND1	—	GND pin for output transistors 15, 16, 17, and 18	
10	PGND2	—	GND pin for output transistors 11, 12, 13, and 14	
21	$\frac{1}{2}PV_{CC}1$	O	$\frac{1}{2}PV_{CC}$ output pin 1	
8	$\frac{1}{2}PV_{CC}2$	O	$\frac{1}{2}PV_{CC}$ output pin 2	

■ Pin Description (Cont.)

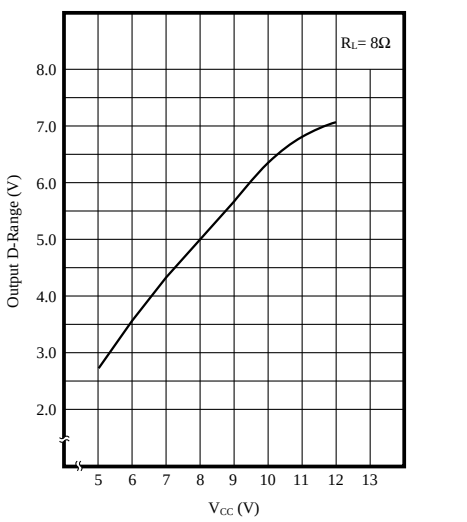
Pin No.	Symbol	I/O	Pin Description	Equivalent Circuit
22	V_{REF}	I	V_{REF} input pin	
23	IN1	I	Input pin of Driver 1	
25	IN2	I	Input pin of Driver 2	
27	IN3	I	Input pin of Driver 3	
28	IN4	I	Input pin of Driver 4	
24	PC1	I	Power cut input pin of Driver 1	
26	PC2	I	Power cut input pin of Driver 2	
11	VO4–	O	Reverse rotation output pin of Driver 4	
12	VO4+	O	Normal rotation output pin of Driver 4	
13	VO3–	O	Reverse rotation output pin of Driver 3	
14	VO3+	O	Normal rotation output pin of Driver 3	
15	VO2–	O	Reverse rotation output pin of Driver 2	
16	VO2+	O	Normal rotation output pin of Driver 2	
17	VO1–	O	Reverse rotation output pin of driver 1	
18	VO1+	O	Normal rotation output pin of Driver 1	

■ Characteristic Curve

P_D –Ta



V_{CC} – Maximum Output Amplitude Characteristics



■ Description for use

• Driver Portion

Calculate the driver gain by using the following formula for setting.

$$G = \frac{60k\Omega}{R_{IN1}+100\ (\Omega)} \times 2$$

The power supply for Ch.1 and 2 is supplied from Pin20 and the power supply for Ch.3 and 4 is supplied from Pin9 independently.

Output amplitude is increased by increasing the supply voltage. Set the power supply voltage as necessary. However, always set Pin7 of V_{CC} to the maximum electric potential.

Pin8 and 21 may require a capacitor for ripple removal.

As protection functions, V_{CC} reset circuit,V_{REF} detector and heat protection circuit are incorporated.

The V_{CC} reset circuit operates at approx. 3V and is released at 3.2V, when the supply (Pin7) decreases. For the V_{REF} detector, the protection function works at approx. 1V (max. 2V).

Also, the set temperature for operation of the heat protection circuit is approx. 180˚C .

PC (Power Cut) functions which can be independently controlled are incorporated in Ch.1 and 2.

• 5V Supply

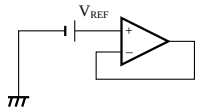
By adding an external PNP transistor, 5V regulator can be constructed. Attach an external capacitor for loop filter to output Pin2.

In Pin1, the base current limiting circuit (typ. 10mA) is incorporated.

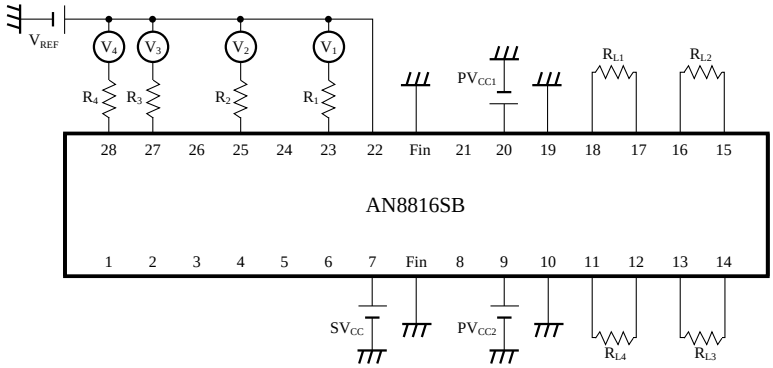
When the V supply is used, the external PNP Tr emitter must be connected to pin than Pin7 (SV_{CC} pin)

• OP Amp.

When the operational amplifier is not used, make connection as follows ;



■ Cautions for use



When the AN8816SB is used, take into account the following cautions and follow the power dissipation characteristic curve.

(1) Load current, I_{P1} flowing in loads R_{L1} and R_{L2} is supplied through Pin20.

$$I_{P1} = \frac{|V_{18}-V_{17}|}{R_{L1}} + \frac{|V_{16}-V_{15}|}{R_{L2}}$$

(2) Load current, I_{P2} flowing in loads R_{L3} and R_{L4} is supplied through Pin9.

$$I_{P2} = \frac{|V_{14}-V_{13}|}{R_{L3}} + \frac{|V_{12}-V_{11}|}{R_{L4}}$$

(3) Dissipation increase (DP_d) inside the IC (power output stage) caused by loads R_{L1}, R_{L2}, R_{L3}, R_{L4} is as follow.

$$DP_d = (PV_{CC1}-|V_{18}-V_{17}|) \times \frac{|V_{18}-V_{17}|}{R_{L1}} + (PV_{CC1}-|V_{16}-V_{15}|) \times \frac{|V_{16}-V_{15}|}{R_{L2}} + (PV_{CC2}-|V_{14}-V_{13}|) \times \frac{|V_{14}-V_{13}|}{R_{L3}} + (PV_{CC2}-|V_{12}-V_{11}|) \times \frac{|V_{12}-V_{11}|}{R_{L4}}$$

(4) Dissipation increase (DP_S) inside the IC (signal block supplied from Pinu) caused by loads R_{L1}, R_{L2}, R_{L3}, R_{L4} is almost as follows ;

$$DP_S = 3\left\{\frac{V_1}{R_1}(2SV_{CC}+|V_{18}-V_{17}|) + \frac{V_2}{R_2}(2SV_{CC}+|V_{16}-V_{15}|) + \frac{V_3}{R_3}(2SV_{CC}+|V_{14}-V_{13}|) + \frac{V_4}{R_4}(2SV_{CC}+|V_{12}-V_{11}|)\right\}$$

(5) Dissipation increase during driver running is $DP_d + DP_S$.

(6) Inside loss under no load (P_{d1}) is almost as follows ;

$$P_{d1} = SV_{CC} \times I\,(SV_{CC}) + PV_{CC1} \times I\,(PV_{CC1}) + PV_{CC2} \times I\,(PV_{CC2})$$

(7) Entire IC inside loss (P_d) is almost as follows ;

$$P_d = P_{d1} + DP_d + DP_S$$