AnaChip

Synchronous PWM Controller

AP2003
(Preliminary)

■ Features

- Single or Dual Supply Application
- 0.8V ± 1.0% Voltage Reference.
- Fast transient response.
- Synchronous operation for high efficiency (95%)
- Soft Start functions
- Small size with minimum external components
- Industrial temperature range
- Under Voltage Lockout function
- SOP-8L package

■ Applications

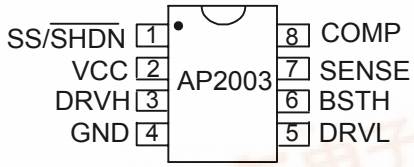
- Microprocessor core supply
- Low cost synchronous applications
- Voltage Regulator Modules (VRM)
- DDR termination supplies
- Networking power supplies
- Sequenced power supplies

■ General Description

The AP2003 is a low-cost, full featured, and synchronous voltage-mode controller designed for use in single ended power supply applications where efficiency is of the primary concern. This synchronous operation allows the elimination of heat sinks in many applications. The AP2003 is ideal for implementing DC/DC converters needed to power advanced microprocessors in low cost systems, or in distributed power applications where efficiency is important. Internal level-shift, high-side drive circuitry, and preset shoot-thru control, allows the use of inexpensive N-channel power switches.
AP2003 features include temperature compensated voltage reference, an internal 200KHz virtual frequency oscillator, under-voltage lockout protection, soft-start, and shutdown function.

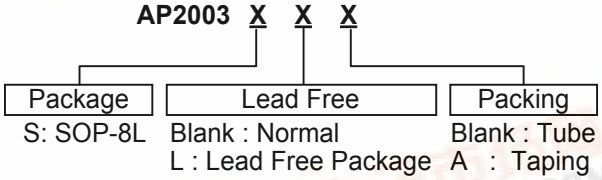
■ Pin Assignment

(Top View)



SOP-8L

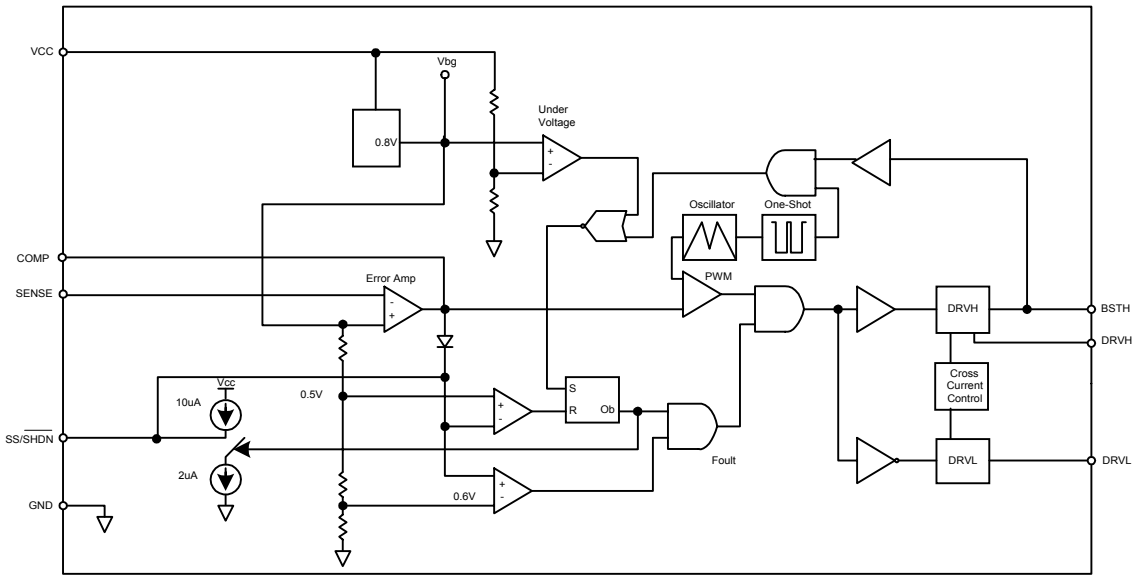
■ Ordering Information



■ Pin Descriptions

Name	Description
VCC	Chip supply voltage
DRVH	High side driver output
DRVL	Low side driver output
BSTH	Bootstrap, high side driver
SENSE	Voltage sense input
COMP	Compensation pin
SS/$\overline{SHDN}$	Soft start, a capacitor to ground sets the slow start time
GND	Ground

■ Block Diagram



■ Absolute Maximum Ratings

Symbol	Parameter	Max.	Unit
V_{IN}	VCC to GND	-1 to 14	V
Θ_{JC}	Thermal Resistance Junction to Case	60	°C/W
Θ_{JA}	Thermal Resistance Junction to Ambient	160	°C/W
T_{OP}	Operating Temperature Range	-40 to +85	°C
T_{ST}	Storage Temperature Range	-65 to +150	°C
T_{LEAD}	Lead Temperature (Soldering) 10 Sec.	300	°C

■ Electrical Characteristics

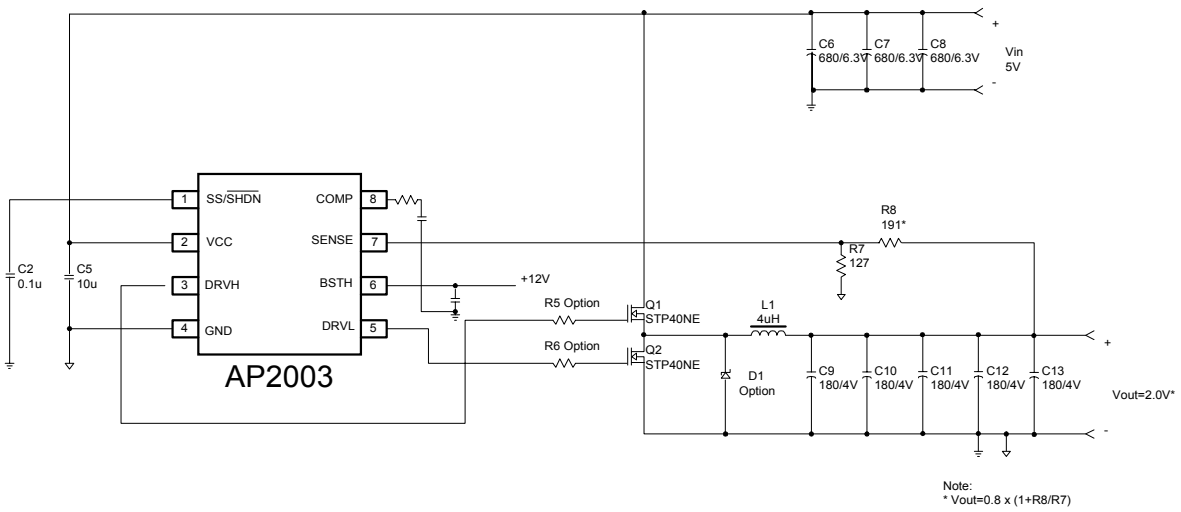
Unless specified: V_{CC} = 12V; GND = 0V; FB = V_O; $V_{BSTH-GND}$ = 12V; T_J = 25°C

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Power Supply						
V_{CC}	Supply Voltage	V_{CC}	4.2		16	V
I_{CC}	Supply Current			6	10	mA
ΔV_{LINE}	Line Regulation	VO = 2.5V		0.5		%
Error Amplifier						
A_{OL}	Gain (A_{OL})			50		dB
I_B	Input Bias			5	8	uA
Oscillator						
F_{OSC}	Oscillator Frequency		180	200	220	KHz
DC_{MAX}	Oscillator Max Duty Cycle		90	95		%
Mofset Drivers						
I_{DRVH}	DRVH Source/Sink	$V_{BSTH} - V_{DRVH}$ =4.5V $V_{DRVH} - V_{PHASE}$ = 2V	1			A
I_{DRVL}	DRVL Source/Sink	$V_{BSTH} - V_{DRVL}$ = 4.5V $V_{DRVL} - V_{GND}$ = 2V	1			A
Protection						
T_{DEAD}	Dead Time		45		100	nS
Reference						
V_{REF}	Reference Voltage	0°C to 70°C	0.792	0.8	0.808	V
	Accuracy		-1		+ 1	%
Soft Start						
I_{SSC}	Charge Current	V_{SS} = 1.5V	8.0	10	12	uA
I_{SSD}	Discharge Current	V_{SS} = 1.5V	1.3	2	2.7	uA
Under voltage lockout (UVLO)						
V_{UT}	Upper threshold voltage (V_{CC})	$I_{O(REF)}$ = 0.1mA T_A = 25ºC		4.2		V
V_{LWT}	Lower threshold voltage (V_{CC})			4.1		V
V_{HT}	Hysteresis (V_{CC})			200		mV

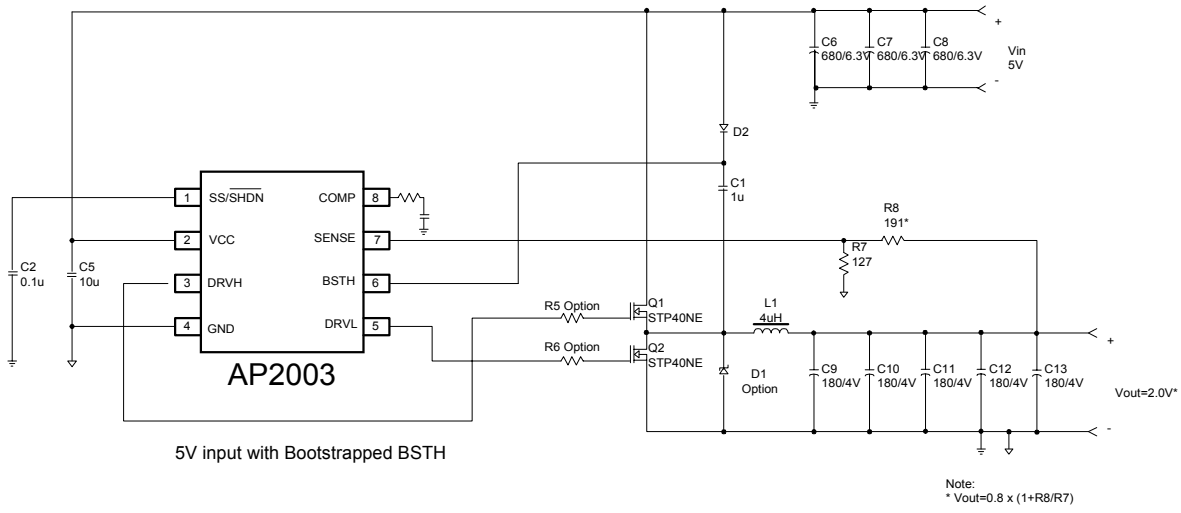
Note 1. Specification refers to Typical Application Circuit.
Note 2. This device is ESD sensitive. Use of standard ESD handling precautions is required.

■ Typical Application Circuit

(1)



(2)



■ Function Description

Synchronous Buck Converter

Primary V_{CORE} power is provided by a synchronous, voltage-mode pulse width modulated (PWM) controller. This section has all the features required to build a high efficiency synchronous buck converter, shutdown function.

The output voltage of the synchronous converter is set and controlled by the output of the error amplifier. The external resistive divider reference voltage is derived from an internal trimmed band-gap voltage reference. The inverting input of the error amplifier receives its voltage from the SENSE pin.

The internal oscillator uses an on-chip capacitor and trimmed precision current sources to set the oscillation frequency to 200KHz. The triangular output of the oscillator sets the reference voltage at the inverting input of the comparator. When the oscillator output voltage drops below the error amplifier output voltage, the comparator output goes high. This pulls DRVL low, turning off the low-side FET, and DRVH is pulled high, turning on the high-side FET (once the cross-current control allows it). When the oscillator voltage rises back above the error amplifier output voltage, the comparator output goes low. This pulls DRVH low, turning off the high-side FET, and DRVL is pulled high, turning on the low-side FET (once the cross-current control allows it).

As SENSE increases, the output voltage of the error amplifier decreases. This causes a reduction in the on-time of the high-side MOSFET connected to DRVH, hence lowering the output voltage.

Under Voltage Lockout

The under voltage lockout circuit of the AP2003 assures that the high-side MOSFET driver outputs remain in the off state whenever the supply voltage drops below set parameters. Lockout occurs if V_{CC} falls below 4.1V. Normal operation resumes once V_{CC} rises above 4.2V.

Soft Start

Initially, SS/$\overline{\text{SHDN}}$ sources 10uA of current to charge an external capacitor. The outputs of the error amplifiers are clamped to a voltage proportional to the voltage on SS/$\overline{\text{SHDN}}$. This limits the on-time of the high-side MOSFETs, thus leading to a controlled ramp-up of the output voltages.

Hiccup Mode

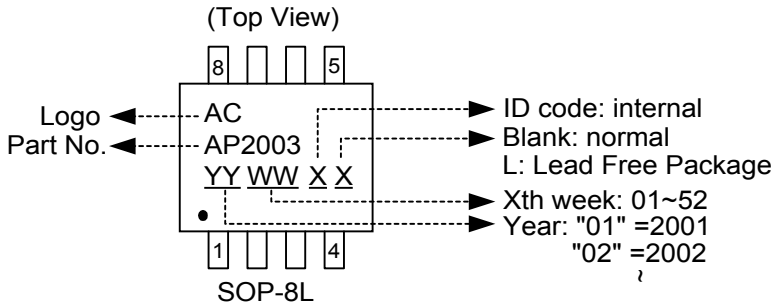
During power up, the SS/$\overline{\text{SHDN}}$ pin is internally pulled low until V_{CC} reaches the under-voltage lockout level of 4.2V. Once V_{CC} has reached 4.2V, the SS/$\overline{\text{SHDN}}$ pin is released and begins to source 10uA of current to the external soft-start capacitor. As the soft-start voltage rises, the output of the internal error amplifier is clamped to this voltage. When the error signal reaches the level of the internal triangular oscillator, which swings from 1V to 2V at a fixed frequency of 200KHz, switching occurs. As the error signal crosses over the oscillator signal, the duty cycle of the PWM signal continues to increase until the output comes into regulation.

The soft-start voltage will begin to decrease as the 2uA of current discharge the external capacitor. When the soft-start voltage reaches 0.8V, the SS/$\overline{\text{SHDN}}$ pin will begin to source 10uA and begin to charge the external capacitor causing the soft-start voltage to rise again. Again, when the soft-start voltage reaches the level of the internal oscillator, switching will occur.

In conclusion, above is shown a typical “12V Application Circuit” which has a BSTH voltage derived by bootstrapping input voltage to the PHASE node through diode D2. This circuit is very useful in cases where only single input power of 5V(or 12V) is available.

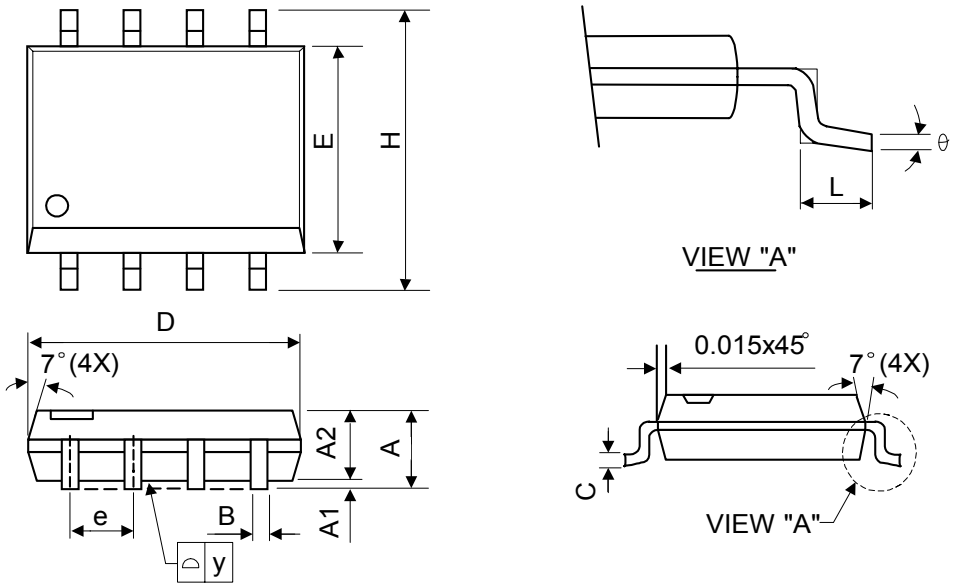
In order to prevent substrate glitching, a small-signal diode should be placed in close proximity to the chip with cathode connected to PHASE and anode connected to GND.

■ Marking Information



■ Package Information

Package Type: SOP-8L



Symbol	Dimensions In Millimeters			Dimensions In Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	1.40	1.60	1.75	0.055	0.063	0.069
A1	0.10	-	0.25	0.040	-	0.100
A2	1.30	1.45	1.50	0.051	0.057	0.059
B	0.33	0.41	0.51	0.013	0.016	0.020
C	0.19	0.20	0.25	0.0075	0.008	0.010
D	4.80	5.05	5.30	0.189	0.199	0.209
E	3.70	3.90	4.10	0.146	0.154	0.161
e	-	1.27	-	-	0.050	-
H	5.79	5.99	6.20	0.228	0.236	0.244
L	0.38	0.71	1.27	0.015	0.028	0.050
y	-	-	0.10	-	-	0.004
θ	0^{O}	-	8^{O}	0^{O}	-	8^{O}