

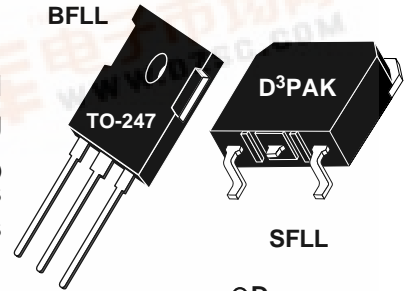


APT10078BFLF

APT10078SFLF

1000V 14A 0.780Ω

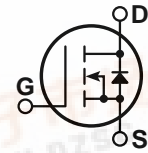
POWER MOS 7™



SFLF

Power MOS 7™ is a new generation of low loss, high voltage, N-Channel enhancement mode power MOSFETS. Both conduction and switching losses are addressed with Power MOS 7™ by significantly lowering $R_{DS(ON)}$ and Q_g . Power MOS 7™ combines lower conduction and switching losses along with exceptionally fast switching speeds inherent with APT's patented metal gate structure.

- Lower Input Capacitance
- Lower Miller Capacitance
- Lower Gate Charge, Q_g
- Increased Power Dissipation
- Easier To Drive
- TO-247 or Surface Mount D³PAK Package
- **FAST RECOVERY BODY DIODE**



MAXIMUM RATINGS

All Ratings: $T_C = 25^\circ\text{C}$ unless otherwise specified.

Symbol	Parameter	APT10078	UNIT
V_{DSS}	Drain-Source Voltage	1000	Volts
I_D	Continuous Drain Current @ $T_C = 25^\circ\text{C}$	14	Amps
I_{DM}	Pulsed Drain Current ^①	56	
V_{GS}	Gate-Source Voltage Continuous	±30	Volts
V_{GSM}	Gate-Source Voltage Transient	±40	
P_D	Total Power Dissipation @ $T_C = 25^\circ\text{C}$	400	Watts
	Linear Derating Factor	3.2	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to 150	°C
T_L	Lead Temperature: 0.063" from Case for 10 Sec.	300	
I_{AR}	Avalanche Current ^① (Repetitive and Non-Repetitive)	14	Amps
E_{AR}	Repetitive Avalanche Energy ^①	30	mJ
E_{AS}	Single Pulse Avalanche Energy ^④	1300	

STATIC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic / Test Conditions	MIN	TYP	MAX	UNIT
BV_{DSS}	Drain-Source Breakdown Voltage ($V_{GS} = 0V, I_D = 250\mu A$)	1000			Volts
$I_{D(on)}$	On State Drain Current ^② ($V_{DS} > I_{D(on)} \times R_{DS(on)}$ Max, $V_{GS} = 10V$)	14			Amps
$R_{DS(on)}$	Drain-Source On-State Resistance ^② ($V_{GS} = 10V, 0.5 I_{D(Cont.)}$)			0.78	Ohms
I_{DSS}	Zero Gate Voltage Drain Current ($V_{DS} = V_{DSS}, V_{GS} = 0V$)			250	μA
	Zero Gate Voltage Drain Current ($V_{DS} = 0.8 V_{DSS}, V_{GS} = 0V, T_C = 125^\circ\text{C}$)			1000	
I_{GSS}	Gate-Source Leakage Current ($V_{GS} = \pm 30V, V_{DS} = 0V$)			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage ($V_{DS} = V_{GS}, I_D = 1mA$)	3		5	Volts

CAUTION: These Devices are Sensitive to Electrostatic Discharge. Proper Handling Procedures Should Be Followed.

APT Website - <http://www.advancedpower.com>

DYNAMIC CHARACTERISTICS

APT10078 BFL - SFL

Symbol	Characteristic	Test Conditions	MIN	TYP	MAX	UNIT
C_{iss}	Input Capacitance	$V_{GS} = 0V$ $V_{DS} = 25V$ $f = 1 \text{ MHz}$		2480		pF
C_{oss}	Output Capacitance			410		
C_{rss}	Reverse Transfer Capacitance			82		
Q_g	Total Gate Charge ^③	$V_{GS} = 10V$ $V_{DD} = 0.5 V_{DSS}$ $I_D = I_D [\text{Cont.}] @ 25^\circ\text{C}$		95		nC
Q_{gs}	Gate-Source Charge			15		
Q_{gd}	Gate-Drain ("Miller") Charge			63		
$t_d(\text{on})$	Turn-on Delay Time	$V_{GS} = 15V$ $V_{DD} = 0.5 V_{DSS}$ $I_D = I_D [\text{Cont.}] @ 25^\circ\text{C}$ $R_G = 1.6\Omega$		10		ns
t_r	Rise Time			5		
$t_d(\text{off})$	Turn-off Delay Time			20		
t_f	Fall Time			7		

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Symbol	Characteristic / Test Conditions	MIN	TYP	MAX	UNIT
I_S	Continuous Source Current (Body Diode)			14	Amps
I_{SM}	Pulsed Source Current ^① (Body Diode)			56	
V_{SD}	Diode Forward Voltage ^② ($V_{GS} = 0V, I_S = -I_D [\text{Cont.}]$)			1.3	Volts
dv/dt	Peak Diode Recovery dv/dt ^⑤			18	V/ns
t_{rr}	Reverse Recovery Time ($I_S = -I_D [\text{Cont.}], di/dt = 100A/\mu s$)	$T_j = 25^\circ\text{C}$		200	ns
		$T_j = 125^\circ\text{C}$		350	
Q_{rr}	Reverse Recovery Charge ($I_S = -I_D [\text{Cont.}], di/dt = 100A/\mu s$)	$T_j = 25^\circ\text{C}$		0.7	μC
		$T_j = 125^\circ\text{C}$		1.8	
I_{RRM}	Peak Recovery Current ($I_S = -I_D [\text{Cont.}], di/dt = 100A/\mu s$)	$T_j = 25^\circ\text{C}$		11	Amps
		$T_j = 125^\circ\text{C}$		17	

THERMAL CHARACTERISTICS

Symbol	Characteristic	MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction to Case			0.31	$^\circ\text{C/W}$
$R_{\theta JA}$	Junction to Ambient			40	

① Repetitive Rating: Pulse width limited by maximum junction temperature.

② Pulse Test: Pulse width < 380 μs , Duty Cycle < 2%

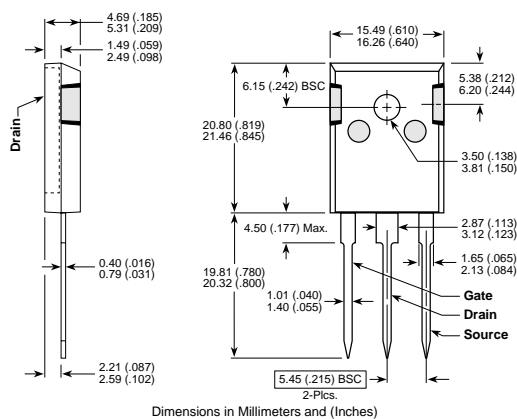
③ See MIL-STD-750 Method 3471

④ Starting $T_j = +25^\circ\text{C}$, $L = 13.26\text{mH}$, $R_G = 25\Omega$, Peak $I_L = 14\text{A}$

⑤ dv/dt numbers reflect the limitations of the test circuit rather than the device itself. $I_S \leq -I_{D[\text{Cont.}]}$, $di/dt \leq 700A/\mu\text{s}$, $V_R \leq V_{DSS}$, $T_j \leq 150^\circ\text{C}$

APT Reserves the right to change, without notice, the specifications and information contained herein.

TO-247 Package Outline



D³PAK Package Outline

