APW7045

Advanced PWM and Linear Power Controller

Features

- 2 Regulated Voltage are provided
  - –Switching Power for Fixed Voltage (1.0V)
  - –Linear Regulator for V_{MEM}(2.5V)
- Simple Single-Loop Control Design
  - –Voltage-Mode PWM Control
- Excellent Output Voltage Regulation
  - –PWM Output: ±1%
  - –Linear Output: ±3%
- Fast Transient Response
  - –High-Bandwidth Error Amplifier
  - –Full 0% to 100% Duty Ratio
- Power-Good Output Voltage Monitor
- Over-Voltage and Over-Current Fault Monitors
- Small Converter Size
  - –200KHz Free-Running Oscillator ; Progammable from 50KHz to 800KHz
  - –Reduce External Component Count

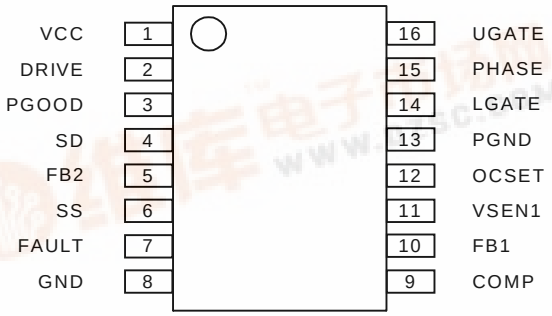
Applications

- Motherboard Power Regulation for Computers
- Low-Voltage Distributed Power Supplies
- VGA Card Power Regulation
- DDR SDRAM Power Regulation

General Description

The APW7045 integrates PWM controller and linear controller, as well as the monitoring and protection functions into a single package, which provides two controlled power outputs with over-voltage and over-current protections. The PWM controller regulates the DDR termination voltage (1.25V) or GPU Voltage (2.05V) with a synchronous-rectified buck converter. The linear controller regulates the Memory Voltage (2.5V). The pre cision reference and voltage-mode PWM control provide ±1% static regulation. The linear controller drives an external N-channel MOSFET to provide adjustable voltage. The APW7045 monitors two output voltages, and a single Power Good signal is issued when the PWM voltage is within ±10% of the DAC setting and the lineat regulator output level is above under-voltage threshold. Additional built-in over-voltage protection for the PWM output uses the lower MOSFET to prevent output voltages above 115% of the DAC setting. The PWM over-current function monitors the output current by using the voltage drop across the upper MOSFET's $R_{DS(ON)}$, eliminating the need for a current sensing resistor.

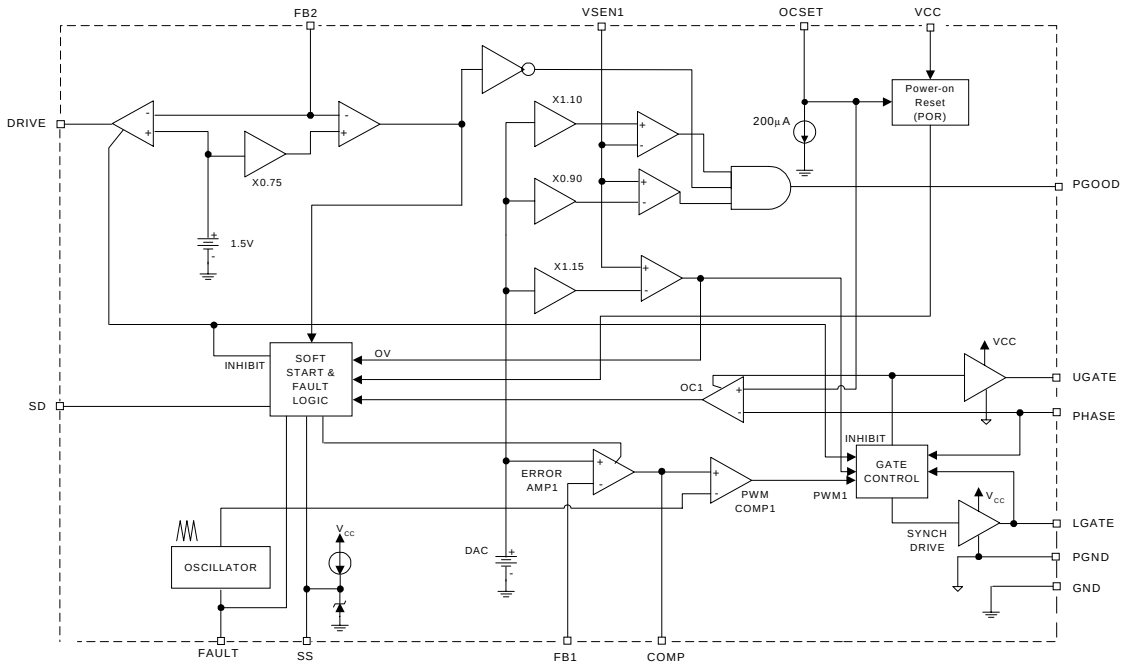
Pin Description



Ordering and Marking Information

APW7045 □□ □□-□□ Handling Code Temp. Range Package Code Voltage Code	Voltage Code 10 : 1.0V Package Code K : SOP - 16 (150mil) N : SSOP-16 Temp. Range C : 0 to 70° C Handling Code TU : Tube TR : Tape & Reel
APW7045 K/N : APW7045 XXXXX	XXXXX - Date Code

Block Diagram



Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
V_{CC}	Supply Voltage	15	V
V_I , V_O	Input , Output or I/O Voltage	GND -0.3 V to V_{CC} +0.3	V
T_A	Operating Ambient Temperature Range	0 to 70	°C
T_J	Junction Temperature Range	0 to 125	°C
T_{STG}	Storage Temperature Range	-65 to +150	°C
T_S	Soldering Temperature	300 ,10 seconds	°C

Thermal Characteristics

Symbol	Parameter	Value	Unit
θ_{JA}	Thermal Resistance in Free Air SOIC SOIC (with 3in^2 of Copper)	 75 65	°C/W

Electrical Characteristics

(Recommended operating conditions , Unless otherwise noted) Refer to Block and Simplified Power System Diagrams , and Typical Application Schematic.

Symbol	Parameter	Test Conditions	APW7045			Unit
			Min.	Typ.	Max.	
V_{CC} Supply Current						
I_{CC}	Nominal Supply Current	UGATE, LGATE, DRIVE open		4		mA
Power-on Reset						
V_{CC}	Rising VCC Threshold	Vocset=4.5V			10.7	V
	Falling VCC Threshold	Vocset=4.5V	8.2			
V_{OCSET}	Rising V_{OCSET} Threshold			1.26		
V_{SD}	Shutdown Input High Voltage		2.0			V
	Shutdown Input Low Voltage				0.8	
Oscillator						
F_{OSC}	Free Running Frequency	Fault= Open	185	200	215	kHz
ΔV_{OSC}	Ramp Amplitude	Fault= Open		1.9		V_{P-P}

Electrical Characteristics (Cont.)

(Recommended operating conditions, Unless otherwise noted) Refer to Block and Simplified Power System Diagram, and Typical Application Schematic.

Symbol	Parameter	Test Conditions	APW7045			Unit
			Min.	Typ.	Max.	
DAC Reference Voltage						
V_{DAC}	Reference Voltage APW7045-10			1.00		V
	Reference Voltage accuracy		-1.0		+1.0	%
Linear Regulator						
	Reference Voltage			1.5		V
	Regulation			3		%
	Output Drive Current	V_{DRIVE}=4V	20	40		mA
Synchronous PWM Controller Error Amplifier						
	DC Gain			88		dB
GBWP	Gain-Bandwidth Product			15		MHz
SR	Slew Rate	COMP=10pF		6		V/µs
PWM Controller Gate Driver						
I_{UGATE}	UGATE Source	V_{CC}=12V, V_{UGATE} =6V		1		A
R_{UGATE}	UGATE Sink	V_{UGATE1} =1V		2.1	3.5	Ω
I_{LGATE}	LGATE Source	V_{CC}=12V, V_{LGATE} =1V		1		A
R_{LGATE}	LGATE Sink	V_{LGATE}= 1V		1.6	3	Ω
Protection						
	VSEN1 Over-Voltage	VSEN1 Rising		115	120	%
	VSEN1 Over-Voltage Hysteresis			2		%
I_{OCSET}	OCSET Current Source	V_{OCSET}= 4.5V	170	200	230	µA
I_{SS}	Soft Start Current			28		µA
Power Good						
	VSEN1 Upper Threshold	VSEN1 Rising		109		%
	VSEN1 Under Voltage	VSEN1 Rising		93		%
	VSEN1 Hysteresis	Upper /Lower Threshold		2		%
V_{PGOOD}	PGOOD Voltage Low	I_{PGOOD}= -4mA		0.2	0.8	V

Functional Pin Description

VCC (Pin 1)

Provide a 12V bias supply for the IC to this pin. This pin also provides the gate bias charge for all the MOSFETs controlled by the IC. The voltage at this pin is monitored for Power-On Reset (POR) purposes.

DRIVE (Pin 2)

Connect this pin to the gate of an external MOSFET. This pin provides the drive for the V_{MEM} regulator's pass transistor.

Functional Pin Description (Cont.)

PGOOD (Pin 3)

PGOOD is an open collector output used to indicate the status of the output voltages. This pin is pulled low when the synchronous regulator output is not within ±10% of the DAC reference voltage or linear regulator output is below under-voltage threshold.

SD (Pin 4)

The pin shuts down all the outputs. A TLL-compatible , logic level high signal applied at this pin immediately discharges the soft-start capacitor , disabling all the outputs . Left open , this pin is pulled low by an internal pull-down resistor , enabling operation.

FB2 (Pin 5)

Connect this pin to a resistor divider to set the linear regulator output voltage (V_{MEM}). The output voltage set by the resistor divider is determined using the following formula :

$$V_{MEM} = 1.5V \times (1 + \frac{R_{OUT}}{R_{GND}})$$

Where R_{OUT} is the resistor connected from V_{MEM} to FB2, and R_{GND} is the resistor connected from FB2 to ground. The voltage at this pin is also monitored for Under-Voltage protection.

SS (Pin 6)

Connect a capacitor from this pin to ground. This capacitor , along with an internal 28uA current source , sets the soft-start interval of the converter.

FAULT (Pin 7)

This pin provides oscillator switching frequency adjustment, referring to the typical performence. By placing a resistor (RT, kΩ) from this pin to GND, the nominal 200kHz switching frequency is increased according to the following equation :

$$Fs = 200 + \frac{4000}{RT} \times (1.16 \frac{1.4}{RT-1}) \text{ (kHz)}$$

(R_T to GND, $R_T \geq 10k\Omega$ is more accurate)
Conversely, connecting a resistor from this pin to +12V reduces the switching frequency according to the following equation :

$$Fs = 200 + \frac{47920}{R_T} \text{ (kHz)}$$

(R_T to 12V, $R_T \geq 250\ k\Omega$ is more accurate)
Nominally, the voltage at this pin is 1.26V. In the event of an over-voltage or over-current condition, this pin is internally pulled to VCC.

GND (Pin 8)

Signal ground for the IC. All voltage levels are measured with respect to this pin.

COMP and FB1 (Pin 9, and 10)

COMP and FB1 are the available external pins of the PWM converter error amplifier. The FB1 pin is the inverting input of the error amplifier. Similarly , the COMP pin is the error amplifier output. These pins are used to compensate the voltage-mode control feedback loop of the synchronous PWM converter.

VSEN1 (Pin 11)

This pin is connected to the PWM converter's output voltage. The PGOOD and OVP comparator circuits use this signal to report output voltage status and for over- voltage protection.

OCSET (Pin 12)

Connect a resistor (R_{OCSET}) from this pin to the drain of PWM converter's upper MOSFET. R_{OCSET}, an internal 200μA current source (I_{OCSET}), and the MOSFET's on-resistance($R_{DS(ON)}$) set the converter's over-current (OC) trip point according to the following equation:

$$I_{PEAK} = \frac{I_{OCSET} \times R_{OCSET}}{R_{DS(ON)}}$$

Functional Pin Description (Cont.)

OCSET (Pin 12)

An over-current trip cycles the soft-start function. The voltage at this pin is monitored for Power-On Reset (POR) purpose and pulling this pin low with an open drain device will shutdown the IC.

PGND (Pin 13)

This is the power ground connection. Tie the synchronous PWM converter's lower MOSFET source to this pin.

LGATE (Pin 14)

Connect LGATE to the PWM converter's lower MOSFET gate. This pin provides the gate drive for the lower MOSFET.

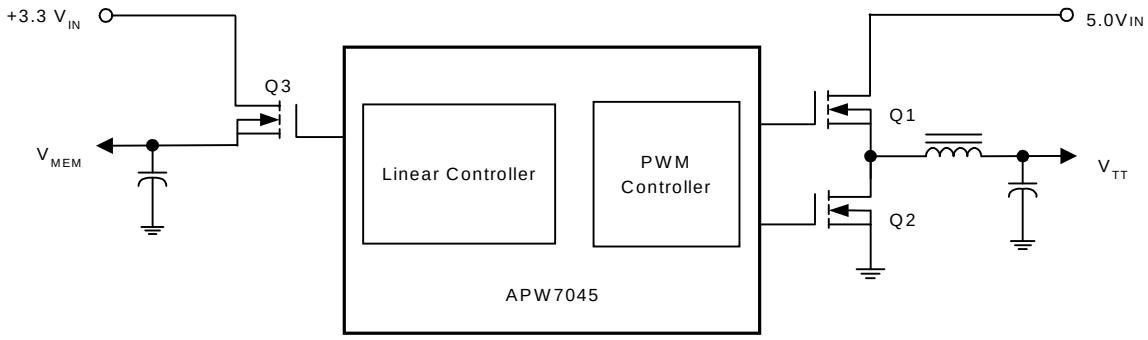
PHASE (Pin 15)

Connect the PHASE pin to the PWM converter's upper MOSFET source. This pin is used to monitor the voltage drop across the upper MOSFET for over-current protection.

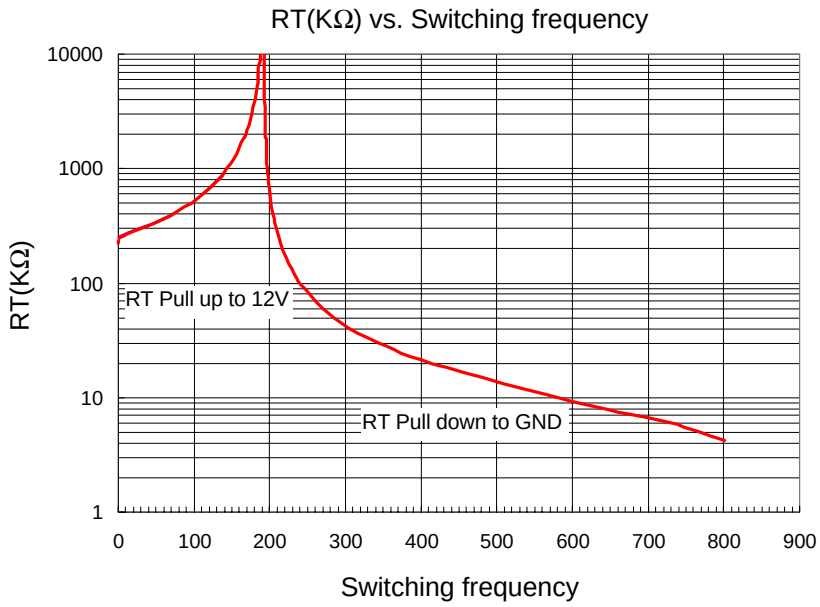
UGATE (Pin 16)

Connect UGATE pin to the PWM converter's upper MOSFET gate. This pin provides the gate drive for the upper MOSFET.

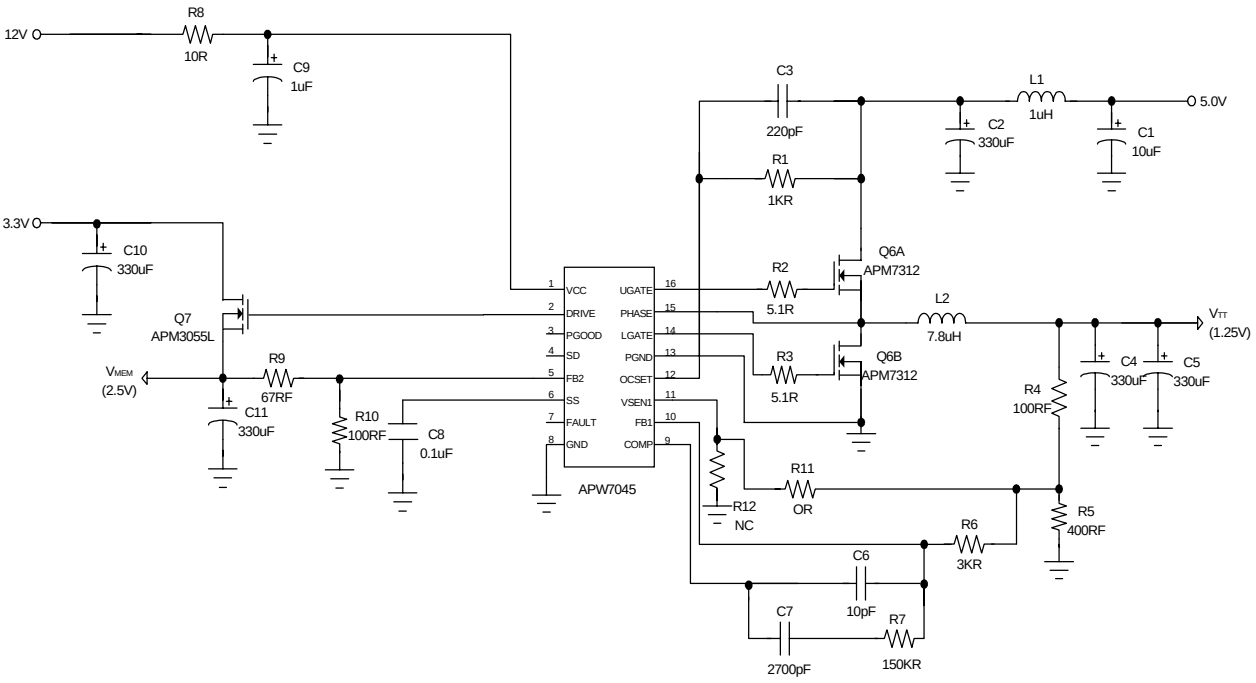
Simplified Power System Diagram



Typical Performance Curve

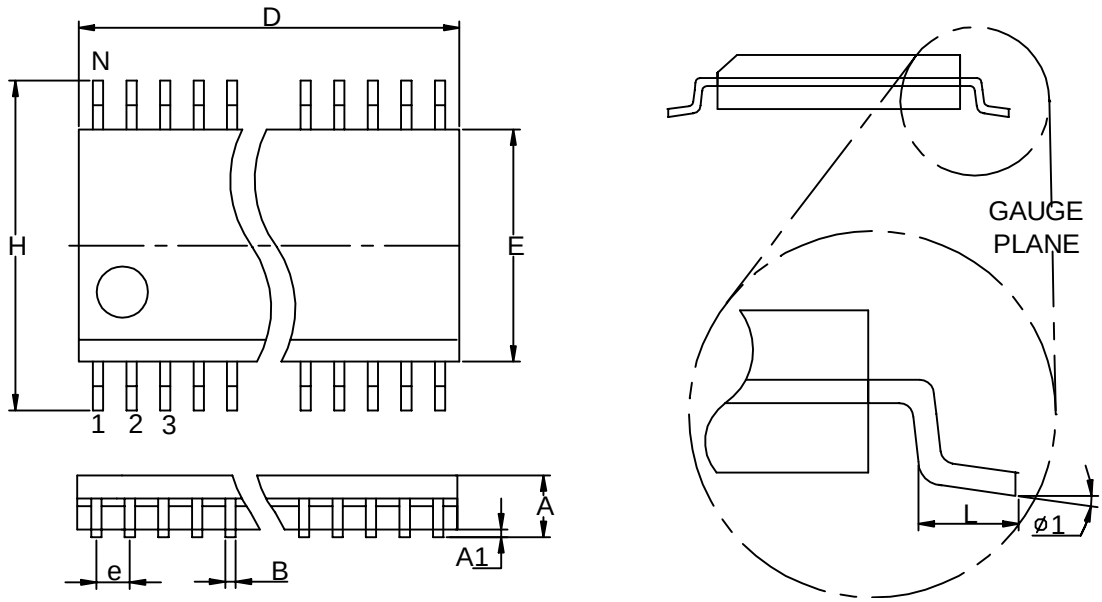


Typical Application Circuit



Package Informaion

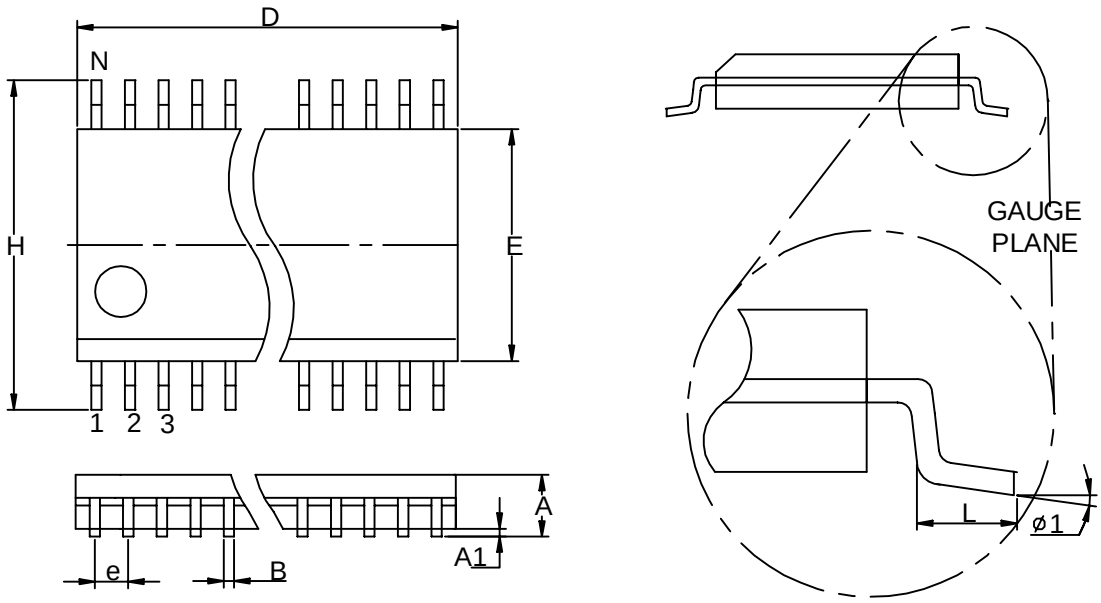
SOP-16 (150mil)



Dim	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	0.313	0.407	0.053	0.069
A1	0.024	0.059	0.004	0.010
B	0.094 typ.		0.016typ.	
D	2.279	2.327	0.386	0.394
E	0.886	0.927	0.150	0.157
e	0.295typ.		0.050typ.	
H	0.165	1.441	0.028	0.244
L	0.094	0.295	0.016	0.050
N	See variations		See variations	
ϕ1	0°	8°	0°	8°

Package Informaion

SSOP-16



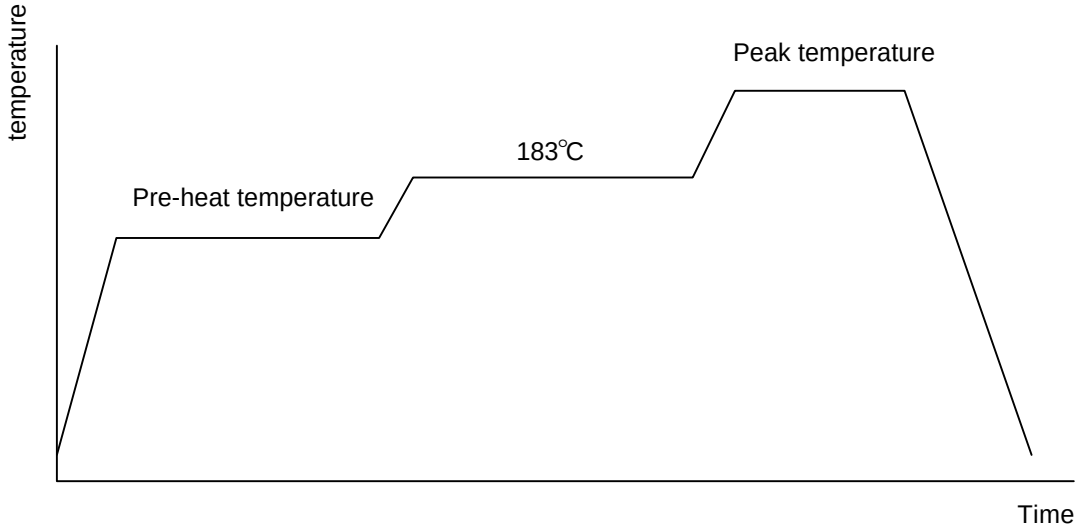
Dim	Millimeters		Variations- D			Dim	Inches		Variations- D		
	Min.	Max.	Variations	Min.	Max.		Min.	Max.	Variations	Min.	Max.
A	1.350	1.75	SSOP-16	4.75	5.05	A	0.053	0.069	SSOP-16	0.187	0.199
A1	0.10	0.25				A1	0.004	0.010			
B	0.20	0.30				B	0.008	0.012			
D	See variations					D	See variations				
E	3.75	4.05				E	0.147	0.160			
e	0.625 TYP.					e	0.025 TYP.				
H	5.75	6.25				H	0.226	0.246			
L	0.4	1.27				L	0.016	0.050			
N	See variations					N	See variations				
ϕ 1	0°	8°				ϕ 1	0°	8°			

Physical Specifications

Terminal Material	Solder-Plated Copper (Solder Material : 90/10 or 63/37 SnPb)
Lead Solderability	Meets EIA Specification RSI86-91, ANSI/J-STD-002 Category 3.

Reflow Condition (IR/Convection or VPR Reflow)

Reference JEDEC Standard J-STD-020A APRIL 1999



Classification Reflow Profiles

	Convection or IR/ Convection	VPR
Average ramp-up rate(183°C to Peak)	3°C/second max.	10 °C /second max.
Preheat temperature 125 ± 25°C)	120 seconds max	
Temperature maintained above 183°C	60 – 150 seconds	
Time within 5°C of actual peak temperature	10 –20 seconds	60 seconds
Peak temperature range	220 +5/-0°C or 235 +5/-0°C	215-219°C or 235 +5/-0°C
Ramp-down rate	6 °C /second max.	10 °C /second max.
Time 25°C to peak temperature	6 minutes max.	

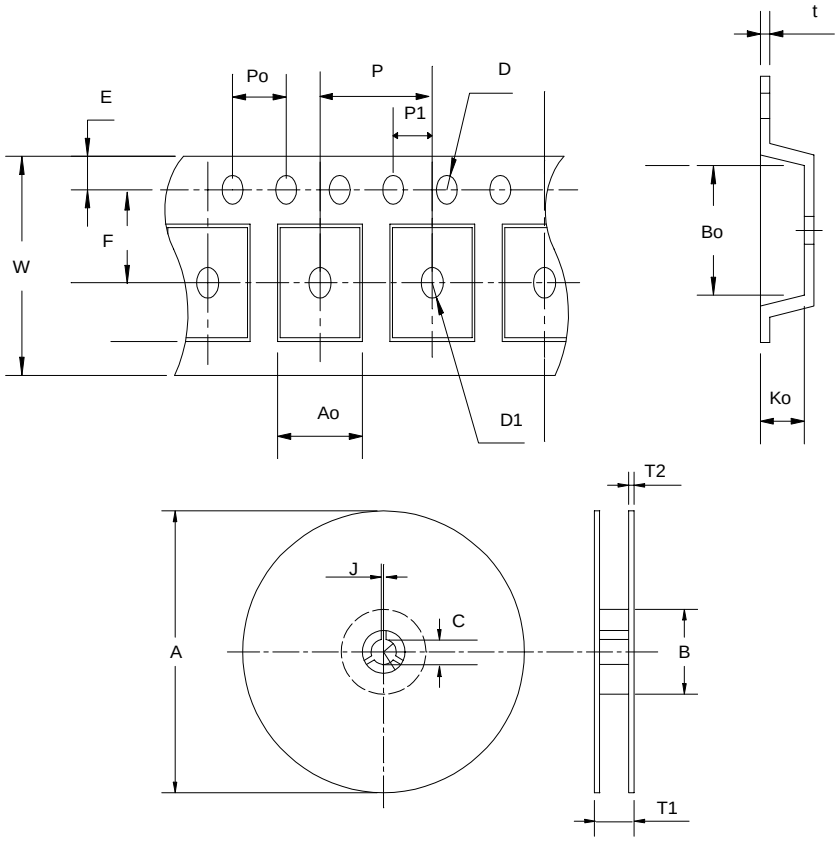
Package Reflow Conditions

pkg. thickness ≥ 2.5mm and all bgas	**pkg. thickness < 2.5mm and pkg. volume ≥ 350 mm³**	**pkg. thickness < 2.5mm and pkg. volume < 350mm³**
Convection 220 +5/-0 °C		Convection 235 +5/-0 °C
VPR 215-219 °C		VPR 235 +5/-0 °C
IR/Convection 220 +5/-0 °C		IR/Convection 235 +5/-0 °C

Reliability test program

Test item	Method	Description
SOLDERABILITY	MIL-STD-883D-2003	245°C , 5 SEC
HOLT	MIL-STD-883D-1005.7	1000 Hrs Bias @ 125 °C
PCT	JESD-22-B, A102	168 Hrs, 100 % RH , 121°C
TST	MIL-STD-883D-1011.9	-65°C ~ 150°C, 200 Cycles
ESD	MIL-STD-883D-3015.7	VHBM > 2KV, VMM > 200V
Latch-Up	JESD 78	10ms , I_{tr} > 100mA

Carrier Tape & Reel Dimensions



Application	A	B	C	J	T1	T2	W	P	E
SOP- 16 (150mil)	330 ± 3	100 + 2	13 + 0.5	2 ± 0.5	16.4 + 0.3 - 0.2	2.5 ± 0.5	16 ± 0.3	8.0 ± 0.1	1.75 ± 0.1
	F	D	D1	Po	P1	Ao	Bo	Ko	t
	7.5 ± 0.1	1.5 + 0.1	1.5 + 0.25	4.0 ± 0.1	2.0 ± 0.1	6.5 ± 0.1	10.3 ± 0. 1	2.1 ± 0.1	0.3 ± 0.05
Application	A	B	D0	D1	E	F	P0	P1	P2
SSOP-16	6.95	5.4	1.55±0.05	1.55±0.1	1.75±0.1	5.5±0.05	4.0±0.1	8.0±0.1	2.0±0.05
	T	T2	W	W1	C1	C2	T1	T2	C
	0.3±0.05	2.2	12.0±0.3	9.5	13±0.3	21±0.8	13.5±0.5	2.0±0.2	80±1

(mm)

Cover Tape Dimensions

Application	Carrier Width	Cover Tape Width	Devices Per Reel
SOP- 16	24	21.3	1000
SSOP-16	16.8	12.3	2500

Customer Service

Anpec Electronics Corp.
Head Office :
5F, No. 2 Li-Hsin Road, SBIP,
Hsin-Chu, Taiwan, R.O.C.
Tel : 886-3-5642000
Fax : 886-3-5642050

Taipei Branch :
7F, No. 137, Lane 235, Pac Chiao Rd.,
Hsin Tien City, Taipei Hsien, Taiwan, R. O. C.
Tel : 886-2-89191368
Fax : 886-2-89191369