ARA2000S23

CATV Reverse Amplifier with Step Attenuator
Advanced Product Information

Rev. 2

FEATURES

- Low cost integrated monolithic GaAs amplifier with step attenuator.
- Attenuation Range: 0 – 58 dB, variable in 1 dB steps via 16 bit serial input.
- Meets DOCSIS distortion requirements at +60 dBmV
- Low distortion & Low noise figure
- Frequency range: 5 – 100 MHz
- 5 Volt operation
- Programmable address allows multiple parts to share 3 wire bus

APPLICATIONS

- MCNS/DOCSIS Compliant Cable Modems
- CATV Interactive Set-Top Box
- Telephony over Cable Systems
- Open Cable Set-Top Box

S23
28 PIN SSOP PACKAGE

Description

The ARA2000S23 is a GaAs IC designed to provide the reverse path amplification and output level control functions in a CATV Set-Top Box or Cable Modem. It incorporates a digitally controlled precision step attenuator that is preceded by an ultra low noise amplifier stage, and followed by an ultra-linear output driver amplifier. This part is a balanced design that meets or exceeds the MCNS/DOCSIS requirement for harmonic performance @ +60dBmV output levels while only requiring a single polarity +5V supply. Both the input and output are matched to 75 ohms. The precision attenuator provides up to 58 dB of attenuation in 1 dB increments. The ARA2000S23 is supplied in a 28-pin SSOP package featuring a thermal heat slug on the bottom of the package. Soldering this heat slug to the ground plane of the PC board ensures the lowest possible thermal resistance for the device resulting in a long MTF.

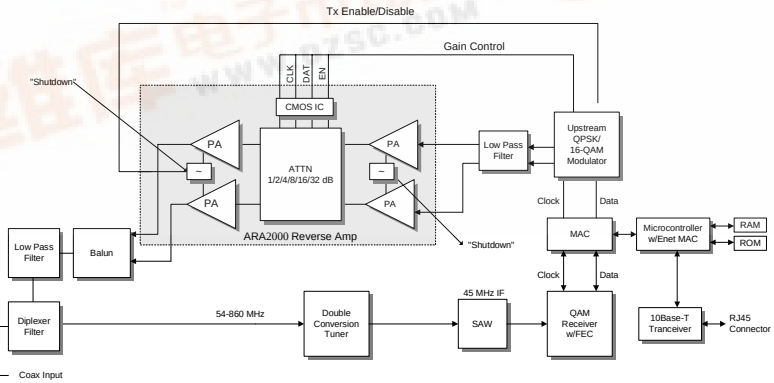


Figure 1: Cable Modem or Interactive Set-Top Box Block Diagram

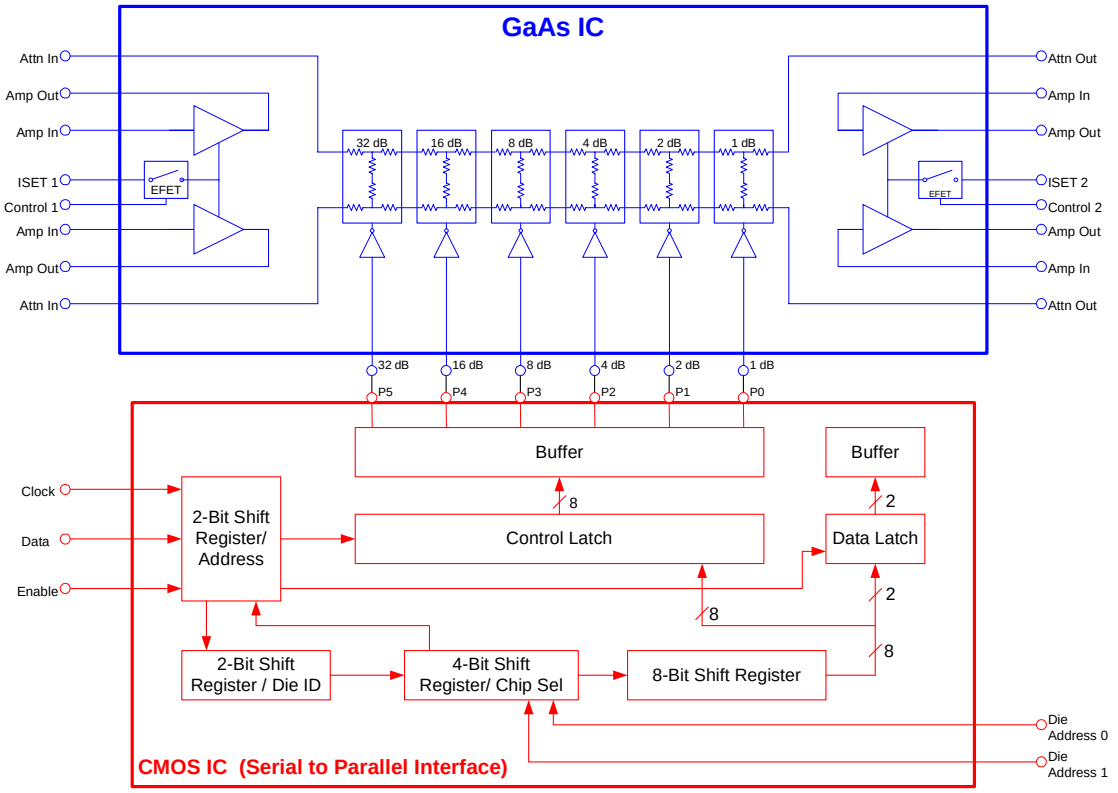


Figure 2: ARA 2000 Block Diagram

ABSOLUTE MAXIMUM RATINGS		
PARAMETER	**PARAMETER**	
V_{DD} (PINS 2,4,9,21,24)	9	VDC
V_{RFIN} (PINS 5,8)	0 to -3	VDC
ATT_{IN} (3,10) ATT_{OUT} (19,26)V	5	VDC
I_{SET} (PINS 7, 22)	2	VDC
RF Input Voltage (PINS 5,8)*	+ 60	dBmV
Storage Temperature	- 55 to +200	°C
Soldering Temperature	260	°C
Soldering Time	5	Sec
Operating Case Temperature	0 to + 85	°C

ELECTRICAL CHARACTERISTICS (TYPICAL) (V_{DD}=5 V_{DC}, Tc=25 °C)

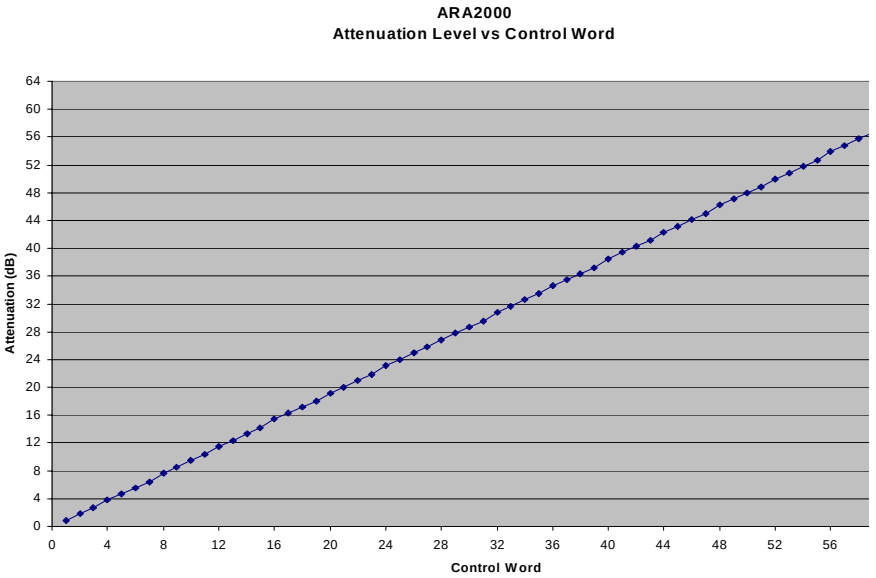
PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
Gain [1] @ 10 MHz	27.5	29.3	30.5	dB	At 0dB attenuation setting
Gain Flatness [1]	-	0.75	-	dB	5 to 42 MHz
Gain Variation Over Temp	-	-0.006	-	dB/°c	
Attenuation Steps [1] 1 dB 2 dB 4 dB 8 dB 16 dB 32 dB	0.65 1.6 3.6 7.5 15.0 30.2	0.83 1.70 3.75 7.75 15.40 30.75	1.00 2.05 4.0 8.0 15.8 31.3	dB	
2nd Harmonic Distortion Level [2] 10 MHz	-	-75	-53	dBc	at +60 dBmV
3rd Harmonic Distortion Level [2] 10 MHz	-	-60	-53	dBc	at +60 dBmV
3rd Order Output Intercept Point	78	-	-	dBmV	
1 dB Gain Compression Point	-	68.5	-	dBmV	
Noise Figure[1]	-	3.0	4.0	dB	Includes input balun loss
Ouput Noise Power Active/No Signal/Min Attn. Setting Active/No Signal/Max Attn. Setting	 - -	 - -	 -25.5 -40.8	dBmV	Any 3200 KHz bandwidth from 5-42 MHz
Isolation in Tx disable mode @ 45 MHz	-	65	-	dB	Difference in output signal level between Tx enable / disable
Input Impedance[1]	-	75	-	ohm	
Input Return Loss[1]	-	-20	-12	dB	Tx enabled
Input Return Loss [1]	-	-5	-	dB	Tx disabled
Output Impedance[1]	-	75	-	ohm	
Output Return Loss[1]	-	-17	-12	dB	Tx enabled
Output Return Loss[1]	-	-15	-10	dB	Tx disabled
V_{DD1}, V_{DD2} (Pins 4, 9, 21, 24)	-	5	7	V	
V_{DD} Digital (Pin 2)	-	5	-	V	
V_{DD} CMOS (Pin 11)	3	-	5	V	
I_{DD1} (Input Amp) (Pins 4 and 9)	-	48	80	mA	Tx enabled

ELECTRICAL CHARACTERISTICS (TYPICAL) (V_{DD}=5 V_{DC}, T_C=25 °C) (Continued)

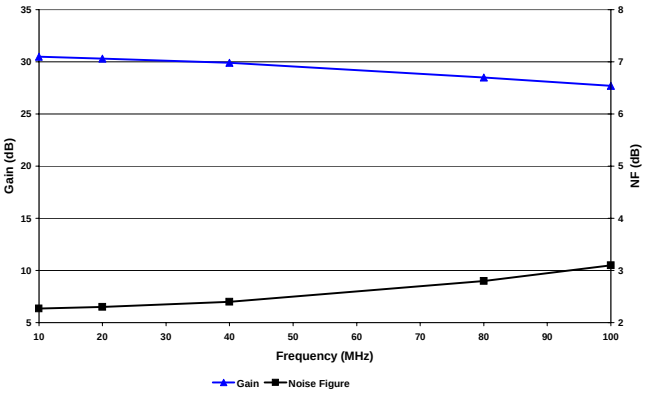
PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
I_{DD1}	-	2.4	6	mA	Tx disabled
I_{DD2} (Output Amp) (Pins 21 and 24)	-	77	120	mA	Tx enabled
I_{DD2}	-	3.7	9	mA	Tx disabled
I_{DD} Digital (Attenuator) (Pin 2)	-	9	15	mA	
Power Consumption	-	0.67	1.08	W	Tx enabled
Power Consumption	-	75	150	mW	Tx disabled
Attenuator Step Size	0.6	-	1.4	dB	
Gain Flatness [1]	-	1.5	-	dB	5 - 65 MHz
Output Voltage Transient [1] Tx enable/disable	- -	- 4	100 7	mVp-p -	At 0 db Attenuator Setting At 24 db Attenuator Setting
Maximum Attenuation	58.6	60.3			

Notes:

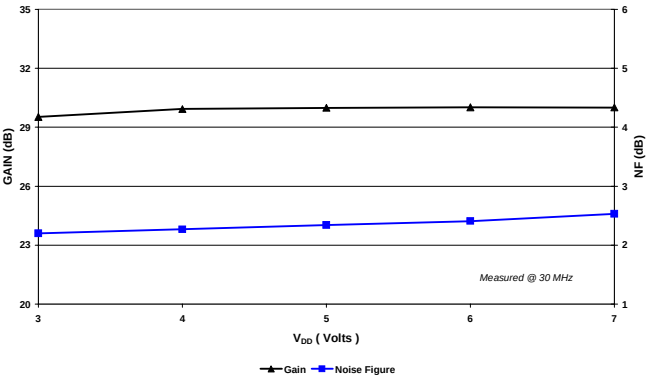
1. As measured in ANADIGICS test fixture
2. At +60 dBmV output level into 75 ohm load



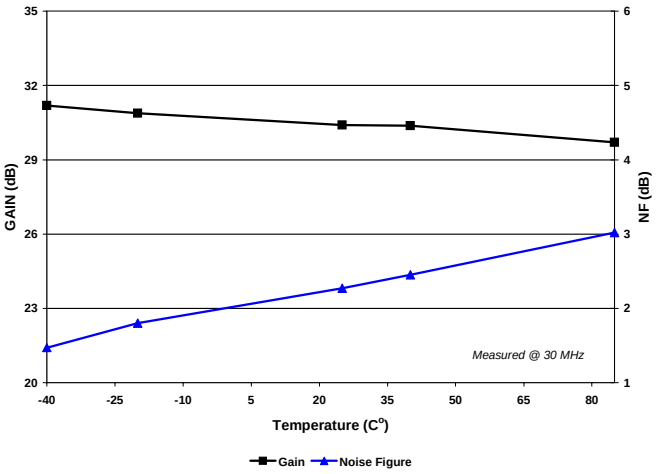
Gain & Noise Figure vs Frequency



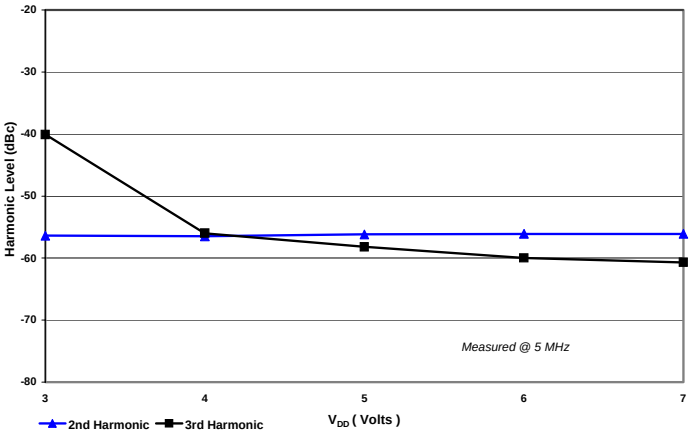
Gain & Noise Figure vs V_{DD}



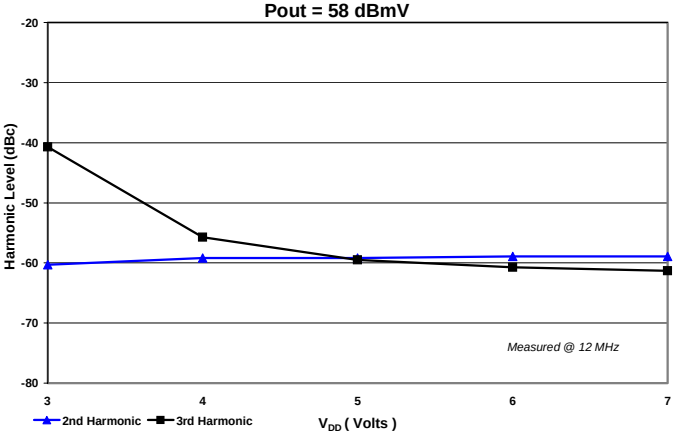
GAIN & Noise Figure vs Temperature



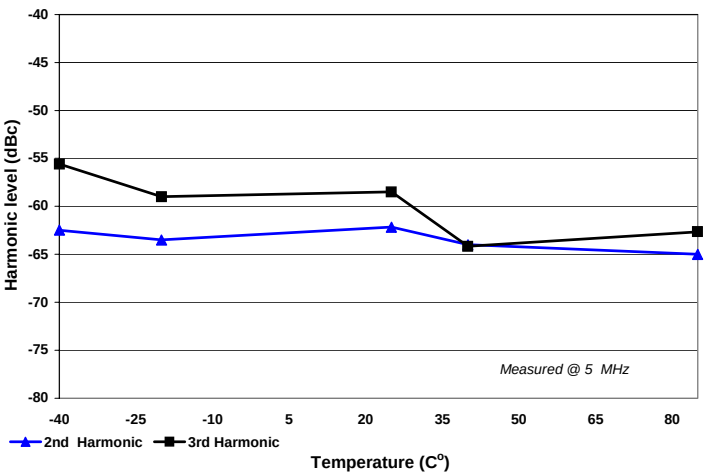
Harmonic Distortion vs V_{DD}
Pout = 58 dBmV

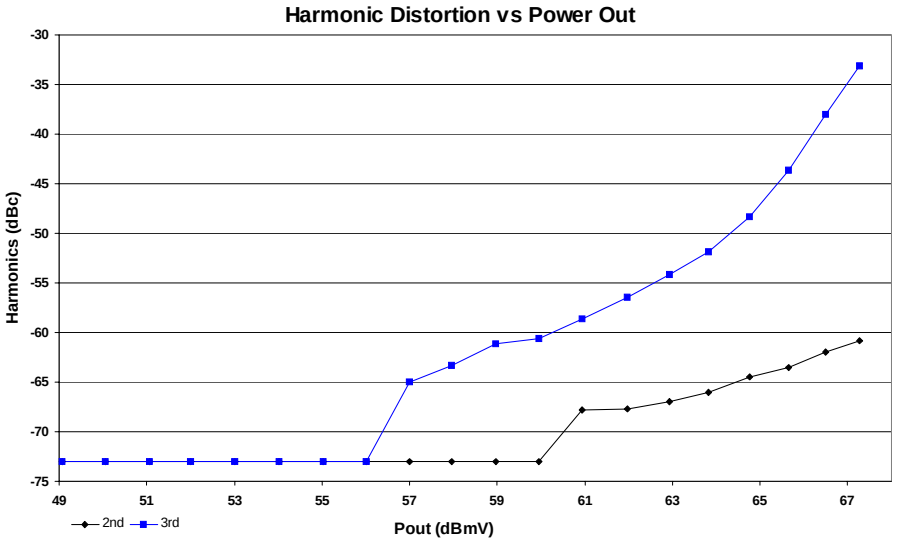


Harmonic Distortion vs V_{DD}
Pout = 58 dBmV



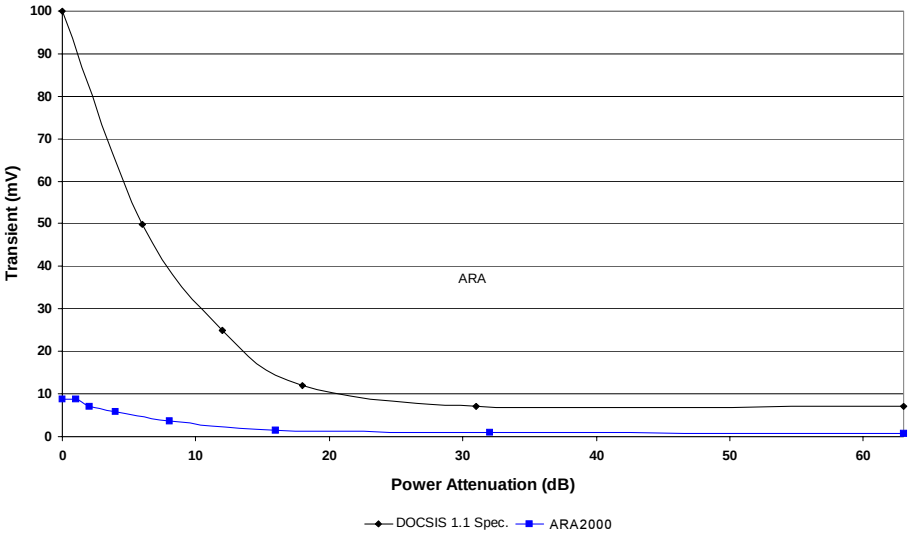
Harmonic Distortion vs Temperature
Pout = 58 dBmV



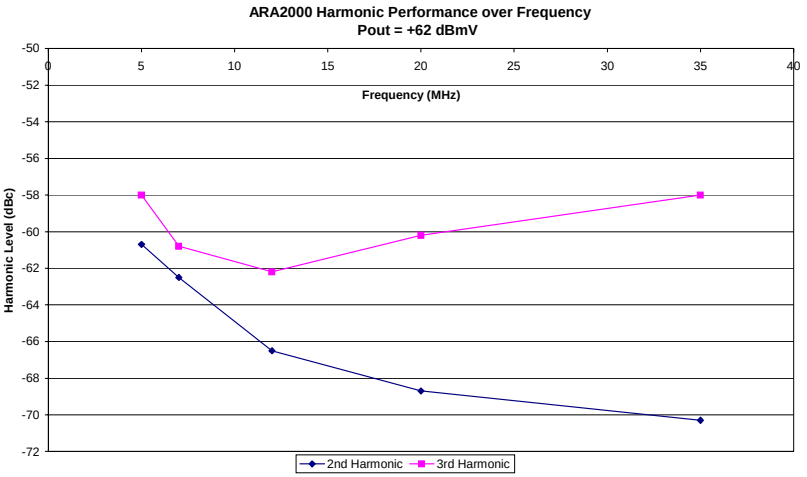


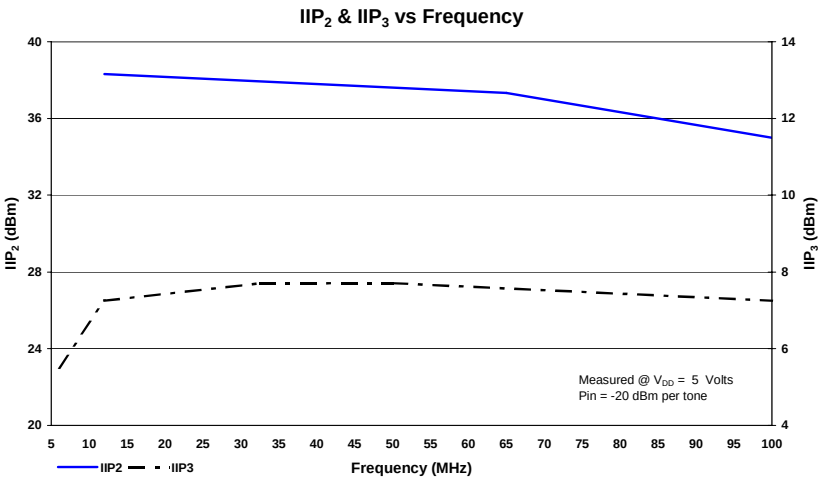
Transients vs Attenuation

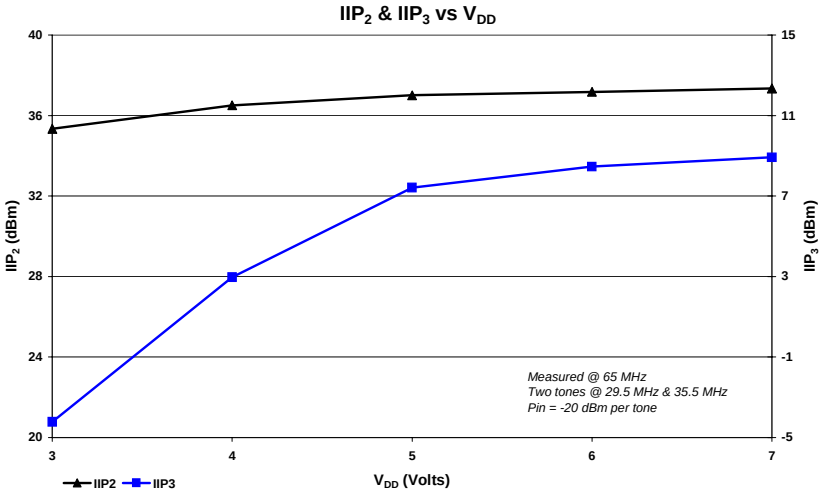
P_{out} = 55 dBmV at 0dB attenuation.



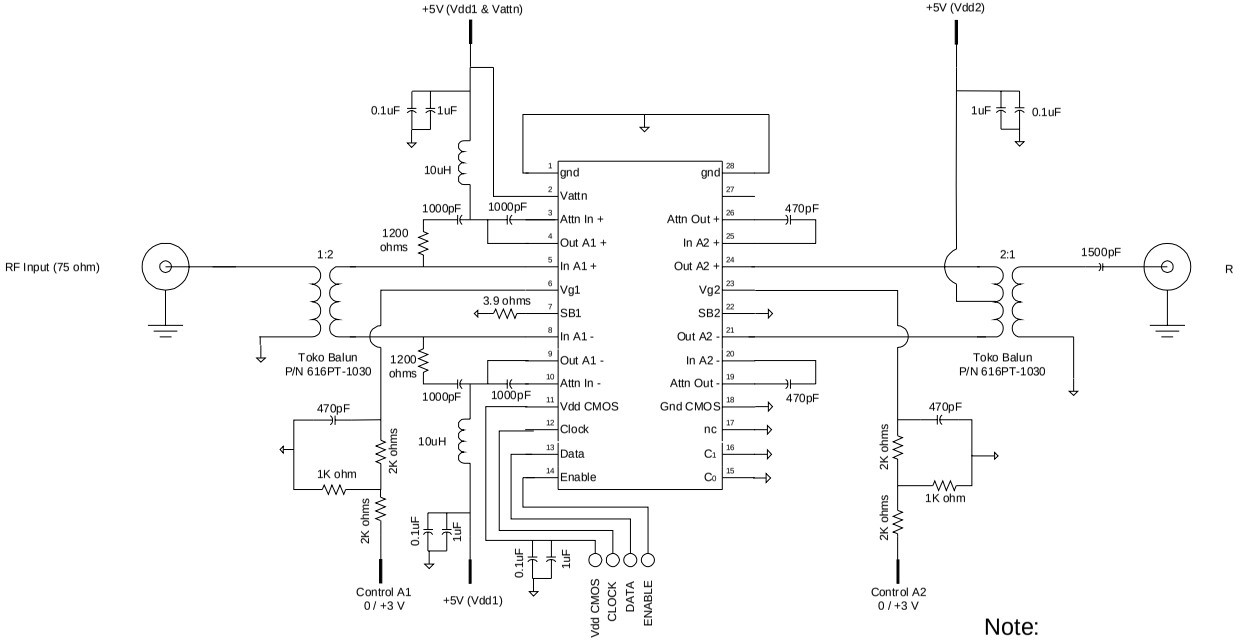
ARA2000S23


ARA2000 Harmonic Performance over Frequency
Pout = +62 dBmV
Frequency (MHz)
Harmonic Level (dBc)
2nd Harmonic
3rd Harmonic


IIP2 & IIP3 vs Frequency
IIP2 (dBm)
IIP3 (dBm)
Measured @ VDD = 5 Volts
Pin = -20 dBm per tone
IIP2
IIP3
Frequency (MHz)


IIP2 & IIP3 vs VDD
IIP2 (dBm)
IIP3 (dBm)
Measured @ 65 MHz
Two tones @ 29.5 MHz & 35.5 MHz
Pin = -20 dBm per tone
IIP2
IIP3
VDD (Volts)

ARA2000 & 2001
Balanced Reverse Amp Test Fixture with 3 Wire Interface



Note:

Tx Enable = Control
Tx Disable = Control

TEST CIRCUIT

ARA2000S23

Programming Word

D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	D_8	D_9	D_{10}	D_{11}	D_{12}	D_{13}	D_{14}	D_{15}
A0	A1	C0	C1	CS0	CS1	CS2	CS3	P0/D0	P1/D1	P2	P3	P4	P5	P6	P7

Register Address

A0	A1	REGISTER
0	0	Data Port
0	1	N/A
1	0	N/A
1	1	Parallel Port

Chip Select

CS0	CS1	CS2	CS3	APPLICATION
1	0	0	0	Serial-Parallel Interface
All Other Combinations				N/A

Die Address

C0 C1		External Die Connection			
		00	01	10	11
Serial Data Input	00	■			
	01		■		
	10			■	
	11				■

■ Indicates Device is Selected

Data Port Description

SERIAL DATA	FUNCTION
P0/D0	1 dB Attenuator Bit / External Data Port 0
P1/D1	2 dB Attenuator Bit / External Data Port 1
P2	4 dB Attenuator Bit
P3	8 dB Attenuator Bit
P4	16 dB Attenuator Bit
P5	32 dB Attenuator Bit
P6	N/A
P7	N/A

Figure 3

SERIAL DATA INPUT TIMING

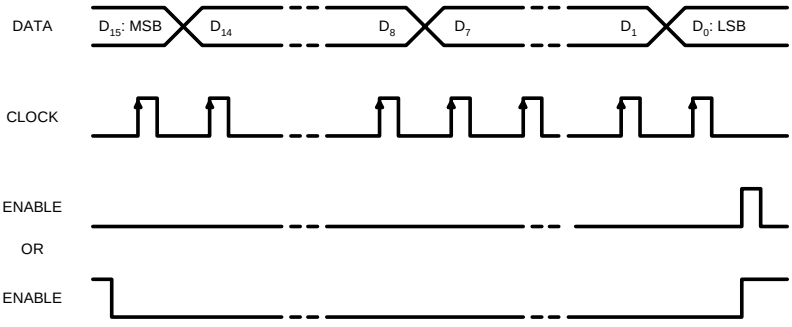
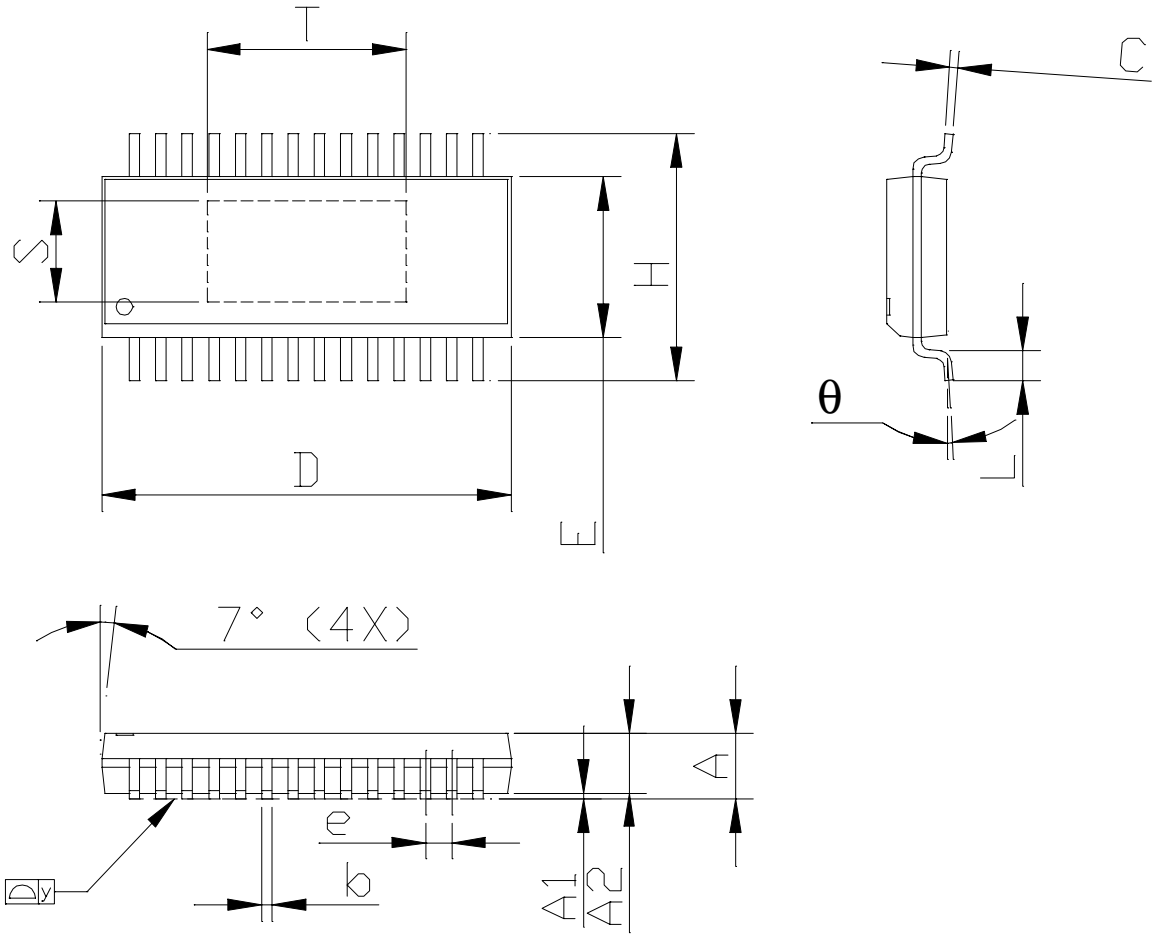


Figure 4

PIN DESCRIPTION		
Pin	**Function**	**Description**
1	Ground	
2	V_{ATTN}	Supply for Attenuator
3	ATT_{IN} (+)	Attenuator Input (+)
4	$A1_{OUT}$ (+)	Amplifier 1 (+) Output
5	$A1_{IN}$ (+)	Amplifier 1 (+) Input
6	Vg1	Amplifier A1 (+/-) Control
7	I_{SET1}	Amplifier A1 (+/-) Current Adjust
8	$A1_{IN}$ (-)	Amplifier A1 (-) Input
9	$A1_{OUT}$ (-)	Amplifier A1 (-) Output
10	ATT_{IN} (-)	Attenuator Input (-)
11	CMOS	Supply For Digital CMOS Circuit
12	CLK	Clock
13	DAT	Data
14	En	Enable
15	C0	Die Address (see page 6)
16	C1	Die Address (see page 6)
17	N/C	No connection
18	CMOS	Ground for Digital CMOS Circuit
19	ATT_{OUT} (-)	Attenuator Output (-)
20	$A2_{IN}$ (-)	Amplifier A2 (-) Input
21	$A2_{OUT}$ (-)	Amplifier A2 (-) Output
22	I_{SET2}	Amplifier A2 (+/-) Current Adjust
23	Vg2	Amplifier A2 (+/-) Control
24	$A2_{OUT}$ (+)	Amplifier A2 (+) Output
25	$A2_{IN}$ (+)	Amplifier A2 (+) Input
26	ATT_{OUT} (+)	Attenuator Output (+)
27	N/C	No Connection
28	GND	Ground

Package Outline



SYMBOLS	DIMENSIONS IN INCHES		DIMENSIONS IN MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.057	0.061	1.45	1.55
A1	0.000	0.004	0.00	0.10
A2	0.057 (NOMINAL)		1.45 (NOMINAL)	
b	0.008	0.012	0.20	0.30
C	0.007	0.010	0.18	0.25
D	0.386	0.394	9.80	10.00
E	0.150	0.157	3.81	4.00
H	0.228	0.244	5.80	6.20
e	0.025 BSC		.64 BSC	
L	0.016	0.050	0.40	1.27
y	––	0.004	––	0.10
θ	0°	8°	0°	8°
T	––	0.190	––	4.82
S	––	0.096	––	2.43

NOTE
1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS
2. TOLERANCE 0.004in.[0.10 mm] UNLESS OTHERWISE SPECIFIED
3. CONTROLLING DIMENSION ARE INCHES.
4. REF. - MO-137

98000–031

Notes

Notes

Notes

ANADIGICS, Inc.
35 Technology Drive
Warren, New Jersey 07059
Tel: (908) 668-5000
Fax: (908) 668-5132

http://www.anadigics.com
Mktg@anadigics.com