

PHEMT GaAs IC SPDT Switch DC–2.5 GHz



AS169-73

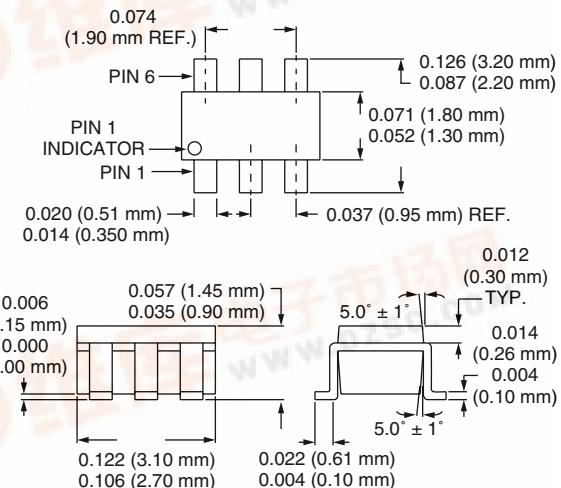
Features

- P₁ dB +30 dBm Typical @ +3 V
- IP3 52 dBm Typical
- Low Insertion Loss (0.3 dB @ 0.9 GHz)
- Low DC Power Consumption
- Ultra Miniature Low Cost SOT-6 Plastic Package
- PHEMT Process

Description

The AS169-73 is an IC FET SPDT switch in a low cost SOT-6 plastic package. The AS169-73 features low insertion loss and positive voltage operation with very low DC power consumption. This general purpose switch can be used in a variety of telecommunications applications.

SOT-6



Electrical Specifications at 25°C (0, +3 V)

Parameter ¹	Frequency ²	Min.	Typ.	Max.	Unit
Insertion Loss ³	DC–1.0 GHz DC–2.5 GHz		0.3 0.4	0.4 0.5	dB dB
Isolation	DC–1.0 GHz DC–2.5 GHz	22 21	25 24		dB dB
VSWR ⁴	DC–1.0 GHz DC–2.5 GHz		1.15:1 1.3:1	1.25:1 1.4:1	

Operating Characteristics at 25°C (0, +3 V)

Parameter	Condition	Frequency	Min.	Typ.	Max.	Unit
Switching Characteristics ⁵	Rise, Fall (10/90% or 90/10% RF) On, Off (50% CTL to 90/10% RF) Video Feedthru			10 20 25		ns ns mV
Input Power for 1 dB Compression	0/+3 V 0/+5 V	0.5–2.5 GHz 0.5–2.5 GHz		+30 +34		dBm dBm
Intermodulation Intercept Point (IP3)	For Two-tone Input Power +5 dBm 0/+3 V 0/+5 V	0.5–2.5 GHz 0.5–2.5 GHz		+43 +50		dBm dBm
Control Voltages	V _{Low} = 0 to 0.2 V @ 20 μA Max. V _{High} = +3 V @ 100 μA Max. to +5 V @ 200 μA Max.					

1. All measurements made in a 50 Ω system, unless otherwise specified.

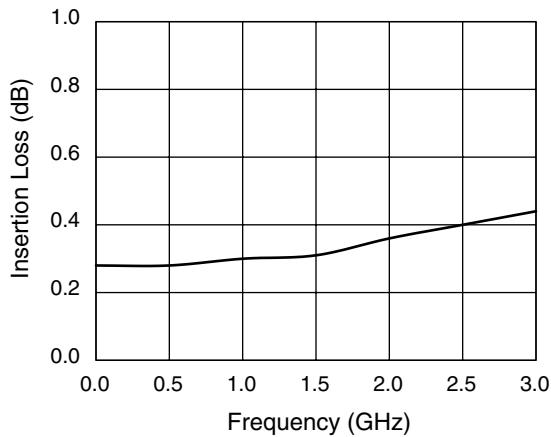
2. DC = 300 kHz.

3. Insertion loss changes by 0.003 dB/°C.

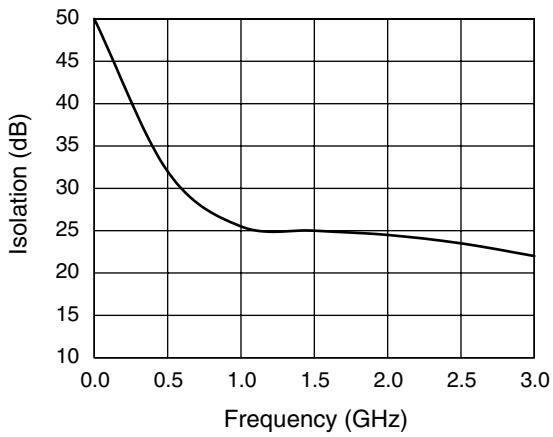
4. Insertion loss state.

5. Video feedthru measured with 1 ns risetime pulse and 500 MHz bandwidth.

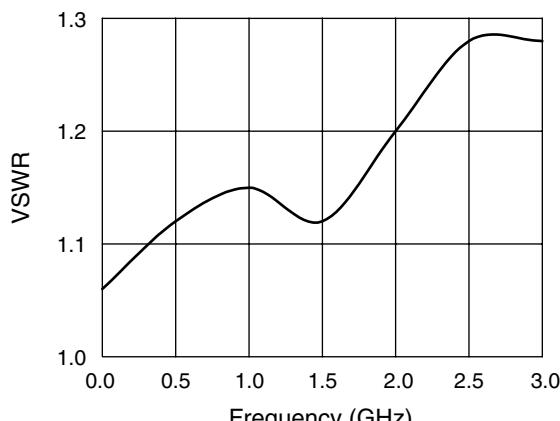
Typical Performance Data (0, +3 V)



Insertion Loss vs. Frequency



Isolation vs. Frequency

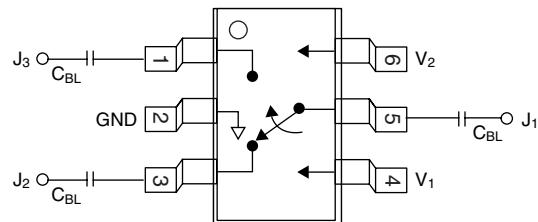


VSWR vs. Frequency

Absolute Maximum Ratings

Characteristic	Value
RF Input Power	6 W > 500 MHz 0/+7 V Control
Control Voltage	-0.2 V, +8 V
Operating Temperature	-40°C to +85°C
Storage Temperature	-65°C to +150°C
Θ_{JC}	25°C/W

Pin Out



DC blocking capacitors (C_{BL}) must be supplied externally for positive voltage operation.
 $C_{BL} = 100 \text{ pF}$ for operation $>500 \text{ MHz}$.

Truth Table

V₁	V₂	J₁-J₂	J₁-J₃
V _{High}	0	Isolation	Insertion Loss
0	V _{High}	Insertion Loss	Isolation

$V_{High} = +3 \text{ to } +5 \text{ V}$ ($V_S = V_{High} \pm 0.2 \text{ V}$).