

# **AS2214**

## Primary Side PWM Controller

#### **Features**

- Low Startup Current
- Bulk and AC sensing
- Soft Start
- Single-start or auto-restart modes
- Oscillator trimmed for precision duty cycle clamp
- Standard temperature range extended to 105°C
- Remote on / off control
- Buffered Ramp for slope compensation
- Standard current mode control

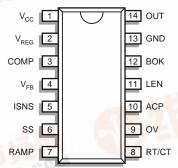
#### Description

The AS2214 is a full featured, pulse width modulation controller. Based on an improved AS3842, the AS2214 provides additional features that reduce component count and improve specifications in a wide range of power supply designs. The added functionality includes AC power and bulk voltage sensing, over-voltage input, as well as the ability to latch off or bounce through different fault conditions.

The PWM function is controlled by the current sense comparator for normal current mode control and a second comparator for voltage mode soft start. A buffered RAMP signal is available for slope compensation without loading the oscillator. The output stage is a high current totem pole output that sees only 85 ns delay from the PWM comparator.

The AS2214 requires less than 10µA of startup current. The undervoltage lockout (UVLO) thresholds are nominally 13.8V for turn on and 8 V for turn off. A precision 2.5 V bandgap reference serves as an input for the error amplifier. The oscillator discharge current is trimmed to provide guaranteed duty cycle clamping.

#### Pin Configuration — Top view

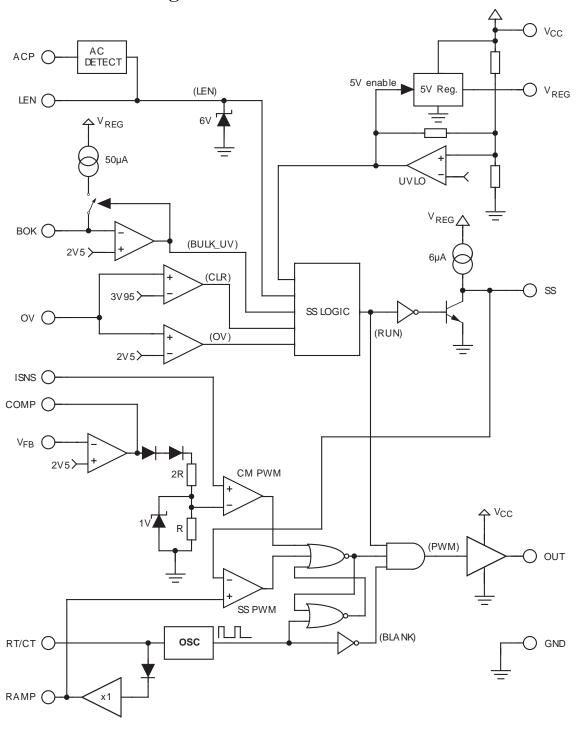


### Ordering Information

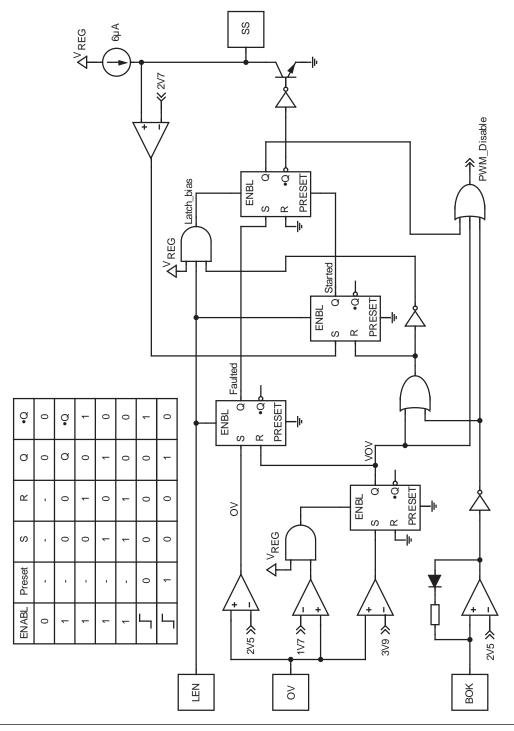
Package	Temperature Range	Order Code
14-Pin Plastic DIP	0 to 105° C	AS2214N



# Functional Block Diagram



AS2214 Soft Start Logic



# Pin Function Description

Pin Number	Function	Description
1	Vcc	Positive supply voltage for the IC.
2	$V_{REG}$	Output of 5V series regulator.
3	COMP	This pin is the error amplifier output. Typically used to provide loop compensation to maintain $V_{\text{FB}}$ at 2.5 V.
4	$V_{FB}$	Inverting input of the error amplifier. The non-inverting input is a trimmed 2.5 V bandgap reference.
5	ISNS	A voltage proportional to inductor current is connected to this pin. The PWM uses this information to terminate the gate drive of the output.
6	SS	This pin provides a 6µA current source to linearly charge an external capacitor. This pin is compared to the RAMP pin in the soft start comparator, terminating output pulses when RAMP goes above the SS voltage.
7	RAMP	This pin is a level-shifted and buffered oscillator signal used to provide slope compensation to the current sense signal. The pin also serves as the non-inverting input of the soft-start comparator.
8	RT/CT	Oscillator frequency and maximum duty cycle are set by connecting a resistor $(R_T)$ to VREG and a capacitor $(C_T)$ to ground.
9	OV	This pin latches SS low when pulled above 2.5 V. The latch can be reset by pulling OV above 4 V then back to ground.
10	ACP	This pin detects the presence of AC signal and drives LEN high.
11	LEN	This pin must be high to enable starting. The pin can also clear all latches by going low then high.
12	вок	This pin monitors the bulk voltage through a resistor divider and, when BOK exceeds 2.5 V, provides a 50µA current source for hysteresis. When BOK drops below 2.5V, SS is pulled low and the hysteresis current is turned off. Auto-restart after a brown-out is possible.
13	GND	Circuit common ground.
14	OUT	This totem pole output is designed to directly drive a power MOSFET switch capable of sourcing and sinking peak currents up to 1 A.

#### **Absolute Maximum Ratings**

Parameter	Symbol	Rating	Unit
Reference Current	I <sub>REF</sub>	200	mA
Output Current	louт	1	А
Supply Voltage	V <sub>CC</sub>	20	V
Output Voltage	V <sub>OUT</sub>	20	V
Continuous Power Dissipation at 25° C	P <sub>D</sub>	500	mW
Junction Temperature	TJ	150	°C
Storage Temperature Range	T <sub>STG</sub>	-65 to 150	°C
Lead Temperature, Soldering 10 Seconds	TL	300	°C

Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

#### **Recommended Conditions**

Parameter	Symbol	Rating	Unit
Supply Voltage	Vcc	10 - 15	V
Oscillator	Fosc	50 - 250	kHz

## Typical Thermal Resistance

Package	$\theta_{JA}$	$\theta$ JC	<b>Typical Derating</b>
14L PDIP	85° C/W	40° C/W	11.7 mW/°C

#### **Electrical Characteristics**

Electrical Characteristics are guaranteed over full junction temperature range (0 to 105° C). Ambient temperature must be derated based on power dissipation and package thermal characteristics. Unless otherwise specified, the conditions of test are  $V_{CC} = 15 \text{ V}$ ; BOK = 3 V; OV = 0V;  $R_T = 680 \Omega$ ;  $C_T = 10 \text{ nF}$ . To override UVLO,  $V_{CC}$  should be raised above 18 V prior to test.

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Error Amplifier						
Input Voltage	V <sub>FB</sub>	T <sub>J</sub> = 25°C	2.465	2.500	2.535	V
Input Bias Current	I <sub>BIAS</sub>			-0.1	-1	μА
Voltage Gain	Avol	2 ≤ V <sub>COMP</sub> ≤ 4 V	65	90		dB
Transconductance	Gm			1		mA/mV
Unity Gain Bandwidth	GBW		0.8	1.2		MHz
Power Supply Rejection Ratio	PSRR	12 ≤ V <sub>CC</sub> ≤ 18 V	60	70		dB
Output Sink Current	I <sub>COMPL</sub>	V <sub>FB</sub> = 2.7 V; V <sub>COMP</sub> = 1.1 V	2	6		mA
Output Source Current	Ісомрн	V <sub>FB</sub> = 2.3 V; V <sub>COMP</sub> = 5 V	0.5	1.0		mA
Output Swing High	Ісомрн	$V_{FB}$ = 2.3 V; $R_L$ = 15 $\Omega$ to GND	5	5.5		V
Output Swing Low	I <sub>COMPL</sub>	$V_{FB}$ = 2.7 V; $R_L$ = 15 $\Omega$ to $V_{REG}$		0.7	1.1	V

## **AS2214**

#### Electrical Characteristics (cont'd)

Electrical Characteristics are guaranteed over full junction temperature range (0 to 105° C). Ambient temperature must be derated based on power dissipation and package thermal characteristics. Unless otherwise specified, the conditions of test are  $V_{CC}$  = 15 V; BOK = 3 V; OV = 0V;  $R_T$  = 680  $\Omega$ ;  $C_T$  = 10 nF. To override UVLO,  $V_{CC}$  should be raised above 18 V prior to test.

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
5 V Regulator						
Output Voltage	V <sub>REG</sub>	I <sub>REG</sub> = 1 mA, T <sub>J</sub> = 25° C	4.90	5.00	5.10	V
Line Regulation	PSRR	12 ≤ V <sub>CC</sub> ≤ 18 V		5	15	mV
Load Regulation		1≤ I <sub>REG</sub> ≤ 20mA		5	15	mV
Temperature Stability	TC <sub>REG</sub>			0.2	0.4	mV/°C
Total Output Variation		Line, Load,Temperature	4.85		5.15	V
Long-Term Stability		Over 1,000 hrs at 25°C		5	25	mV
Output Noise Voltage	V <sub>NOISE</sub>	10 ≤ f ≤ 100kHz, T <sub>J</sub> = 25°C		50		μV
Maximum Source Current	I <sub>MAX</sub>	V <sub>REG</sub> = 4.8 V	30	120	180	mA
Oscillator						
Initial Accuracy	Fosc	T <sub>J</sub> =25°C	108	120	132	kHz
Voltage Stability		12 ≤ V <sub>CC</sub> ≤ 18 V		0.2	1	%
Temperature Stability	TC <sub>F</sub>	$T_{MIN} \le T_J \le T_{MAX}$		5		%
Amplitude	Vosc	VRT/CT peak-to-peak		1.55		V
Upper Trip Point	V <sub>H</sub>			2.80		V
Lower Trip Point	VL			1.25		V
Discharge Current	I <sub>DSC</sub>		7.50	8.70	9.50	mA
Duty cycle Limit		R <sub>T</sub> =680 Ω, C <sub>T</sub> =10nF, T <sub>J</sub> =25°C	46	50	54	%
Over-Temperature Shutdown	T <sub>OT</sub>			140		°C
Soft Start Comparator						•
SS Charge Current	I <sub>SS</sub>	V <sub>SS</sub> ≤ V <sub>RAMP</sub>	-4	-6	-10	μА
SS Discharge Current	I <sub>Dsc</sub> SS	V <sub>SS</sub> = 1 V, V <sub>OV</sub> > 2.5V	2	8		mA
SS Lower Clamp	V <sub>SS Low</sub>			0.6		V
RAMP High Level	V <sub>RAMPH</sub>	T <sub>J</sub> =25°C		2.15		V
RAMP Low Level	V <sub>RAMPL</sub>	T <sub>J</sub> =25°C		0.6		V
RAMP Levels TC		Note: RAMP wavefrom is the same as the RT/CT wavefrom, but level shifted down one diode drop		-2		mV/°C
RAMP Sink Current	IRAMPL	T <sub>J</sub> =25°C	-0.1	-0.2		mA
RAMP Source Current	I <sub>RAMPH</sub>	T <sub>J</sub> =25°C	1			mA
Propagation Delay to Output	t <sub>PB</sub>			85	150	ns

#### Electrical Characteristics (cont'd)

Electrical Characteristics are guaranteed over full junction temperature range (0 to 105° C). Ambient temperature must be derated based on power dissipation and package thermal characteristics. Unless otherwise specified, the conditions of test are  $V_{CC} = 15 \text{ V}$ ; BOK = 3 V; OV = 0V;  $R_T = 680 \Omega$ ;  $C_T = 10 \text{ nF}$ . To override UVLO,  $V_{CC}$  should be raised above 18 V prior to test.

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Housekeeping			•	•		
BOK UV Threshold	V <sub>BOK</sub> UV	V <sub>REG</sub> = 5 V	2.500	2.537	2.575	V
BOK UV Hysteresis Current	I <sub>HYST ВОК</sub>	V <sub>BOK</sub> = 2.6 V	42	50	58	μΑ
BOK Input Bias Current	l <sub>OFF BOK</sub>	V <sub>BOK</sub> = 2.4 V		0.1	1.0	μΑ
OV Threshold	Vov		2.50	2.80	3.10	V
OV Clear Threshold	Vovн		3.80	4.00	4.50	V
OV Reset Threshold	V <sub>OVL</sub>		1.10	1.75	2.20	V
OV Bias Current	I <sub>BIAS OV</sub>	V <sub>REG</sub> = 5 V, V <sub>OV</sub> ≤ OV Threshold  * For Vov > OV Reset Threshold, see characteristic curve	-1	-0.2	1	μА
ACP Voltage	V <sub>ACP</sub>	I <sub>ACP</sub> = 10 μA		1.3		V
ACP Voltage	V <sub>ACP</sub>	I <sub>ACP</sub> = -10 μA		-1.2		V
LEN Charge Current	I <sub>LEN</sub>	$I_{ACP} = 10 \mu A; V_{LEN} = 0 V$	-30	-45	-65	μΑ
LEN Charge Current	I <sub>LEN</sub>	$I_{ACP} = -10 \mu\text{A}; \ V_{LEN} = 0 \text{V}$	-30	-50	-65	μΑ
Minimum Voltage for LEN Functionality	V <sub>LEN MIN</sub>			3.6	4.5	V
LEN Logic Reset Voltage	V <sub>LEN</sub>	This level reflects one diode drop of hysteresis from V <sub>LEN min</sub>		3.0		V
LEN Regeneration Current	I <sub>LENrgn</sub>			-10		μΑ
LEN Clamp	V <sub>LEN</sub>	I <sub>ACP</sub> = 5 μA	5.2	5.9	6.6	V
LEN Bias Current	I <sub>BIAS</sub> LEN	V <sub>LEN</sub> = 5 V, I <sub>ACP</sub> = 0 μA * For LEN input current over full range, see characteristic curve.		8		μА
Current Sense Comparator						
Transfer Gain	AV <sub>ISNS</sub>	-0.2 ≤ V <sub>ISNS</sub> ≤ 0.8 V	2.85	3.00	3.15	V/V
I <sub>SNS</sub> Level Shift	V <sub>LS</sub>	V <sub>ISNS</sub> = 0 V		1.50		V
Maximum Input Signal		V <sub>COMP</sub> =+5 V	1.00	1.08	1.20	V
Power Supply Rejection Ratio	PSRR	12 ≤ V <sub>CC</sub> ≤ 18 V		70		dB
Input Bias Current	I <sub>BIAS</sub>			-1	-10	μА
Propagation Delay to Output	t <sub>PB</sub>			85	150	ns

#### Electrical Characteristics (cont'd)

Electrical Characteristics are guaranteed over full junction temperature range (0 to 105° C). Ambient temperature must be derated based on power dissipation and package thermal characteristics. Unless otherwise specified, the conditions of test are  $V_{CC} = 15 \text{ V}$ ; BOK = 3 V; OV = 0V;  $R_T = 680 \Omega$ ;  $C_T = 10 \text{ nF}$ . To override UVLO,  $V_{CC}$  should be raised above 18 V prior to test.

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Under Voltage Lockout					•	
Startup Threshold	V <sub>CC</sub> (ON)		12.5	14.0	15.8	V
Minimum Operating Voltage after Trun-on	V <sub>CC</sub> (OFF)		7.3	8.0	8.5	V
Startup Current	Icc	V <sub>CC</sub> = 12 V; V <sub>ACP</sub> = V <sub>LEN</sub> = 0 V		2	10	μΑ
Startup Current	Icc	V <sub>CC</sub> = 12V; I <sub>ACP</sub> = 5 μA		225	300	μΑ
Operating Supply Current	Icc			12	20	mA
Maximum Operating Supply Voltage	V <sub>CC Max</sub>				18	V
Output Impedance to GND in UVLO State	Z <sub>OUT</sub>	V <sub>CC</sub> = 6 V		22.0		kΩ
Output						
Output Low Level	V <sub>OL</sub>	I <sub>SINK</sub> = 20 mA		0.1	0.4	V
Output Low Level	V <sub>OL</sub>	I <sub>SINK</sub> = 150 mA		1.5	2.2	V
Output High Level	V <sub>OH</sub>	I <sub>SOURCE</sub> = 20 mA	13	13.5		V
Output High Level	V <sub>OH</sub>	I <sub>SOURCE</sub> = 150 mA	12	13		V
Rise Time	t <sub>R</sub>	C <sub>L</sub> = 1 nF		50	150	ns
Fall Time	t <sub>F</sub>	C <sub>L</sub> = 1 nF		50	150	ns
Maximum Duty Cycle	D <sub>MAX</sub>		94	97	100	%
Minimum Duty Cycle	D <sub>MIN</sub>		0			%

ASTEC reserves the right to make changes without further notice to any products described herein to improve reliability, function, or design. ASTEC does not assume any liability arising out of the application or use of any product or circuit described herein; neither does it convey any license under its patent rights or the rights of others. ASTEC products are not authorized for use as components in life support devices or systems intended for surgical implant into the body or intended to support or sustain life. Buyer agrees to notify ASTEC of any such intended end use whereupon ASTEC will determine availability and suitability of its products for the intended use. ASTEC and the ASTEC logo are trademarks of ASTEC (BSR) PLC.

#### **ASTEC SEMICONDUCTOR**

255 Sinclair Frontage Road • Milpitas, California 95035 • Tel. (408) 263-8300 • FAX (408) 263-8340