Austria Mikro Systeme International AG

13-BIT LINEAR FEATURE CODEC WITH ANALOGUE FRONTEND

Key Features

- 13-Bit Linear Sigma Delta Codec with Filters Exceeding ETSI prETS30085 and G712 .
- Single Rail 3.0 V ~5.5 V Power Supply.
- Typical Power Dissipation of 30 mW at 3 V.
- Two Low Noise Microphone Inputs with Internal Gain Adjust (+16 / +46 dB).
- 150Ω Push/Pull Earpiece Driver with Internal Gain Adjust (-12 / +6 dB).
- 50Ω Loudspeaker Amplifier with up to 50 mW Output Power.
- Push/ Pull Output Driver for Tone Ringer.
- On Chip Electret Microphone Voltage Source.
- Digital Transmit Gain Setting (-38 / +10 dB).
- Digital Receive Gain Setting (-42 / +6 dB).
- Digital Sidetone Control Function (0 / -48 dB).
- Programmable Call Progress Tone/ DTMF / Ring Tone Generator.
- Analogue and Digital Loopback Modes.
- 16-Bit Linear / 8-Bit A-Law Switchable Serial PCM Interface with Non Delayed and Delayed Timing Modes.
- 4-Wire Serial Control Interface.
- Packaged in SOIC-28, TQFP-64.

General Description

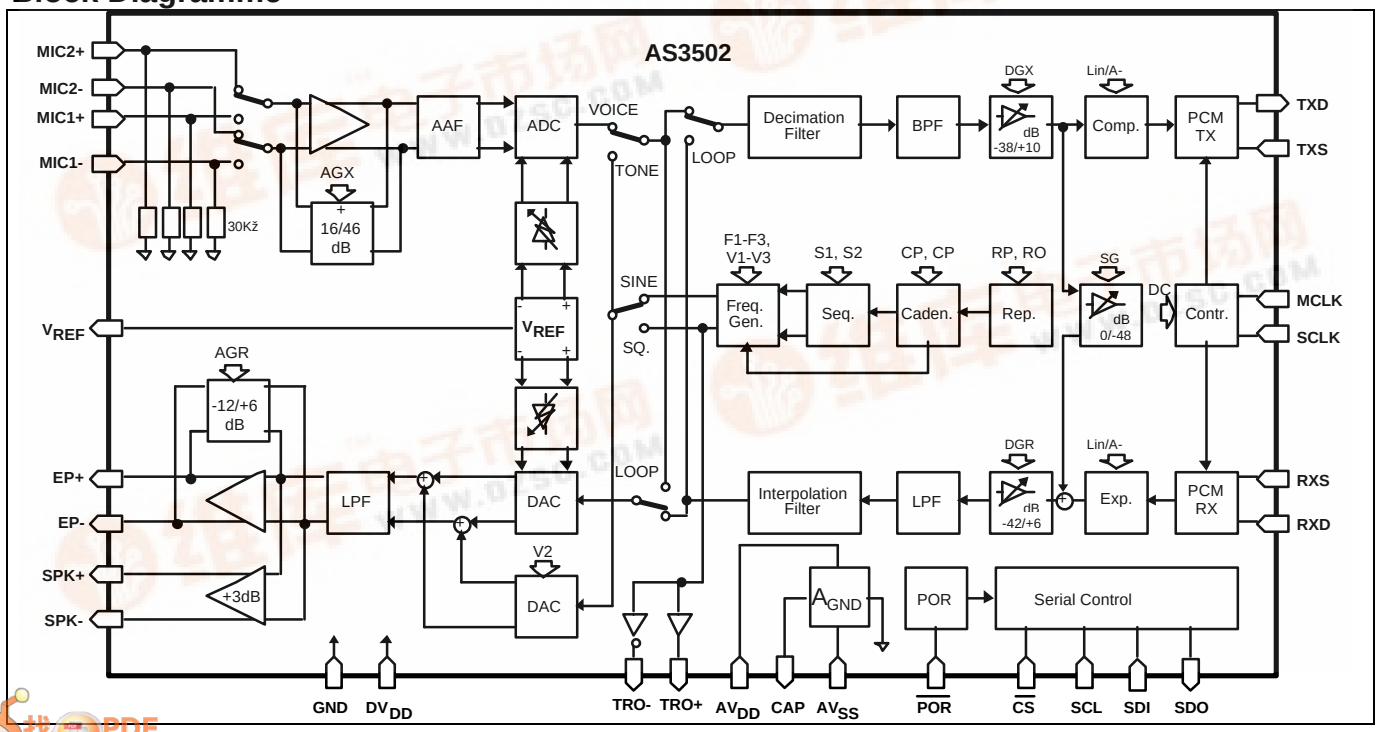
AS3502 is a high performance 13-bit linear feature Codec/Filter with 8 kHz sampling rate specifically tailored to implement all analogue frontend functions of battery powered digital terminals. It includes a programmable analogue interfaces for handset and handsfree operation with a minimum amount of external components.

The Codec function of AS3502 uses Sigma-Delta (ΣΔ) modulation conversion techniques with 2nd order modulators and an over sampling rate of 128 for excellent signal to noise performance. The AS3502 exceeds all CCITT G712 recommendations and the European ETSI prETS 300085 recommendations.

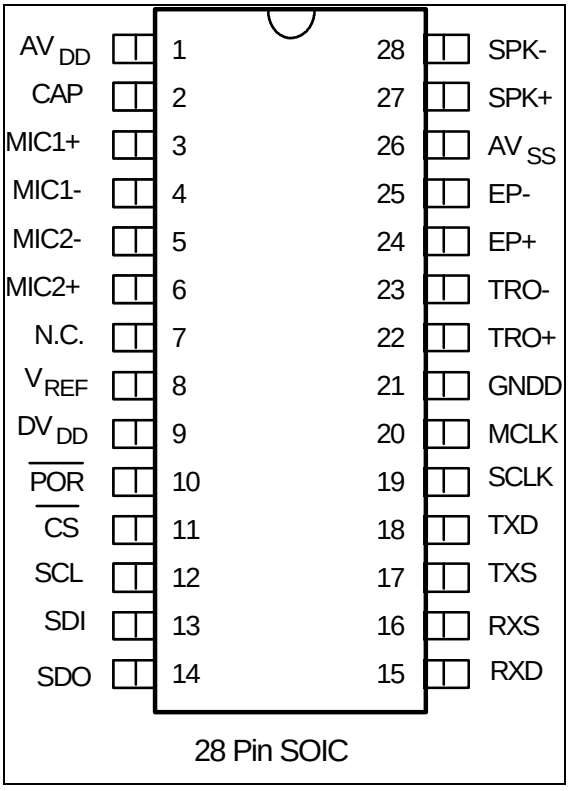
Digital gain setting stages for transmit and receive allow to compensate for transducer tolerances and to set up a handsfree function under software control. A programmable tone generator allows to generate DTMF/Call-Progress Tones and alert sounds required in digital terminals. All programmable functions of AS3502 are controlled by a 4-wire serial control port that easily interfaces to any popular micro controller.

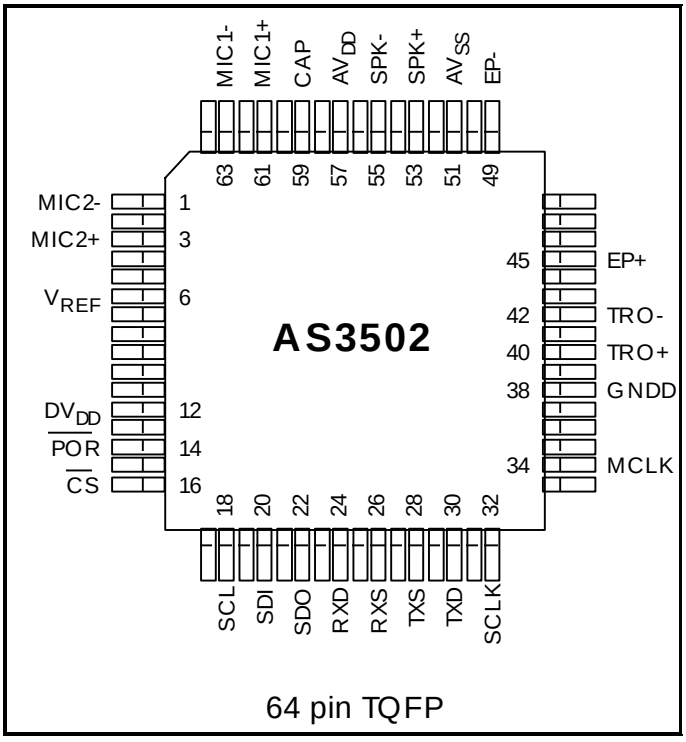
The interface to the digital world is accomplished by a serial PCM interface that supports 16-bit linear format or 8-bit A-Law format for both non-delayed and delayed frame synchronzation modes.

Block Diagramme



Pinout Diagramme





Pin Description

Pin #	Name	Type	Function
1	AVDD	SI	**Analogue Positive Supply Voltage Input**
2	CAP	AO	**Filter Capacitor Output** This pin requires to be connected to an external blocking capacitor of app. 47µF and is internally connected to the potential divider of the analogue ground generation circuit.
3 4	MIC1- MIC1+	AI AI	**Differential Microphone 1 Inputs** These two pins are differential inputs to the analogue input multiplexer of the gain programmable microphone amplifier with an input impedance of approx. 60 kΩ.
5 6	MIC2- MIC2+	AI AI	**Differential Microphone 2 Inputs** These two pins are differential inputs to the analogue input multiplexer of the gain programmable microphone amplifier with an input impedance of approx. 60 kΩ.
7	N.C.		
8	VREF	AO	**Microphone Reference Voltage Output** This pin provides a stabilized reference voltage for an electret microphone of approx. 2V.
9	DVDD	SI	**Digital Positive Supply Voltage Input**

Pin Description (continued)

Pin #	Name	Type	Function
10	$\overline{\text{POR}}$	DI	**Power On Reset Input** An active Low signal on this pin starts the system initialization. All internal registers are set to their default values and the serial interface will be reinitialized and the chip will enter power down mode.
11	$\overline{\text{CS}}$	DI	**Serial Control Chip Select Input** An active Low signal on this pin enables serial data transfers via SDI and SDO.
12	SCL	DI	**Serial Control Clock Input** This pin acts as shift clock signal input for serial control data transfer via SDI and SDO when $\overline{\text{CS}}$ is active Low and may be asynchronous to all other clock signals.
13	SDI	DI	**Serial Control Data Input** This input samples control data bits on the rising edges of the serial clock SCL when $\overline{\text{CS}}$ is active Low. Depending on the type of transfer 8 or 16 bits are shifted in.
14	SDO	DO	**Serial Control Data Output** This output shifts out control/status data with the falling edge of SCL when $\overline{\text{CS}}$ is active Low.
15	RXD	DI	**Receive PCM Data Input** This input samples PCM data bits on the falling edges of the serial clock SCLK following a rising edge on the receive strobe signal. After the time when all data bits have been shifted into the receive shift register all bits are latched into the receive latch for digital to analogue conversion.
16	RXS	DI	**Receive PCM Strobe Input** The signal on this input initiates shifting of serial data into the receive shift register. It must be synchronized with SCLK. The clock rate is typically 8 kHz. The signal width determines whether short strobe or long strobe mode is used: A pulse width of one to two shift clock periods selects short strobe mode. (For further information see PCM Timing Diagramme). The strobe signal does not need to be active throughout the transmission period since an internal bit counter generates the necessary timing for 8 or16 bit periods depending on the selected output format for serial PCM reception.
17	TXS	DI	**Transmit PCM Strobe Input** This signal on this input initiates shifting of serial data out of the transmit shift register. It must be synchronized with SCLK. The clock rate is typically 8 kHz. The signal width determines whether short strobe or long strobe mode is used: A pulse width of one to two shift clock periods selects short strobe mode. Pulse widths from 3 clock periods on wards select long strobe mode. The strobe signal does not need to be active throughout the transmission period since an internal bit counter generates the necessary timing for 8 or 16 bit periods depending on the selected output format for serial PCM transmission.
18	TXD	DO	**Transmit PCM Data Output** This Tristate output shifts out PCM data from the Codec's A/D converter and is activated during the transmission of serial data for 8 or 16 transmit clock periods following a rising edge on the transmit strobe signal. It is updated by the rising edges of the SCLK clock signal. The output goes back to high impedance after transmission of 8 or 16 data bits.

Pin Description (continued)

Pin #	Name	Type	Function
19	SCLK	DI	**Serial PCM Shift Clock Input** This pin acts as shift clock input signal for the externally provided signal for serial PCM data transfer. The frequency may vary from 128 kHz to 4.096 MHz in 8 kHz increments and should be synchronized to MCLK. In the receive direction the bitstream is latched with the falling edge of this clock. In the transmit direction the bitstream is shifted out with the rising edges of this clock.
20	MCLK	DI	**Master Clock Input** This signal is the timing reference for all internal operations. The clock frequency must be a integer multiple of 2.048 MHz with a maximum of 18.432MHz and must be synchronized to SCLK. The required master clock dividing ratio is selected by setting the DIV3 -DIV0 bits in the Digital Control Register.
21	GND	SI	**Digital Negative Supply Voltage Input**
22 23	TR+ TR-	DO DO	**Differential Toneringer Outputs** These digital outputs provide square or sine wave signal for driving transducers directly. TRO+ and TRO- are operating in push/pull mode providing peak to peak voltage swing of 2 x VDD.The output volume is programmable and is accomplished either through pulse density modulation or through pulse width modulation.
24 25	EP- EP+	AO AO	**Differential Earpiece Outputs** These two pins are the outputs of the differential earpiece amplifier driving either dynamic earpieces with 150Ω impedance or ceramic transducers with up to 50nF directly. The signal reference on both pins is DC referenced to the internally generated Analogue Ground which is appr. 1/2 VDD.
26	AVSS	SI	**Analogue Negative Supply Voltage Input**
27 28	SP+ SP-	AO AO	**Differential Loudspeaker Outputs** These two pins are the outputs of the differential loudspeaker amplifier that is capable driving dynamic speakers with 50Ω impedance directly. The maximum output power is 50mW. The signal reference on both pins is DC referenced to the internally generated Analogue Ground which is appr. 1/2 VDD.

AI: Analogue Input
DI: Digital Input
DI/O: Digital Input/Output
AO: Analogue Output
DO: Digital Output
SI: Supply Input

Functional Description

Power-On Reset

When power is applied first a power on reset signal is generated on chip which initializes AS3502:
The on chip programmable AFE registers are set to their default values (those values are defined in the register allocation section), the tone control register is set to the default status and the serial interface is initialized. AS3502 remains in power down state until a software start-up command. An active Low signal with a duration of min. 25 µs on the power on reset pin can be used to externally reset the device AS3502. For normal operation this pin must be pulled High.

Power Up Mode

AS3502 is powered up through a one byte start-up command. The byte written into the Digital Control Register DC allows to individually enable the transmit and the receive section. If the transmit channel is enabled first, the receive channel may be enabled any time without any restrictions. On enabling the receive channel and subsequent enabling of the transmit channel the PCM strobe signals TXS and RXS have to be tied together. The configuration information written into the AC and AG define which analogue transducer interfaces will be enabled on power up. The PCM output TXD remains in Tristate until the second frame synchronization signal after start-up. Any of the programmable registers may be modified while AS3502 is in active mode.

Power Down Mode

In power down mode all chip functions except the serial interface are kept inactive. All analogue functions are powered down and all digital outputs are put into Tristate mode. In this operating state the internal registers are normally configured to the desired values prior to the start-up command. The chip can be brought into power down mode any time through a power down command written into the DC Register. In this case all programmable registers retain their programmed values.

Analogue Input interface

The AS3502 input interface provides two identical differential inputs e.g. for a handset microphone and for a handsfree microphone. The input sources are selected through the AG register. Clipping of signals with arbitrary DC offset must be avoided by capacitive coupling. The input impedance of 2 x 30 kΩ is compatible with both electret and dynamic microphones. Each input is connected through an analogue input multiplexer to a low noise high gain preamplifier. The gain is software programmable through register AG from +16 to +46 dB in 6 dB steps with a tolerance of ±0.2 dB. This wide range guarantees optimum usage of the A/D converter dynamic range with various transducers.

Analogue Output Interface

The AS3502 output interface provides differential outputs for an earpiece, for a loudspeaker and for a toneringer. The output stages are selected through the AC register. The earpiece output driver is a fully differential amplifier that is capable of driving 3.2Vpp into a 150Ω transducer directly and is gain programmable in three steps from -12 dB to +6 dB through the AG register. The +6 dB step allows to drive ceramic earpiece transducers or to boost the receive amplitude. The loudspeaker driver is a fully differential power amplifier with a peak output power of 50 mW into a 50Ω loudspeaker. This output allows loudhearing and handsfree operation under software control.
The tone ringer outputs are digital push/pull outputs with rail to rail voltage swing that capable of driving various toneringers. For volume control the output signal may be either pulse density modulated or pulse width modulated under software control.

Transmit Section

The scaled analogue input signal enters a 1st order RC antialiasing filter with a corner frequency of approx. 40 kHz. This filter eliminates the need for any off chip filtering as it provides sufficient attenuation at 1.024 MHz to avoid aliasing. From there the bandlimited signal is fed to a 2nd order Sigma Delta modulator with a sampling frequency of 1.024 MHz. A factory trimmed voltage reference guarantees accurate absolute transmit gain (0 dBm0 reference level). The modulator is followed by a digital decimation filter that transforms the resolution in time to resolution in amplitude. The decimation filter is followed by a minimum phase 5th order IIR filter implementing the CCITT lowpass portion of the encoder bandpass frequency characteristics. Finally a 3rd order IIR high pass filter implements the highpass portion of the encoder bandpass frequency characteristics according to CCITT specifications.
The digitally filtered signal is further fed to a digital gain setting stage which allows to program the gain from -38 to +10 dB with a tolerance of better than ±0.05 dB from 0 to +6 dB to compensate for transducer sensitivity variations. The same stage may additionally be used for digital volume control for transmit volume attenuation. This feature may be used for software based handsfree voice switching algorithms.
In case of 16 bit linear mode the voice band signals are converted to a PCM two's complement 12 data bit plus sign bit format with a sample rate of 8 kHz and

shifted out of the encoder under control of an externally applied shift clock signal SCLK.
In case of 8-bit companded mode the voice band signals are converted to a PCM two's complement 7 data bit plus sign bit A-Law format with a sample rate of 8 kHz and shifted out of the encoder under control of an externally applied shift clock signal SCLK.

Receive Section

In case of 16 bit linear mode PCM data is shifted into the input shift register at a clock rate determined by the shift clock SCLK every 128 µs. 13 bits of PCM data are transferred to the receive latch that holds the data throughout the conversion process.
In case of 8-bit companded mode PCM data is shifted into the input shift register at a clock rate determined by the shift clock SCLK every 128µs and converted from A-Law format to 13-bit linear format. Optionally a programmable digital sidetone stage adds a certain amount of the transmit signal to the receive path for natural acoustic performance. The sidetone range can be adjusted from -48 dB to 0 dB with a default value of -18 dB. Both signals are combined and fed to a digital gain setting stage which allows to program the gain from -42 to +6 dB with a tolerance of ±0.05 dB from 0 to -6dB to compensate for transducer sensitivity variations. The same stage may additionally be used for digital volume control for receive volume attenuation. This feature may be used for software based handsfree voice switching algorithms. The gainsetting stage is followed by a digital filter that bandlimits the signal according to CCITT recommendations and that converts the resolution in amplitude to resolution in time through interpolation. The output signal is fed to a digital 2nd order sigma delta modulator with a sampling rate of 1.024 MHz. The bit stream is further fed to a combined 1 bit DAC / 2nd order SC Lowpass filter with an corner frequency of 8 kHz and further to a 1st order RC active smoothing filter that provides additional filtering of out of band signals.
The loudspeaker volume may be controlled digitally through the Receive Digital Gain Register DGR.

Tone Generator

AS3502 contains a powerful tone generator that is capable of generating all European country specific ring/ call progress tones and DTMF tones for audible feedback in the receive path or inband signalling tones in the transmit path under software control.
The tone generator operation modes are programmable through 13 8-bit registers that are accessed through the serial control interface. (See register description for further details). Since all melody functions are handled by the AS3502 tone generator hardware only a minimum amount of software overhead for the controlling microprocessor is necessary.
The tone generator consists of a single /dual tone synthesizer, a six tone sequencer, a cadence counter and a repetition counter.

Frequency Generator

For in band signalling a square wave or sine signal with precise DTMF capability is generated. The tones may be added to the receive section or injected into the transmit section. For tone ringing a square wave push/pull signal is generated on the TRO+ and TRO-. digital outputs.

Transmit Tone Volume Control

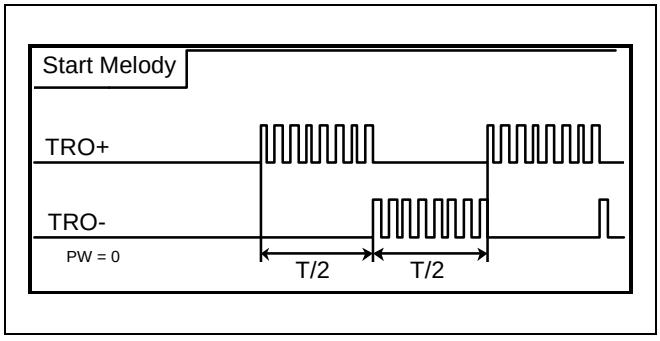
For sine wave forms the transmit PCM level is controlled by a 0 /-2.5 dB attenuation block and additionally by the digital transmit gain stage (DGX).
For square wave forms the transmit PCM level is controlled by the V1 register and the DGX register.

Receive Tone Volume Control

The receive amplitude of sine wave signals may be controlled via the V2 register.
The receive amplitude of square wave signals may be controlled by both the V1 and the V2 register.

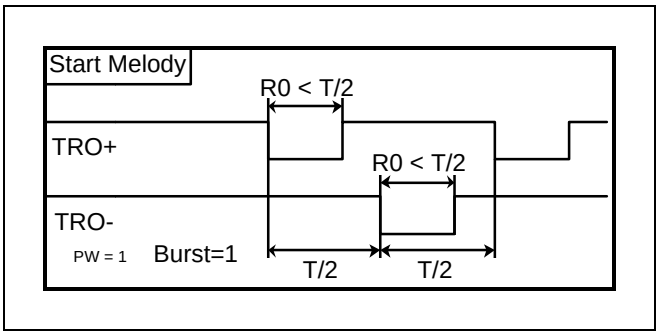
Tone Ringer Volume Control

The output volume is programmable through the V1 register and is accomplished either through pulse density modulation or through pulse width modulation.
For pulse density volume control the amplitude is controlled through the V1 register.



Pulse Density Volume Control

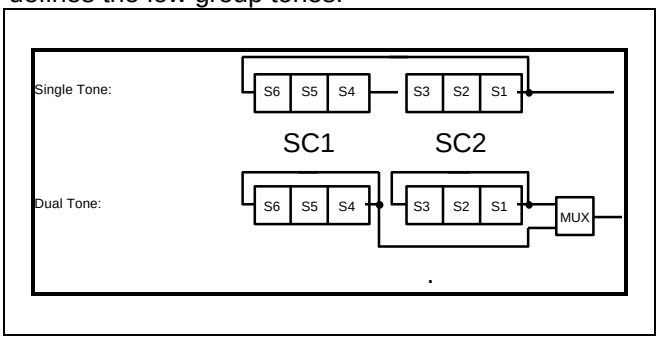
For pulse width volume control the R0 counter is used where it generates the duty cycle. In this case the repetition has to be controlled by the microprocessor through software.



Pulse Width Volume Control

Sequencer

The sequencer controlling the synthesizer is a six step rotating shift register that is controlled by a cadence counter. Each location in the two sequence control registers (SC1, SC2) contains the value of one out of three different frequencies or the value of a tone pause that are played in consecutive order. In DTMF mode the 6-bit shift register is split up into two 3-byte shift registers. In this mode the cadence steps are interleaved as S1/S4, S2/S5, S3/S6 where the SC1 register defines the high group tones with an attenuation of 2.5 dB and where the SC2 register defines the low group tones.

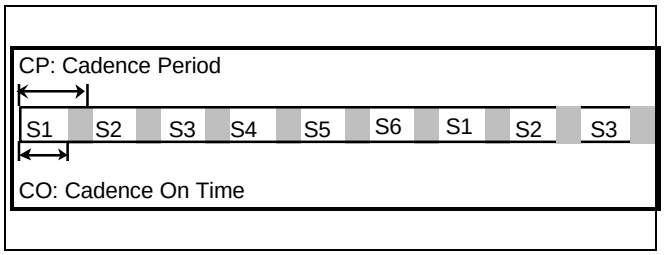


Tone Sequencer

Cadence Generation

The cadence counter determines the sequencer rotation speed and the on/ off timing characteristics of the tones and controls both the sequencer shift clock and the tone synthesizer on/ off time. The tone off time allows to insert pauses on switching from one frequency to the other.

Cadence Period (CP) and Cadence On Time (CO) are programmed with an 8-bit value. The CS bit defines two time spans with different resolution:



Cadence Counter

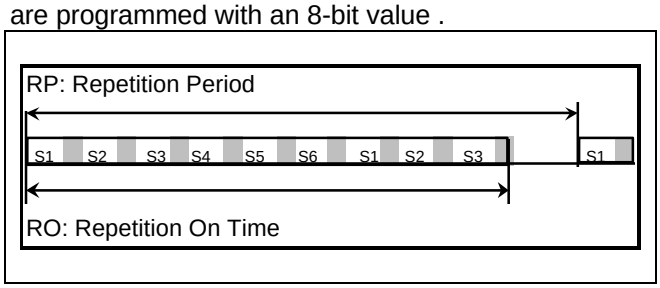
Repetition Counter

The repetition counter controls either the duration (RO) and repetition (RP) of the melody sequence or the volume for pulse width volume control of the tone ringer output.

In repetition mode the repetition counter may be operated in continuous mode where the ringing signal is turned on and off with the RP and R0 period or in single shot mode where the ringing signal is active for the R0 period. only.

Each tone signalling sequence must be started with this counter:

Repetition Period (RP) and Repetition On Time (RO) are programmed with an 8-bit value .



Repetition Counter

PCM Serial Interface

The AS3502 5-wire PCM port interfaces directly to many serial port standards. The PCM data word is either formated in 16-bit linear format with 13 bit 2`s complement data justified left where the last three LSB bits are reserved or formatted according to 8-bit A-Law format with alternate mark inversion (AMI) meaning that the even bits are inverted per CCITT G711 specification.

PCM Level	8-Bit A-Law Format								16-Bit Linear Format														
	D7	D6	D5	D4	D3	D2	D1	D0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
VIN = + Full Scale	1	0	1	0	1	0	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1	x	x	x
VIN = +0-Code	1	1	0	1	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	x	x	x
VIN = -0-Code	0	1	0	1	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	x	x	x
VIN = - Full Scale	0	0	1	0	1	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	x	x	x

x: not used

The interface supports short and long strobe synchronisation modes and full duplex synchronous operations of both receive and transmit section. PCM data is written into the transmit register and shifted out in 8 or 16 clock cycles by the transmit shift register. In the receive direction serial input 8 or 16 samples are converted into parallel format by the receive shift register and hereafter buffered in the receive latch. This double buffered hardware I/O scheme guarantees minimum port latency and increased channel service time. Both shift registers have separate strobe signals for asynchronous time slot operation of transmit and receive channel and are clocked by a common shift clock signal that may vary from 64 kHz up to 4.096 MHz and that must be locked to the master clock. The strobe signals have to be synchronised to the shift clock and should have a repetition rate of 8 kHz. ±50 ppm.

Short Strobe Mode

This is the default mode on powering up the device. The transmit and receive strobe inputs must be one bit shift clock long and have to be High during a falling edge of the respective bit shift clocks (see PCM Timing Diagramme) In the transmit section the next rising edges of SCLK enable the TXD output buffer and shift out PCM data bits. The falling edge of the last bit shift clock SCLK disables the TXD output buffer. In the receive section the next falling edge of SCLK shifts in PCM data bits at RXD.

Long Strobe Mode

The serial port enters the long strobe mode if both strobe pulses (TXS, RXS) are more than three bit clock periods long (See PCM Timing Diagramme). In the transmit section the next rising edge of SCLK or TXS, whichever comes later, clocks out the first bit. The effect of the transmit strobe occurring after the shift clock is to shorten the first bit at the TXD output. The following rising edges of the SCLK shift out the remaining data bits. The TXD output is disabled by the last falling SCLK edge or by the TXS signal going Low, whichever comes later. In the receive section a rising edge on the receive strobe input RXS will initiate the PCM data on RXD pin to be shifted into the receive shift register with the falling edges of SCLK.

Serial Control Interface

The internal operation of AS3502 is controlled by a 4-wire serial port that is designed to write and read back control and status information from any serial microprocessor port. It consists of a 16 bit shift register with 8 address bits and 8 data bits. The first byte is the Address Byte that is clocked in serially by asserting the $\overline{CS}$ line for 8 clock cycles. The MSB address bit in the address field defines whether the data transfer is a write or a read operation. The second byte is the Command Data Byte that is clocked in by keeping $\overline{CS}$ Low for another 8 clock cycles. The address decoder latches the address bits received into a register after 8 clock cycles. It operates fully autonomously and constantly cycles through 3 states:

- Load address decoder
- Calculate address and type of data transfer
- Data transfer

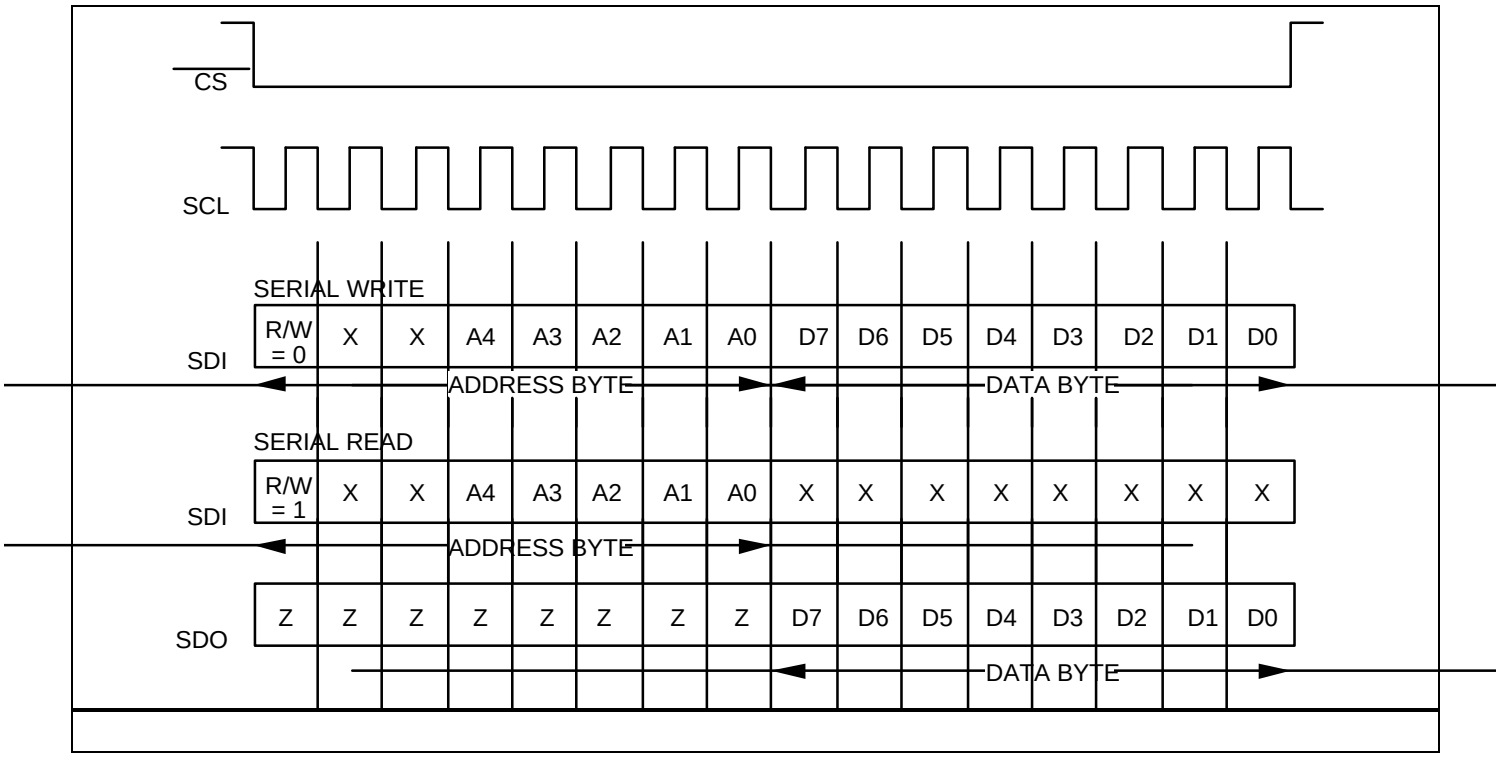
After decoding the data byte is latched into the decoded register during a write operation or retrieved from the selected register during a read operation.

Data is retrieved by asserting the $\overline{CS}$ line and by shifting 8 address bits into the input shift register through SDI. The next 8 clock cycles shift out the data byte through SDO. The full shift register is shifted out where the 8 MSB bits are shifted out as Hi-Z.

Data states on the SDO line can only change with the falling edge of SCL. Data on the SDI line is shifted in with the rising edge of SCL.

All commands are preceded by the start condition, which is a High to Low transition of the $\overline{CS}$ line. The AS3502 continuously monitors this line for the start condition and does not respond to any command until this condition has been met. $\overline{CS}$ may either be kept Low for 16 clock cycles or may go High after 8 clock cycles and go Low again for the next 8 clock cycles when programming different register locations.

All communications are terminated by a stop condition, which is a Low to High transition of $\overline{CS}$ after 16 shift clock cycles. The stop condition is also used to place the AS3502 serial control interface in the standby power mode.



Serial Control Interface

Programmable Functions

19 8-bit internal registers are provided for control and operation status monitoring. The addresses are divided into two register banks with 16 locations each. Address bit A4 selects between the upper and the lower register bank. Address bit A7 defines whether the operation will be a write or read operation.

Register Bit Summary

REGISTER		ADDR	DATA BIT NUMBER							
		A4- A0	D7	D6	D5	D4	D3	D2	D1	D0
Digital Control	**DC**	00_h	A / LIN	ENRX	ENTX	DIV3	DIV2	DIV1	DIV0	0
Analogue Control	**AC**	01_h	0	0	LOOP	CLRX	CLTX	ENEP	ENSPK	NOV
Analogue Gain	**AG**	02_h	0	ENM2	ENM1	AGX2	AGX1	AGX0	AGR1	AGR0
TX Digital Gain	**DGX**	03_h	DGX7	DGX6	DGX5	DGX4	DGX3	DGX2	DGX1	DGX0
Sidetone Gain	**SG**	05_h	SG7	SG6	SG5	SG4	SG3	SG2	SG1	SG0
RX Digital Gain	**DGR**	07_h	DGR7	DGR6	DGR5	DGR4	DGR3	DGR2	DGR1	DGR0
Tone Control	**TC**	10_h	TRINJ	RXINJ	TXINJ	CS	BURST MODE	SHAPE	TONE MODE	START
Sequence Control 1	**SC1**	11_h	0	0	$S3_1$	$S3_0$	$S2_1$	$S2_0$	$S1_1$	$S1_0$
Sequence Control 2	**SC2**	12_h	0	0	$S6_1$	$S6_0$	$S5_1$	$S5_0$	$S4_1$	$S4_0$
Frequency Control 1	**F1**	13_h	$F1_7$	$F1_6$	$F1_5$	$F1_4$	$F1_3$	$F1_2$	$F1_1$	$F1_0$
Volume Control 1	**V1**	14_h	0	$V1_4$	$V1_3$	$V1_2$	$V1_1$	$V1_0$	$F1_9$	$F1_8$
Frequency Control 2	**F2**	15_h	$F2_7$	$F2_6$	$F2_5$	$F2_4$	$F2_3$	$F2_2$	$F2_1$	$F2_0$
Volume Control 2	**V2**	16_h	0	0	$V2_3$	$V2_2$	$V2_1$	$V2_0$	$F2_9$	$F2_8$
Frequency Control 3	**F3**	17_h	$F3_7$	$F3_6$	$F3_5$	$F3_4$	$F3_3$	$F3_2$	$F3_1$	$F3_0$
Volume Control 3	**V3**	18_h	0	0	0	0	PS	PW	$F3_9$	$F3_8$
Repetition Period	**RP**	19_h	RP7	RP6	RP5	RP4	RP3	RP2	RP1	RP0
Repetition On Time	**RO**	$1A_h$	RO7	RO6	RO5	RO4	RO3	RO2	RO1	RO0
Cadence Period	**CP**	$1B_h$	CP7	CP6	CP5	CP4	CP3	CP2	CP1	CP0
Cadence On Time	**CO**	$1C_h$	CO7	CO6	CO5	CO4	CO3	CO2	CO1	CO0

1) DIGITAL CONTROL REGISTER

This register controls the master clock divider, the enabling of the transmit channel, the enabling of thereceive channel and the PCM format.

DC	D7	D6	D5	D4	D3	D2	D1	D0
Name	A/LIN	ENRX	ENTX	DIV3	DIV2	DIV1	DIV0	X
Default	0	0	0	0	0	0	0	X

Bit No	Symbol	Name and Description
D7	A/LIN	A-Law / Linear Select. In default mode or when set to Low 16-bit linear PCM format is selected. When set to High 8-bit A-Law PCM format is selected.
D6	ENRX	Enable Receive Channel. When set to High the Receive Channel including the selected output driver, the master clock divider and the Receive PCM interface are enabled. When set to Low the Receive Channel will be powered down.
D5	ENTX	Enable Transmit Channel. When set to High the Transmit Channel including the selected microphone input, the master clock divider and the Transmit PCM interface are enabled. When set to Low the Transmit Channel will be powered down.
D4- D1	DIV3-DIV0	Master Clock Prescaler Setting Bits.

DIV3	DIV2	DIV1	DIV0	State	Master Clock Frequency
0	0	0	0	÷1	2.048 MHz
0	0	0	1	÷2	4.096 MHz
0	0	1	0	÷3	6.144 MHz
0	0	1	1	÷4	8.192 MHz
0	1	0	0	÷5	10.240 MHz
0	1	0	1	÷6	12.288 MHz
0	1	1	0	÷7	14.336 MHz
0	1	1	1	÷8	16.386 MHz
1	0	0	0	÷9	18.432 MHz

2) ANALOGUE CONTROL REGISTER

The Analogue Control Register enables the output drivers and the muting of the receive voice channel. Further it allows to monitor clipping in both the transmit and the receive channel for software based automatic gain control.

AC	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	LOOP	CLIPRX	CLIPTX	ENEP	ENSPK	NOV
Default	0	0	0	0	0	0	0	0

Bit No	Symbol	Name and Description
D7-D6	-	These bits are Low during a read operation.
D5	LOOP	Loop Back Mode Enable. When set to High a loop back mode is enabled where the output of the sigma delta converter is directly fed to the input of the 1-bit DAC and where the output of the interpolation filter is fed to the input of the decimation filter.
D4	CLIPRX	Receive Channel Clipping. On reading this bit a High indicates an overload condition in the receive channel.
D3	CLIPTX	Transmit Channel Clipping. On reading this bit a High indicates an overload condition in the transmit channel.
D2	ENEP	Enable Earpiece. When set to High the earpiece driver is enabled. When set to Low the earpiece driver is powered down.
D1	ENSPK	Enable Speaker. When set to High the loudspeaker driver is enabled. When set to Low the loudspeaker driver is powered down. Both drivers may be activated if necessary e.g. for call progress monitoring.
D0	NOV	No Voice. When set to High the voice signal in the receive channel is muted.

3) ANALOGUE GAIN REGISTER

This register contains control bits for enabling on of the two microphone inputs and data for setting the analogue microphone amplifier and earpiece amplifier gains.

AG	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	ENM2	ENM1	AGX2	AGX1	AGX0	AGR1	AGR2
Default	0	0	0	0	1	0	0	0

Bit No	Symbol	Name and Description
D6	ENM2	Enable Microphone 2 Input. When set to High the microphone amplifier is connected to the MIC2 + and MIC2 - inputs.
D5	ENM1	Enable Microphone 1 Input. When set to High the microphone amplifier is connected to the MIC1+ and MIC1- inputs.
D4-D2	AGX2 - AGX0	Analogue Transmit Gain Setting (AGX). AGX2 AGX1 AGX0 Microphone Gain 0 0 0 +15.5 dB 0 0 1 +21.5 dB 0 1 0 +27.5 dB Default Value 0 1 1 +33.5 dB 1 0 0 +39.5 dB 1 0 1 +45.5 dB
D1- D0	AGR1 - AGR0	Analogue Receive Gain Setting. (AGR). AGR1 AGR0 Earpiece Gain 0 0 -12 dB Default Value 0 1 -6 dB 1 0 0 dB 1 1 +6 dB

4) TRANSMIT DIGITAL GAIN REGISTER

This register contains the 8 bit coefficient for digital transmit gain setting.

DGX	D7	D6	D5	D4	D3	D2	D1	D0
Name	DGX7	DGX6	DGX5	DGX4	DGX3	DGX2	DGX1	DGX0
Default	0	1	1	0	1	1	0	1

Bit No	Symbol	Name and Description
D7-D0	DGX7-DGX0	Transmit Digital Gain Setting (DGX). An 8-bit coefficient written into this register allows to trim the gain from -38 dB to +10 dB. The coefficient in decimal format for a given gain is calculated as: $X = 77 \times 10^{(\frac{DGX}{20})}$

Coefficient	Transmit Gain	Coefficient	Transmit Gain
154	+6 dB	27	-9 dB
137	+5 dB	19	-12 dB
123	+4 dB	13	-15 dB
109	+3 dB (Default Value)	10	-18 dB
97	+2 dB	7	-21 dB
87	+1 dB	5	-24 dB
77	0 dB	3	-28 dB
55	- 3 dB	2	-32 dB
39	- 6 dB	1	-38 dB

5) SIDETONE GAIN REGISTER

This register contains an 8 bit coeficient for a digital sidetone. The sidetone may be disabled by writing 00_h into this register.

SG	D7	D6	D5	D4	D3	D2	D1	D0
Name	SG7	SG6	SG5	SG4	SG3	SG2	SG1	SG0
Default	0	0	1	0	0	0	0	0

Bit No	Symbol	Name and Description
D7-D0	SG7-SG0	Digital Sidetone Attenuation Control. An 8-bit coefficient written into this register allows to control the sidetone attenuation in the receive channel. The sidetone attenuation range is 0 dB to -48dB. The coefficient in decimal format for a given attenuaton is calculated as: $X = 256 \times 10^{(\frac{SG}{20})}$ The sidetone default coefficient is 32 which corresponds to an attenuation of -18 dB.

6) RECEIVE DIGITAL GAIN REGISTER

This register contains an 8-bit coefficient for digital receive gain setting.

DGR	D7	D6	D5	D4	D3	D2	D1	D0
Name	DGR7	DGR6	DGR5	DGR4	DGR3	DGR2	DGR1	DGR0
Default	0	1	0	1	1	0	1	1

Bit No	Symbol	Name and Description
D7-D0	DGR7-DGR0	Receive Digital Gain Setting (DGR). An 8-bit coefficient written into this register allows to fine trim the receive path gain from -42 to +6 dB. The coefficient in decimal format for a given gain is calculated as: $X = 127.7 \times 10^{(\frac{DGR}{20})}$

Coefficient	Receive Gain	Coefficient	Receive Gain
128	0 dB	23	-15 dB
114	-1 dB	16	-18 dB
101	-2 dB	11	-21 dB
90	-3 dB (Default Value)	8	-24 dB
81	-4 dB	5	-27 dB
72	-5 dB	4	-30 dB
64	-6 dB	3	-33 dB
46	-9 dB	2	-36 dB
32	-12 dB	1	-42 dB

7) TONE CONTROL REGISTER

This register controls the various tone generator operation modes and the tone desstinations.

TC	D7	D6	D5	D4	D3	D2	D1	D0
Name	TRINJ	RXINJ	TXINJ	CS	BURST MODE	SHAPE	TONE MODE	START
Default	0	0	0	0	0	0	0	0

Bit No	Symbol	Name and Description
D7	TRINJ	Tone Ringer Inject. When set to High the tone generator is connected to the toneringer output. When set to Low the TRO+ and TRO- outputs are forced to high impedance state.
D6	RXINJ	Receive Inject. When set to High the tone generator is connected to the AS3502 receive section.
D5	TXINJ	Transmit Inject. When set to High the tone generator is connected to the AS3502 transmit section.
D4	CS	Cadence Slow Bit. When set to High the cadence step size resolution is 4 ms. When set to Low the cadence step size resolution is 1 ms.
D3	BURST MODE	When set to High tone burst mode operation is selected.
D2	SHAPE	When set to High square wave mode is selected. When set to Low sine wave mode is selected
D1	TONE MODE	Tone Mode Bit. When set to High dual tone mode is selected. When set to Low single tone mode is selected.
D0	START	Start Melody. When set to High the tone generation is enabled. This bit acts as single byte on/off sequence.

8) SEQUENCE CONTROL REGISTER 1

This register contains the frequency codes for the first three steps of the six tone cadence.

SC1	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	$S3_1$	$S3_0$	$S2_1$	$S2_0$	$S1_1$	$S1_0$
Default	0	0	x	x	x	x	x	x

Bit No	Symbol	Name and Description
D7, D6	-	Not used; will be low during read
D5, D4	$S3_1$, $S3_0$	Cadence Step 3: 00: No Tone 01: Frequency/Volume Register 1 is selected 10: Frequency/Volume Register 2 is selected 11: Frequency/Volume Register 3 is selected
	$S2_1$, $S2_0$	Cadence Step 2 00: No Tone 01: Frequency/Volume Register 1 is selected 10: Frequency/Volume Register 2 is selected 11: Frequency/Volume Register 3 is selected
D1, D0	$S1_1$, $S1_0$	Cadence Step1 00: No Tone 01: Frequency/Volume Register 1 is selected 10: Frequency/Volume Register 2 is selected 11: Frequency/Volume Register 3 is selected

9) SEQUENCE CONTROL REGISTER 2

This register contains the frequency codes for the second three steps of the six tone cadence.

SC2	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	$S6_1$	$S6_0$	$S5_1$	$S5_0$	$S4_1$	$S4_0$
Default	0	0	X	X	X	X	X	X

Bit No	Symbol	Name and Description
D7, D6	-	Not used; will be low during read
D5, D4	$S6_1$,$S6_0$	Cadence Step 6: 00: No Tone 01: Frequency/Volume Register 1 is selected 10: Frequency/Volume Register 2 is selected 11: Frequency/Volume Register 3 is selected
D3, D2	$S5_1$, $S5_0$	Cadence Step 5 00: No Tone 01: Frequency/Volume Register 1 is selected 10: Frequency/Volume Register 2 is selected 11: Frequency/Volume Register 3 is selected
D1, D0	$S4_1$, $S4_0$	Cadence Step 4 00: No Tone 01: Frequency/Volume Register 1 is selected 10: Frequency/Volume Register 2 is selected 11: Frequency/Volume Register 3 is selected

10) FREQUENCY CONTROL REGISTER 1

This register contains eight bits of the 10-bit coefficient of the first frequency.

F1	D7	D6	D5	D4	D3	D2	D1	D0
Name	$F1_7$	$F1_6$	$F1_5$	$F1_4$	$F1_3$	$F1_2$	$F1_1$	$F1_0$
Default	X	X	X	X	X	X	X	X

Bit No	Symbol	Name and Description
D7-D0	$F1_7$-$F1_0$	A 10-bit coefficient (X) written into this register and into bits D0 and D1 of V1 allows to programme the first frequency from 3.9 Hz to 3996 Hz. The coefficient for a given frequency can be calculated as: $X = \frac{f(Hz) * 256}{1000}$; X = (1…1023)

11) VOLUME CONTROL REGISTER 1

This register contains the remaining two bits of the first frequency coefficient and volume control data for pulse density volume control of square waves.

V1	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	$V1_4$	$V1_3$	$V1_2$	$V1_1$	$V1_0$	$F1_9$	$F1_8$
Default	X	X	X	X	X	X	X	X

Bit No	Symbol	Name and Description
D6-D2	$V1_4$-$V1_0$	A 5 bit coefficient (X) written into this register allows to programme both the tone ringer attenuation in pulse density mode and the attenuation of the tone generator in square wave mode. The coefficient in decimal format for a given attenuation can be calculated as: $X = 31*10\text{^}(\frac{Volume(dB)}{20})$;X= (1…31) $VOUT = 2*VDD*10\text{^}(\frac{V1}{20})$ (V) In tone generator square wave mode a 4-bit coefficient using bits $V1_3$ to $V1_0$ allows to programme the volume where coefficient in decimal format for a given volume can be calculated as: $X = 16*10\text{^}(\frac{Volume(dB)}{20})$;X= (0…15) In receive direction the absolute output value on the speaker and earpiece outputs depends on AGR and V2. *VOUTEP= 6.14 dBm + V2C + V1 + AGR* (dBm) *VOUTSP=6.14 dBm + V2 + V1 + 3 dB* (dBm) In transmit direction the output value depends on V1 and DGX. *VOUT = 6.14 dBm0 + V1 + DGX* (dBm0)
	$F1_9$-$F1_8$	These bits are the two most significant bits of the 10-bit frequency coefficient.

12) FREQUENCY CONTROL REGISTER 2

This register contains eight bits of the 10-bit coefficient of the second frequency.

F2	D7	D6	D5	D4	D3	D2	D1	D0
Name	$F2_7$	$F2_6$	$F2_5$	$F2_4$	$F2_3$	$F2_2$	$F2_1$	$F2_0$
Default	X	X	X	X	X	X	X	X

Bit No	Symbol	Name and Description
D7-D0	$F2_7$-$F2_0$	A 10-bit coefficient (X) written into this register and into bits D0 and D1 of V2 allows to programme the second frequency from 3.9 Hz to 3996 Hz. The coefficient in decimal format for a given frequency can be calculated as: $X = \frac{f(Hz)*256}{1000}$

13) VOLUME CONTROL REGISTER 2

This register contains the remaining two bits of the second frequency coefficient, and coarse and fine tone volume control data for the receive direction.

V2	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	$V2_3$	$V2_2$	$V2_1$	$V2_0$	$F2_9$	$F2_8$
Default	X	X	X	X	X	X	X	X

Bit No	Symbol	Name and Description
D5-D3	$V2_3$-$V2_1$	Receive Tone Coarse Volume Control (V2C) V23 V22 V21 Attenuation 0 0 0 - 10 dB 0 0 1 - 16 dB 0 1 0 - 22 dB 0 1 1 - 28 dB 1 0 0 - 34 dB 1 0 1 - 40 dB
D2	$V2_0$	Sine Tone Fine Volume Control (V2F) V20 Attenuation 0 0 dB 1 - 2.5 dB In transmit direction the sineoutput value depends on V2F and DGX: $VOUT_{SINE}$ = *3.8 dBm + V2F + DGX* (dBm0) $VOUT_{DTMF\ ROW\ TONE}$ = *-2.2dBm + DGX* (dBm0) $VOUT_{DTMFCOLUMN\ TONE}$ = *-4.7dBm + DGX* (dBm0) In receive direction the sine output value on earpiece and speaker depends on V2C, V1 and AGR: $VOUT_{EP}$= *3.8 dBm + V2C + V2F+ AGR* (dBm) $VOUT_{SP}$= *3.8 dBm + V2C + V2F+ 3dB* (dBm)
D1-D0	$F2_9$-$F2_8$	These bits are the two most significant bits of the 10-bit frequency coefficient.

14) FREQUENCY CONTROL REGISTER 3

This register contains eight bits of the 10-bit coefficient of the third frequency.

F3	D7	D6	D5	D4	D3	D2	D1	D0
Name	$F3_7$	$F3_6$	$F3_5$	$F3_4$	$F3_3$	$F3_2$	$F3_1$	$F3_0$
Default	X	X	X	X	X	X	X	X

Bit No	Symbol	Name and Description
D7-D0	$F3_7$-$F3_0$	A 10-bit coefficient (X) written into this register and into bits D0 and D1 of V3 allows to programme the third frequency from 3.9 Hz to 3996 Hz. The coefficient in decimal format for a given frequency can be calculated as: $X = \frac{f(Hz) * 256}{1000}$; X = (1…1023)

15) VOLUME CONTROL REGISTER 3

This register contains two bits of the third frequency coefficient and tone ringer volume mode control bits.

V3	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	PS	PW	$F3_9$	$F3_8$
Default	X	X	X	X	X	X	X	X

Bit No	Symbol	Name and Description
D3	PS	Pulse Width Slow Bit. When set to High the pulse width step size is 4 µs. When set to Low the pulse width step size is 1 µs.
D2	PW	Tone Ringer Volume Control Mode Bit. When set to Low pulse density volume control is selected. When set to High pulse width volume control is selected.
D1-D0	F29-F28	These bits are the two most significant bits of the 10-bit frequency coefficient.

16) REPETITION PERIOD REGISTER

RP	D7	D6	D5	D4	D3	D2	D1	D0
Name	RP7	RP6	RP5	RP4	RP3	RP2	RP1	RP0
Default	X	X	X	X	X	X	X	X

Bit No	Symbol	Name and Description
D7-D0	RP7-RP0	An 8-bit value written into this register allows to set the repetition period with 32ms accuracy. $X = \frac{Time(ms)}{32ms} - 1$; X= (1…255)

17) REPETITION ON REGISTER

RO	D7	D6	D5	D4	D3	D2	D1	D0
Name	RO7	RO6	RO5	RO4	RO3	RO2	RO1	RO0
Default	X	X	X	X	X	X	X	X

Bit No	Symbol	Name and Description
D7-D0	RO7-RO0	An 8-bit value written into this register allows to set the repetition on time with 32ms accuracy. If this time exceeds the repetition period time, continuous operation will be performed. Repetition times can only be generated when using pulse density volume control mode. $X = \frac{Time(ms)}{32ms}$; X= (1…255) If pulse width volume control mode is selected, an 8-bit value written into this register allows to set the duty cycle of the tone ringer outputs with two different accuracies depending on the PS bit in the volume Control Register 3 : PS=0: $X = \frac{Time(\mu s)}{1\mu s}$; X= (1…255) PS=1: $X = \frac{Time(\mu s)}{4\mu s}$; X= (1…255)

18) CADENCE PERIOD REGISTER

CP	D7	D6	D5	D4	D3	D2	D1	D0
Name	CP7	CP6	CP5	CP4	CP3	CP2	CP1	CP0
Default	X	X	X	X	X	X	X	X

Bit No	Symbol	Name and Description
D7-D0	CP7-CP0	A n 8-bit value written into this register allows to set the cadence period with two different accuracies. If the SLOW bit in the TC register is set to Low the resolution is 1ms: $X = \frac{Time(ms)}{1(ms)} - 1$; X= (1…255). If the SLOW bit in the TC register is set to High the resolution is 4ms: $X = \frac{Time(ms)}{4(ms)} - 1$; X= (1…255).

19) CADENCE ON REGISTER

CO	D7	D6	D5	D4	D3	D2	D1	D0
Name	CO7	CO6	CO5	CO4	CO3	CO2	CO1	CO0
Default	X	X	X	X	X	X	X	X

Bit No	Symbol	Name and Description
D7-D0	CO7-CO0	An 8-bit value written into this register allows to set the cadence on time with two different accuracies. If the SLOW bit in the TC register is set to Low the resolution is 1ms: $X = \frac{Time(ms)}{1(ms)}$; X= (1…255). If the SLOW bit in the TC register is set to High the resolution is 4ms: $X = \frac{Time(ms)}{4(ms)}$; X= (1…255).

Absolute Maximum Ratings*

Supply Voltage ..... $-0.3 \le V_{DD} \le 7$ V

Voltage applied on Any Input ..... $-0.3\ V \le V_{IN} \le V_{DD}+0.3$ V

Voltage applied on Digital Outputs ..... $-0.3\ V \le V_{OUT} \le V_{DD}+0.3$ V

Input Current (all pins) ..... $I_{IN} \le \pm 50$ mA

Output Current ..... $I_{OUT} \le \pm 10$ mA

Storage Temperature Range ..... -65 to +150°C

*Exceeding these figures may cause permanent damage. Functional operation under these conditions is not permitted

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min.	Typ.*	Max.	Units
VDD	Supply Voltage		3.0	4.5	5.5	V
TAMB	Operating Temperature Range		-40	+25	+70	°C
V_{IN}	Input Voltage		GND		V_{DD}	V
V_{OUT}	Tristate Output Voltage		GND		V_{DD}	V
CLOCK	Clock Frequency			2.048		MHz
SYNC	Synchronization Frequency			8		kHz

* Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing

DC Characteristics (-40°C<TA< +70°C, 3.0 V≤V_{DD}≤4.5 V)

Symbol	Parameter	Conditions	Min.	Typ.*	Max.	Units
V_{IL}	Input Low Level	All digital inputs			$0.3xV_{DD}$	V
V_{IH}	Input High Level	All digital pins	$0.7xV_{DD}$			V
V_{OL}	Output Low Level	1.6 mA			0.4	V
V_{OH}	Output High Level	1.6 mA	2.4			V
IL	Input Leakage Current	V_{IN}= GND to V_{DD}			±10	µA
I_{OZ}	High Impedance Current	V_{OUT}= GND to V_{DD}			±10	µA
I_{DD}	Supply Current	Outputs unloaded; V_{DD} = 3 V			10	mA
IDD0	Power Down Current	TA= 25°C V_{DD}= 3.0 V			5	µA

Analogue Interface With Microphone Input 1 & 2 (-40°C<TA< +70°C, 3.0 V≤V_{DD}≤4.5 V)

Symbol	Parameter	Conditions	Min.	Typ.*	Max.	Units
AIP	Peak Input Level	Note 1; THD </= 2% AGX= +16 dB; DGX= 0 dB AGX= +46 dB; DGX= 0 dB			 176 5.58	 mVrms mVrms
AIL	Nominal Input Level	0 dBm0; Default Gain: GX=+31 dB		21.8		mVrms
GX	Transmit Gain	GX = AGX + DGX	+16	+31	+52	dB
AGX	Analogue Gain Range		+15.5	+33.5	+45.5	dB
	Analogue Gain Step Size		5.8	6.0	6.2	dB
ZIN	Input Impedance	MIC+ to MIC-,0.3 ≤ f ≤ 3.4kHz	2 x 30			kΩ

* Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing

Note 1: This corresponds to a +3.14 dBm0 signal at the PCM output which is equal to a PCM overload level of ±4096;

Analogue Interface with Earpiece Output (-40°C<TA <+70°C, 3.0 V≤V_{DD}≤4.5 V; RL=150Ω from EP+ to EP-)

Symbol	Parameter	Conditions	Min.	Typ.*	Max.	Units
AOUTP	Peak Overload Level	Note 1 RL=150Ω THD= 2% GR=0 dB CL=60nF THD = 5% GR=+5 dB			 1.12 2.8	 Vrms Vp
AOUT	Nominal Output Level	0 dBm0 PCM Code GR=-15 dB		137.7		mVrms
RL	Load Resistance	EP + to EP-	150			Ω
GREP	Earpiece GainRange	GR = AGR + DGR	-18	-15	+6	dB
AGREP	Analogue Gain Range		-12		+6	dB
	Analogue Gain Step Size		5.8	6.0	6.2	dB
VOFF	Output Offset Voltage			± 100		mV

* Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing
Note 1: This corresponds to a +3.14dBm0 code at the PCM input which is equal to a PCM overload level of ±4096;

Analogue Interface with Speaker Output (-40°C<TA <+70°C, 3.0 V≤V_{DD}≤4.5 V; RL=50Ω from SPK+ to SPK-)

Symbol	Parameter	Conditions	Min.	Typ.*	Max.	Units
AOUTP	Peak Overload Level	Note 1 RL=50Ω THD= 5%, GRSPK= + 3dB	1570			mVrms
RL	Load Resistance	SPK+ to SPK	50			Ω
GRSPK	Speaker Receive Gain Range	GRSPK = AGRSPK + DGR	-3	0	+3	dB
AGRSPK	Speaker Analogue Gain			+3		dB
VOS	Output Offset Voltage	SPK+ to SPK-		± 100		mV

* Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing
Note 1: This corresponds to a +3.14dBm0 code at the PCM input which is equal to a PCM overload level of ±4096;

Analogue Interface with Tone Ringer Output (-40°C<TA <+70°C, 3.0 V≤V_{DD}≤4.5 V)

Symbol	Parameter	Conditions	Min.	Typ.*	Max.	Units
Vout	Max. Output Voltage Swing	TRO+ to TRO-		2 x VDD		Vpp
CL	Load Capacitance	TRO+ to TRO-			50	nF
TDR	Output Rise Time	CL = 50nF		100		µs
TDF	Output Fall Time	CL = 50nF		100		µs

* Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing
Note 1: See text for volume control

Microphone Reference Voltage Output (-40°C<TA <+70°C, 3.0V≤V_{DD}≤4.5V)

Symbol	Parameter	Conditions	Min.	Typ.*	Max.	Units
VREF	Reference Voltage	IL = 1 mA; Note 1	2.0	2.2	2.4	V
PSRR	Power Supply RejectionRatio	300 Hz to 3 kHz, 100 mVrms Note 2	55			dB
	Output Noise	300 Hz to 3.4kHz, Note 2			100	µV

* Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing
Note 1: VREF is turned off in power down mode
Note 2: VREF must be filtered by a suitable RC lowpass filter. A typical setup is using a 500Ω microphone feeding resistor and a 22 µF capacitor to ground.

Transmit Transmission Characteristics (-40°C<TA <+70°C, 3.0V≤V_{DD}≤4.5V; AGX=+16 dB; DGX= 0 dB) unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.*	Max.	Units
GXA	Absolute Transmit Gain Trimming and Step Deviations	25 °C, Note 1, MIC1 Input Steps: 16dB, 22dB, 28dB, 34dB, 40dB			±0.3	dB
GXAT	Gain Variation with Temp.			±0.1		dB
GXAV	Gain Variation with Supply				±0.05	dB
GXAG	Gain Variation with Digital Gain	0 dB ≤ DGX ≤ +6 dB			±0.05	dB
DGX	Digital Gain Setting Range	See text for coefficient calculation	0		+6	dB
GTX	Gain Variation with Input Level	1020 Hz tone ; AGX=40 dB; DGX=0 dB -40 to +3 dBm0 -50 to -40 dBm0 -50 to -55 dBm0			 ±0.2 ±0.4 ±0.8	 dB dB dB
GXAF	Transmit Frequency Response	Relative. to gain at 1020 Hz @ -10dBm0 50 Hz 60 Hz 100 Hz 200 Hz 300 to 3000 Hz 3400 Hz 3400 Hz to 4000 Hz 4000 Hz to 4600 Hz	 -1.8 -0.2 -1.1 	 	 -30 -30 -22 -0.1 0.2 0 Note 2 Note 3	 dB dB dB dB dB dB dB dB
DIS	Discrimination against Out -of Band Input Signals	4.6 kHz at--10 dBm0 8 kHz at -10 dBm0	35 45			dB dB
PDX	Absolute Group Delay	0 dBm0 at 1500 Hz		600		µs
DDX	Group Delay Distortion	Relative to minimum 500 Hz 630 Hz 800 Hz 1000 Hz 1250 Hz 1600 Hz 2100 Hz 2500 Hz	 	 190 100 50 20 0 0 10 50	 	 µs µs µs µs µs µs µs µs
STDX	Signal to Distortion Ratio	f = 1020 Hz , AGX=40 dB; DGX=0 dB; Note 4 0dBm0 -10dBm0 -30dBm0 -40dBm0 -45 dBm0	 50 50 40 31 26	 	 	 dBp dBp dBp dBp dBp
ICNX	Idle Channel Noise	Inputs shorted; AGX=40 dB; DGX=0 dB			-70	dBm0p
SFNX	Single Frequency. Noise	0.3 -3.4 kHz 10 Hz bandwidth; AGX=40 dB; DGX=0 dB			-75	dBm0
PSRRX	Transmit Power Supply Rejection Ratio	VDD + 100 mVrms 0 to 50 kHz inputs shorted; measured on TXD	50			dBp
CT RX->TX	Receive to Transmit Crosstalk		75			dB

* Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing

Note 1: The tolerance of the absolute input level is defined by the trimming accuracy of the converter reference.

Note 2: $GXAF = 15\left[\sin\frac{\pi(4000-f)}{1200} - 1\right]$ Note 3: $GXAF = 20\left[\sin\frac{\pi(4000-f)}{1200} - \frac{15}{20}\right]$

Note 4: Total distortion includes quantization and harmonic distortion;

Receive Transmission Characteristics (-40°C<TA <+70°C, 3.0 V≤V_{DD}≤4.5 V ; AGR = 0 dB; DGR = 0 dB; RL = 150Ω from EP+ to EP-) unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.*	Max.	Units
GRA	Absolute Receive Gain Trimming and Step Deviations	25 °C, Note 1 Steps: 0dB, -6dB, -12dB			±0.3	dB
GRAT	Gain Variation with Temp.			±0.1		dB
GRAV	Gain Variation with Supply				±0.05	dB
GRAG	Gain Variation with Digital Gain	-6 dB ≤ DGR ≤ 0 dB			±0.05	dB
DGR	Digital Gain Setting Range	See text for coefficient calculation	-6		0	dB
GTR	Gain Variation with Input Level	1020 Hz tone -40 to +3 dBm0 -50 to -40 dBm0 -50 to -55 dBm0			 ±0.2 ±0.4 ±0.8	 dB dB dB
GRAF	Receive Frequency Response	Relative to gain @ 1020 Hz, -10dBm0 0 Hz to 2400 Hz 2400 Hz to 3000 Hz 3400 Hz 3400 Hz to 4000 Hz	 -0.2 -0.25 -0.8		 0.2 0.2 0 Note 2	 dB dB dB dB
SOS	Spurious Out-of Band Signals at the Output	4.6 kHz @0 dBm0; 300 Hz ≤ f ≤3.4 kHz 8k Hz @-0 dBm0; 300 Hz ≤ f ≤3.4 kHz			-40 -50	dBm0 dBm0
PDR	Absolute Group Delay	0 dBm0 @ 800Hz		370		µs
DDR	Group Delay Distortion	Relative to minimum 500 Hz 630 Hz 800 Hz 1000 Hz 1250 Hz 1600 Hz 2100 Hz 2500 Hz		 0 0 0 10 20 30 60 110		 µs µs µs µs µs µs µs µs
STDR	Signal to Distortion Ratio	f = 1020 Hz , Note 3 0 dBm0 -10 dBm0 -30 dBm0 -40 dBm0 - 45 dBm0	 50 50 36 31 26			 dBp dBp dBp dBp dBp
ICNR	Idle Channel Noise	PCM +0 Code; AGR = + 6 dB			-75	dBm0p
SFNR	Sampling Frequency. Noise	selectively measured @ 8 kHz; AGR=+6 dB			-78	dBm0
PSRRR	Receive Power Supply Rejection Ratio	VDD + 100 mVrms; PCM +0 Code 0 - 4 kHz 4 - 50 kHz	 50 50			 dBp dB
CT TX->RX	Transmit to Receive Crosstalk	GR = -12 dB	75			dB

* Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing

Note 1: The tolerance of the absolute level is defined by the trimming accuracy of the converter reference.

Note 2: $$GRAF = 13\left[\sin\frac{\pi(4000-f)}{1200} - 1\right]$$

Note 3: Total distortion includes quantization and harmonic distortion.

Tone Generator Characteristics (-40°C<TA <+70°C, 3.0 V≤V_{DD}≤4.5 V)

Symbol	Parameter	Conditions	Min.	Typ.*	Max.	Units
f	Frequency Range	Step size is 3.9 Hz	3.9		3996	Hz
Æf	Frequency Tolerance				± 1	%
THD	Total Harmonic Distortion	300 Hz ≤ f ≤3996 Hz ; 3.14 dBm0			40	dB
tCP tCO	Cadence Period Cadence On Time	CS Bit = Low ; Step Size = 1 ms CS Bit = High; Step Size = 4 ms	2 8		255 1020	ms ms
tRP tRO	Repetition Period Repetition On Time	Step Size = 32 ms	64		8160	ms ms
tRO	Pulse Width Volume Period	PS Bit = Low; Step Size = 1µs PS Bit = High; Step Size = 4µs	2 8		255 1020	µs µs
$Vout_{TX}$	TX Sine Tone Level	Note 1;			3.14	dBm0
$Vout_{SINE-EP}$	Earpiece Sine Tone Level	Note 4; AGR= +6 dB			-0.2	dBm
$Vout_{SINE-SP}$	Speaker Sine Tone Level	Note 4; AGR= +6 dB			-2.8	dBm
Vout	TX DTMF Row Tone Level	Note 2			-4.7	dBm0
PREEM	DTMF Preemphasis	Column to Row Tone		+2.5		dB
V2	Sine Wave Volume Control		-42.5		-10	dB
dV2C	Volume Coarse Step Size			6		dB
dV2F	Volume Fine Step Size			2.5		dB
$Vout_{SQ}$	TX Peak Square Tone Level	Note 3			3.14	dBm
VoutSQ-EP	RX Peak Square Tone Level	AGR=+6dB; Note 5			-2.14	dBm
VoutSQ-SP	RX Peak Square Tone Level	GR=+3dB; Note 5			-0.76	dBm
V1	Square Wave Volume Control	See text for coefficient calculation	-30		0	dB

* Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing

Note 1: In the transmit direction the sine tone level is controlled by the DGX register and the V2F bit.

Note 2: In the transmit direction the DTMF level is controlled by the DGX register only.

Note 3: In the transmit direction the square tone level is controlled by the V1 register and the DGX register. Levels exceeding 3.14 dBm0 are limited by the transmit saturation logic to 3.14 dBm0.

Note 4: In the receive direction the sine tone level is controlled by the V2 and the AGR register.

Note 5: In the receive direction the square tone level is controlled by the V1, V2C and the AGR register.

Timing Specifications**PCM Interface Timing** (-40°C<TA <+70°C, 3.0 V≤V_{DD}≤4.5 V)

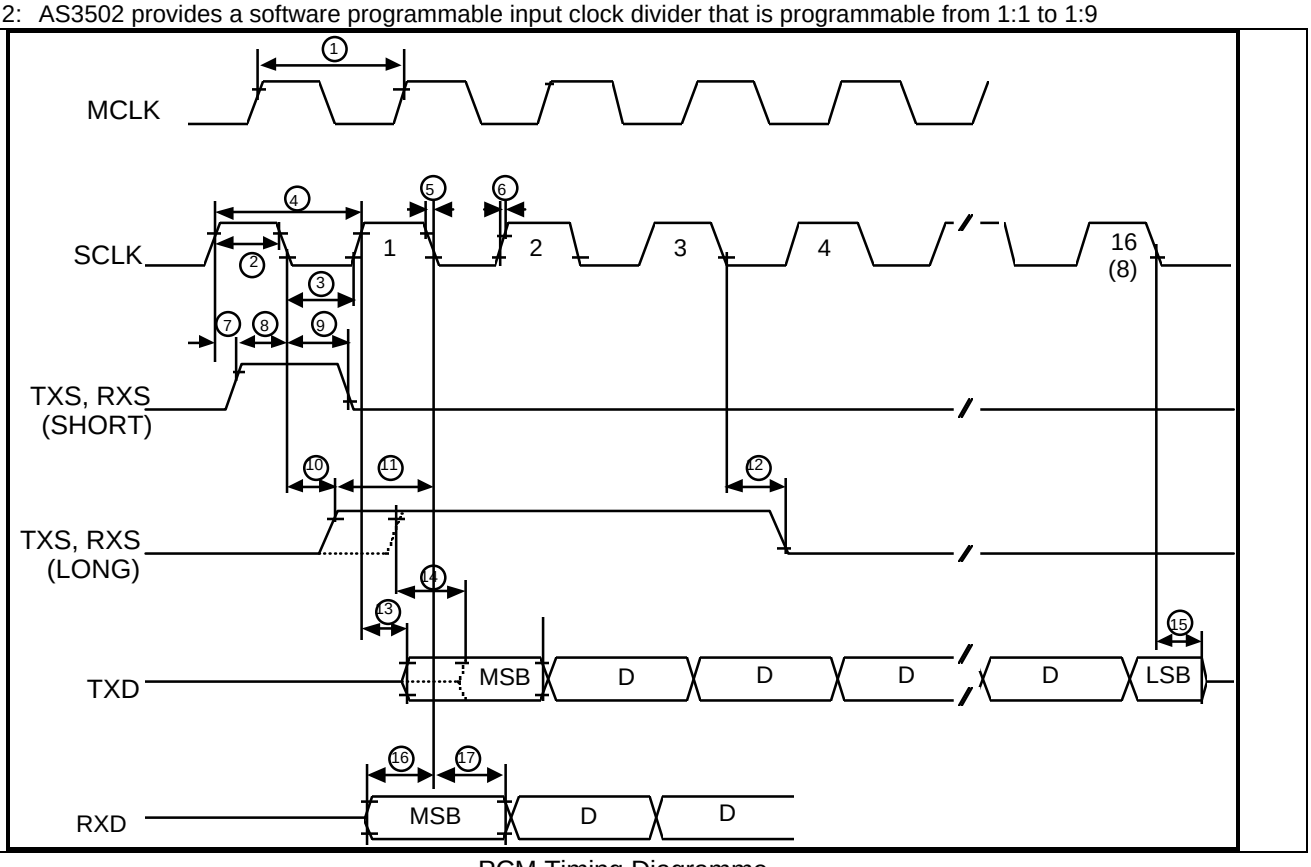
#	Parameter	Symbol	Condition	Min	Typ	Max	Units
1	Frequency of Master Clock	t_{FMCLK}	Note 1, 2	2.048		18.432	MHz
2	Width of SCLK High	t_{WCH}		80			ns
3	Frequency of SCLK	$1/t_C$		64		4096	KHz
4	Width of SCLK Low	t_{WCL}		80			ns
5	Fall Time of SCLK	t_{FC}				30	ns
6	Rise Time of SCLK	t_{RC}				30	ns
7	Hold Time from SCLK High to Short Strobe High	t_{HCSSH}		0			ns
8	Set Up Time from Short Strobe High to SCLK Low	t_{SSSCL}		30			ns

#	Parameter	Symbol	Condition	Min	Typ	Max	Units
9	Hold Time from SCLK Low to Short Strobe Low	t_{HCSSL}		30			ns
10	Hold Time from SCLK Low to Long Strobe High	t_{HCLSH}		0			ns
11	Set Up Time from Long Strobe High to SCLK Low	t_{SLSCL}		30			ns
12	Hold Time from 3rd Period of SCLK Low to Strobe Low	t_{HCLSL}		30			ns
13	Delay Time from SCLK High to TXD Valid	t_{DCD}	C_L= 100 pF + 2 TTL Loads			80	ns
14	Delay Time to Valid Data from TXS or SCLK whichever comes later	t_{DSD}	C_L= 100 pF + 2 TTL Loads			80	ns
15	Delay Time from SCLK or TXS Low to TXD Disabled	t_{DCZ}				80	ns
16	Set Up Time from RXD Valid to SCLK Low	t_{SDC}		30			ns
17	Hold Time from SCLK Low to RXD invalid	t_{HCD}		20			ns
18	Strobe Pulse Frequency	f_{STB}			8		KHz

* Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing

Note 1: A 50:50 duty cycle must be used for 2.048MHz operation

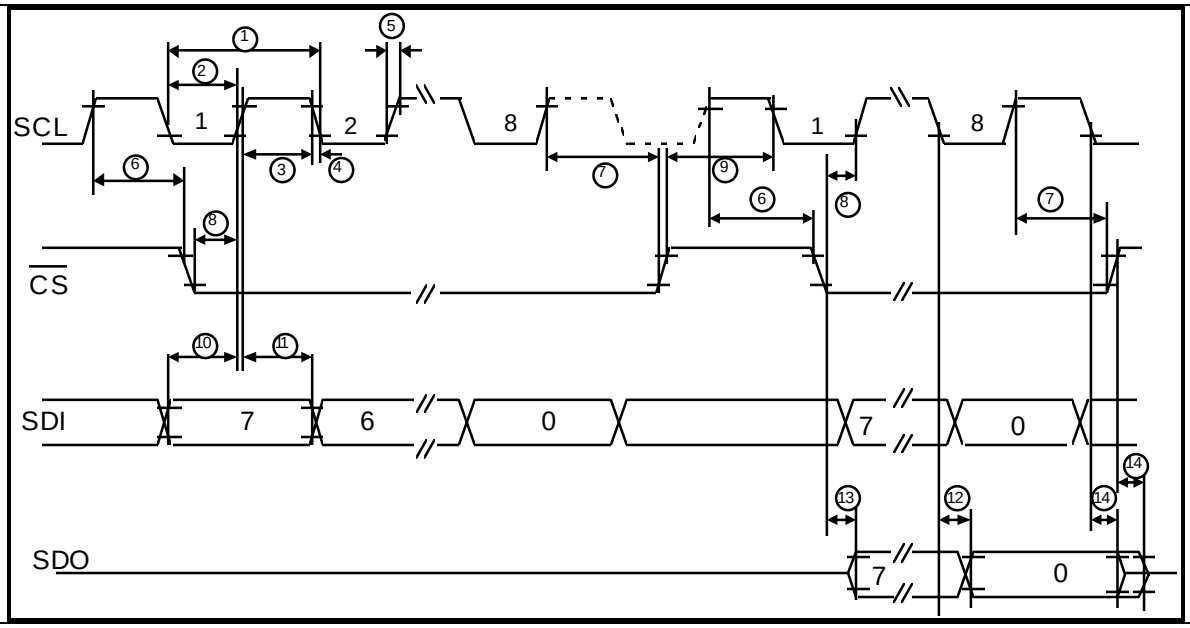
Note 2: AS3502 provides a software programmable input clock divider that is programmable from 1:1 to 1:9



PCM Timing Diagramme

Serial Control Interface Timing (-40°C<TA <+70°C, 3.0 V≤V_{DD}≤4.5 V)

#	Parameter	Symbol	Condition	Min.	Typ.*	Max.	Units
1	Frequency of SCL	f_{SCLK}		128		2048	kHz
2	Width of SCL Low	t_{WCH}		160			ns
3	Width of SCL High	t_{WCL}		160			ns
4	Fall Time of SCL	t_{FC}				50	ns
5	Rise Time of SCL	t_{RC}				50	ns
6	Hold Time from SCL High to /CS Low	t_{HCS}	For 1st SCL	10			ns
7	Hold Time from SCL High to /CS High	t_{HSC}	For 8th SCL	100			ns
8	Set up Time from /CS Transition to SCL High	t_{SSC}		60			ns
9	Setup Time from /CS Transition to SCL Low	t_{SSC0}	SDO is not enabled for a single byte transfer	60			ns
10	Setup Time SDI Data In toSCL High	t_{SDC}		50			ns
11	Hold Time SCL High to SDI Invalid	t_{HCD}		50			ns
12	Delay Time SCL Low to SDO Data Out Valid	t_{DCD}	100pF + 2 LSTTL Loads			80	ns
13	Delay Time from /CS Low to SDO Valid	t_{DSD}	Only valid for dual chip selects			80	ns
14	Delay Time from /CS Low to SDO High Impedance, whichever comes earlier	t_{DDZ}		15		80	ns



Serial Control Interface Timing Diagramme

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Notes