5V µP Power Supply Monitor and Reset Circuit

General Description

The ASM1232LP/LPS is a fully integrated microprocessor supervisor. It can halt and restart a “hung-up” microprocessor, restart a microprocessor after a power failure. It has a watchdog timer and external reset override.

A precision temperature-compensated reference and comparator circuits monitor the 5V, V_{CC} input voltage status. During power-up or when the V_{CC} power supply falls outside selectable tolerance limits, both RESET and $\overline{\text{RESET}}$ become active. When V_{CC} rises above the threshold voltage, the reset signals remain active for an additional 250ms minimum, allowing the power supply and system microprocessor to stabilize. The trip point tolerance signal, TOL, selects the trip level tolerance to be either 5% or 10%.

Each device has both a push-pull, active HIGH reset output and an open drain active LOW reset output. A debounced manual reset input, $\overline{\text{PBRST}}$, activates the reset outputs for a minimum period of 250ms.

There is a watchdog timer to stop and restart a microprocessor that is “hung-up”. The watchdog timeouts periods are selectable: 150ms, 610ms and 1200ms. If the $\overline{\text{ST}}$ input is not strobed LOW before the time-out period expires, a reset is generated.

Devices are available in 8-pin DIP, 16-pin SO and compact 8-pin MicroSO packages.

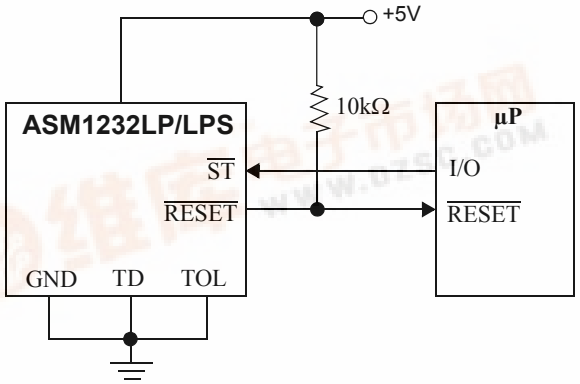
Key Features

- 5V supply monitor
- Selectable watchdog period
- Debounce manual push-button reset input
- Precision temperature-compensated voltage reference and comparator.
- Power-up, power-down and brown out detection
- 250ms minimum reset time
- Active LOW open drain reset output and active HIGH push-pull output
- Selectable trip point tolerance: 5% or 10%
- Low-cost surface mount packages: 8-pin/16-pin SO, 8-pin DIP and 8-pin Micro SO packages
- Wide operating temperature -40°C to +85°C (N suffixed devices)

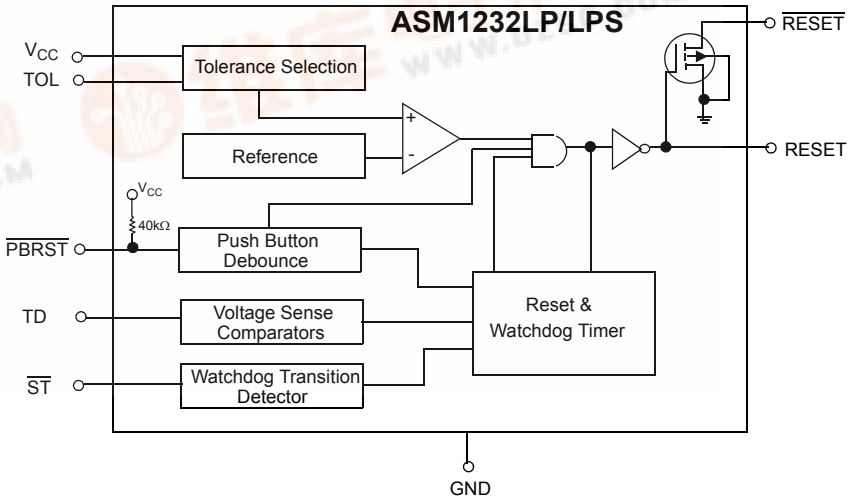
Applications

- Microprocessor Systems
- Computers
- Controllers
- Portable Equipment
- Intelligent Instuments
- Automotive Systems

Typical Operating Circuit

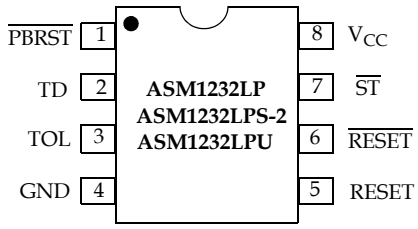


Block Diagram

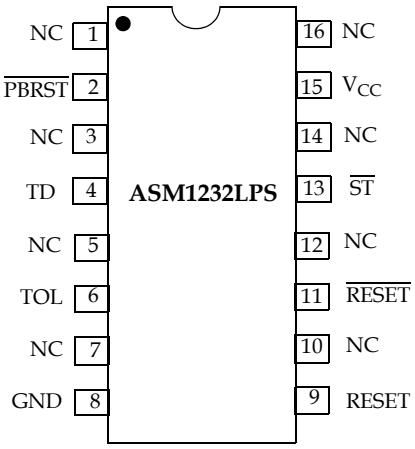


Pin Configuration

DIP/SO/MicroSO



SO



Pin Description

Pin # 8-Pin Package	Pin # 16-Pin Package	Pin Name	Function
1	2	$\overline{\text{PBRST}}$	Debounced manual pushbutton RESET input.
2	4	TD	Watchdog time delay selection. (t_{TD} = 150ms for TD = GND, t_{TD} = 610ms for TD=Open, and t_{TD} = 1200ms for TD = V_{CC}).
3	6	TOL	Selects 5% (TOL connected to GND) or 10% (TOL connected to V_{CC}) trip point tolerance.
4	8	GND	Ground.
5	9	RESET	Active HIGH reset output. RESET is active: 1. If V_{CC} falls below the reset voltage trip point. 2. If $\overline{\text{PBRST}}$ is LOW. 3. If $\overline{\text{ST}}$ is not strobed LOW before the timeout period set by TD expires. 4. During power-up.
6	11	$\overline{\text{RESET}}$	Active LOW reset output. (See RESET).
7	13	$\overline{\text{ST}}$	Strobe input.
8	15	V_{CC}	5V power.
-	1,3,5,7, 10,12,14,16	NC	No internal connection.

Detailed Description

The ASM1232LP/LPS monitors the microprocessor or microcontroller power supply and generates reset signal, both active HIGH and Active LOW, that halt processor operation whenever the power supply voltage levels are outside a predetermined tolerance.

RESET and $\overline{\text{RESET}}$ outputs

RESET is an active HIGH signal developed by a CMOS push-pull output stage and is the logical opposite to $\overline{\text{RESET}}$.

$\overline{\text{RESET}}$ is an active LOW signal. It is developed with an open drain driver. A pull up resistor of typical value 10kΩ to 50kΩ is required to connect with the output.

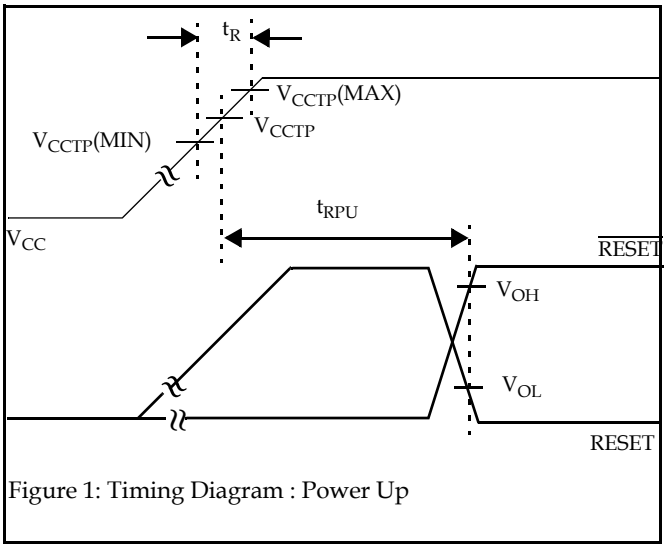


Figure 1: Timing Diagram : Power Up

Trip Point Tolerance Selection

The TOL input is used to determine the level V_{CC} can vary below 5V without asserting a reset. With TOL conected to V_{CC}, RESET and $\overline{\text{RESET}}$ become active whenever V_{CC} falls below 4.5V. RESET and $\overline{\text{RESET}}$ become active when the V_{CC} falls below 4.75V if TOL is connected to ground.

After V_{CC} has risen above the trip point set by TOL, RESET and $\overline{\text{RESET}}$ remain active for a minimum time period of 250ms. On power-down, once V_{CC} falls below the reset threshold RESET stays LOW and is guaranteed to be 0.4V or less until V_{CC} drops below 1.2V. The active HIGH reset signal is valid down to a V_{CC} level of 1.2V also.

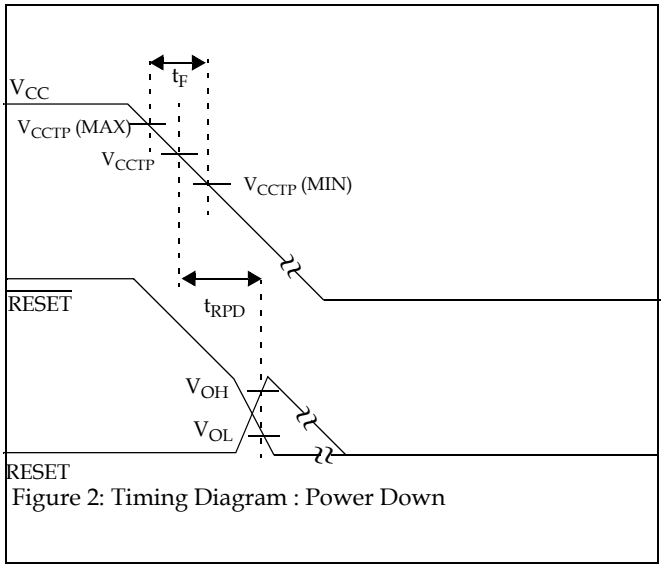


Figure 2: Timing Diagram : Power Down

Tolerance Select	Tolerance	TRIP Point Voltage (V)		
		Min	Nom	Max
TOL = V_{CC}	10%	4.25	4.37	4.49
TOL = GND	5%	4.5	4.62	4.74

Application Information

Manual Reset Operation

Push-button switch input, $\overline{\text{PBRST}}$, allows the user to override the internal trip point detection circuits and issue reset signals. The pushbutton input is debounced and is pulled HIGH through an internal 40kΩ resistor.

When $\overline{PBRST}$ is held LOW for the minimum time t_{PB}, both resets become active and remain active for a minimum time period of 250ms after $\overline{PBRST}$ returns HIGH.

The debounced input is guaranteed to recognize pulses greater than 20ms. No external pull-up resistor is required, since $\overline{PBRST}$ is pulled HIGH by an internal 40kΩ resistor.

The $\overline{PBRST}$ can be driven from a TTL or CMOS logic line or shorted to ground with a mechanical switch.

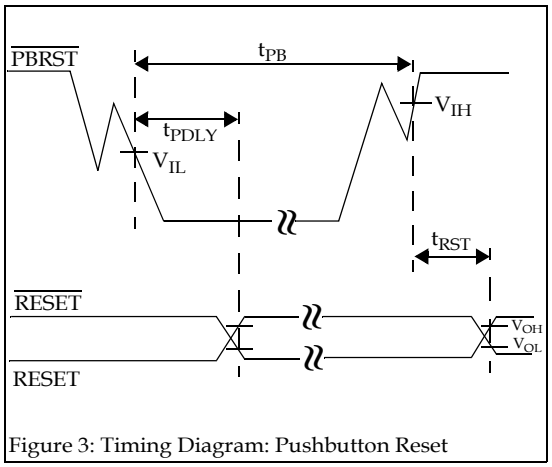


Figure 3: Timing Diagram: Pushbutton Reset

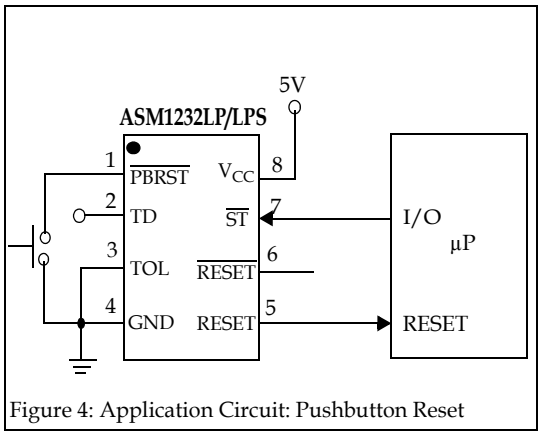
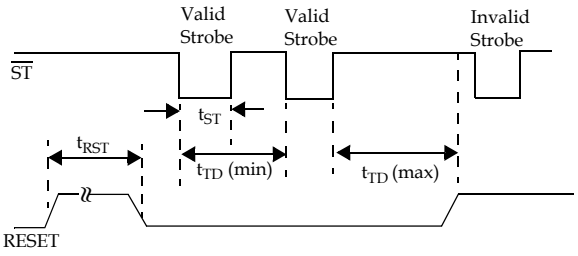


Figure 4: Application Circuit: Pushbutton Reset

Watchdog Timer and $\overline{ST}$ Input

A watchdog timer stops and restarts a microprocessor that is "hung-up". The µP must toggle the $\overline{ST}$ input within a set period (as selectable through TD input) to verify proper software execution. If the $\overline{ST}$ is not toggled low within the minimum timeout period, reset signals become active. In power-up after the supply voltage returns to an in-tolerance condition, the reset signal remains active for 250ms minimum, allowing the power supply and system microprocessor to stabilize. $\overline{ST}$ pulses as short as 20ns can be detected.



Note: $\overline{ST}$ is ignored whenever a reset is active

Figure 5: Timing Diagram: Strobe Input

Timeouts periods of approximately 150ms, 610ms or 1,200ms are selected through the TD pin.

TD Voltage level	Watchdog Time-out Period (ms)		
	Min	Nom	Max
GND	62.5	150	250
Floating	250	610	1000
V_{CC}	500	1200	2000

The watchdog timer can not be disabled. It must be strobed with a high-to-low transition to avoid watchdog timeout and reset.

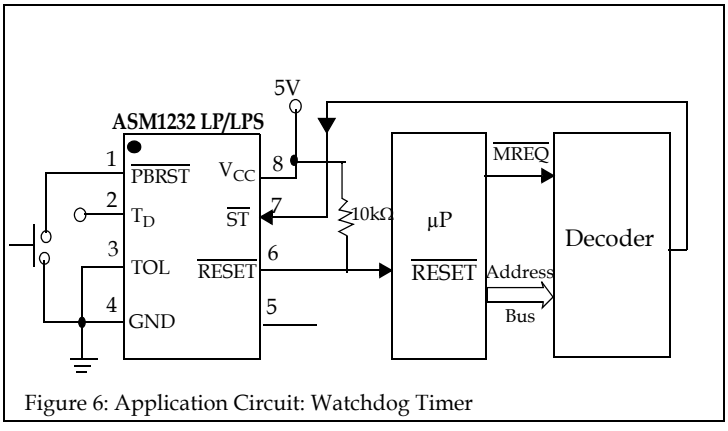


Figure 6: Application Circuit: Watchdog Timer

Absolute Maximum Ratings

Parameter	Min	Max	Unit
Voltage on V_{CC}	-0.5	7	V
Voltage on $\overline{ST}$, TD	-0.5	V_{CC} + 0.5	V
Voltage on $\overline{PBRST}$, RESET, $\overline{RESET}$	-0.5	V_{CC} + 0.5	V
Operating Temperature Range (N suffixed devices)	-40	+85	°C
Operating Temperature Range (others)	0	70	°C
Soldering Temperature (for 10 sec)		+260	°C
Storage Temperature	-55	+125	°C
ESD rating HBM MM		 2 200	 KV V
Note: 1. Voltages are measured with respect to ground 2. These are stress ratings only and functional implication is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.			

DC Electrical Characteristics

Unless otherwise stated, 4.5V <= V_{CC}<= 5.5V and over the operating temperature range of 0°C to 70°C (-40°C to +85°C. for N devices). All voltages are referenced to ground.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{CC}		4.5		5.5	V
$\overline{ST}$ and $\overline{PBRST}$ Input High Level	V_{IH}		2		V_{CC} + 0.3	V
$\overline{ST}$ and $\overline{PBRST}$ Input Low Level	V_{IL}		-0.3		0.8	V
V_{CC} Trip Point (T_{OL} = GND)	V_{CCTP}		4.50	4.62	4.74	V
V_{CC} Trip Point (T_{OL} = V_{CC})	V_{CCTP}		4.25	4.37	4.49	V
Watchdog Timeout Period	t_{TD}	T_D = GND	62.5	150	250	ms
Watchdog Timeout Period	t_{TD}	T_D = VCC	500	1200	2000	ms
Watchdog Timeout Period	t_{TD}	T_D Floating	250	610	1000	ms
Output Voltage	V_{OH}	I=-500µA, Note 3	V_{CC} - 0.5	V_{CC} - 0.1		V
Output Current	I_{OH}	Output = 2.4V, Note 2	-8	-10		mA
Output Current	I_{OL}	Output = 0.4V	10			mA

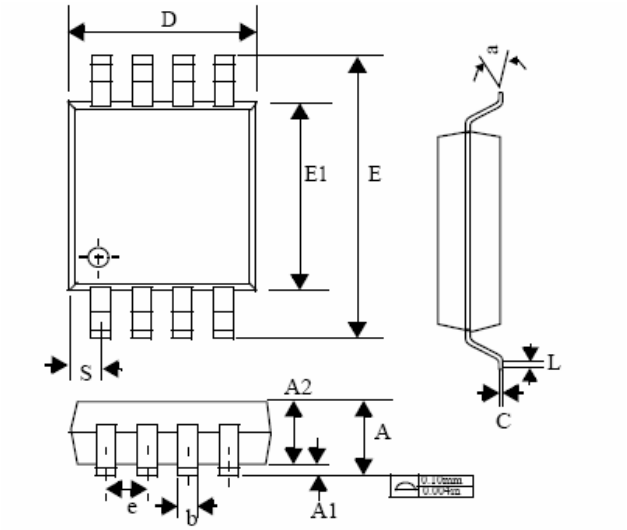
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Leakage	I_{IL}	Note 1	-1.0		1.0	µA
RESET Low Level	V_{OL}	Note 3			0.4	V
Internal Pull-up Resistor		Note 1		40		kΩ
Operating Current (CMOS)	I_{CC1}				30	µA
Input Capacitance	C_{IN}				5	pF
Output Capacitance	C_{OUT}				10	pF
$\overline{PBRST}$ Manual Reset Minimum Low Time	t_{PB}	$\overline{PBRST} = V_{IL}$	20			ms
Reset Active Time	t_{RST}		250	610	1000	ms
$\overline{ST}$ Pulse Width	t_{ST}	Note 4	20			ns
V_{CC} Fail Detect to $\overline{RESET}$ or RESET	t_{RPD}			5	8	µs
V_{CC} Slew Rate	t_F	4.75V to 4.25V	300			µs
$\overline{PBRST}$ Stable LOW to RESET and $\overline{RESET}$ Active	t_{PDLY}				20	ms
V_{CC} Detect to RESET or $\overline{RESET}$ inactive	t_{RPU}	t_{RISE} = 5µs	250	610	1000	ms
V_{CC} Slew Rate	t_R	4.25V to 4.75V	0			ns

Notes

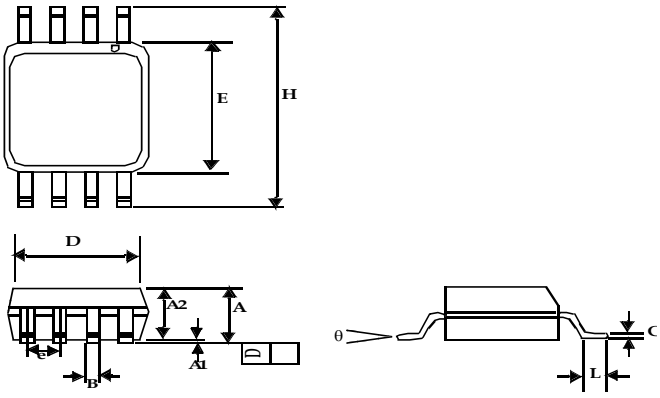
1. $\overline{PBRST}$ is internally pulled HIGH to V_{CC} through a nominal 40kΩ resistor.
2. $\overline{RESET}$ is an open drain output.
3. RESET remains within 0.5V of V_{CC} on power-down until V_{CC} falls below 2V. $\overline{RESET}$ remains within 0.5V of ground on power-down until V_{CC} falls below 2.0V.
4. Must not exceed the minimum watchdog time-out period (t_{TD}). The watchdogcircuit cannot be disabled. To avoid a reset, $\overline{ST}$ must be strobed.

Package Information

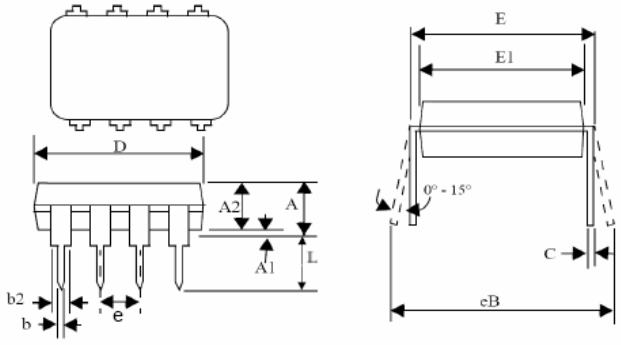
MicroSO (8-Pin)



SO (8-Pin)

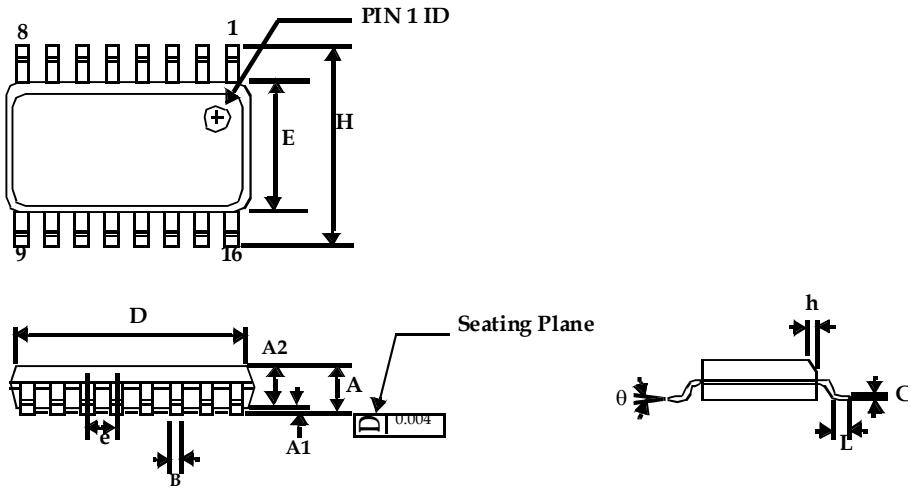


Plastic DIP (8-Pin)



	Inches		Millimeteres	
	Min	Max	Min	Max
MicroSO (8-Pin)				
A	0.032	0.044	0.81	1.10
A1	0.002	0.006	0.05	0.15
A2	0.030	0.038	0.76	0.97
b	0.012 BSC		0.30 BSC	
C	0.004	0.008	0.10	0.20
D	0.114	0.122	2.90	3.10
e	0.0256 BSC		0.65 BSC	
E	0.184	0.200	4.67	5.08
E1	0.114	0.122	2.90	3.10
L	0.016	0.026	0.41	0.66
S	0.0206 BSC		0.52 BSC	
a	0°	6°	0°	6°
SO (8-Pin)				
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
A2	0.049	0.059	1.25	1.50
B	0.012	0.020	0.31	0.51
C	0.007	0.010	0.18	0.25
D	0.193 BSC		4.90 BSC	
E	0.154 BSC		3.91 BSC	
e	0.050 BSC		1.27 BSC	
H	0.236 BSC		6.00 BSC	
L	0.016	0.050	0.41	1.27
θ	0°	8°	0°	8°
Plastic DIP (8-Pin)				
A	-	0.210	-	5.33
A1	0.015	-	0.38	-
A2	0.115	0.195	2.92	4.95
b	0.014	0.022	0.36	0.56
b2	0.045	0.070	1.14	1.78
C	0.008	0.014	0.20	0.36
D	0.355	0.400	9.02	10.16
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
eB	-	0.430	-	10.92
L	0.115	0.150	2.92	3.81

SO (16-Pin)



	SO (16-Pin)*			
	Inches		Millimeter	
	Min	Max	Min	Max
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
A2	0.049	0.059	1.25	1.50
B	0.013	0.022	0.33	0.53
C	0.008	0.012	0.19	0.27
D	0.386	0.394	9.80	10.01
E	0.150	0.157	3.80	4.00
e	0.050 BSC		1.27 BSC	
H	0.228	0.244	5.80	6.20
h	0.010	0.016	0.25	0.41
L	0.016	0.035	0.40	0.89
θ	0°	8°	0°	8°

* JEDEC Drawing MS-013AA

Ordering Information

Part Number	Package	Operating Temperature Range	Maximum Supply Current (µA)	Voltage Monitoring Application	Package Marking
TIN-LEAD DEVICES					
ASM1232LP	8L PDIP	0°C to +70°C	30	5V	ASM1232LP
ASM1232LPN	8L PDIP	-40° C to +85°C	30	5V	ASM1232LPN
ASM1232LPS	16L SOIC	0°C to +70°C	30	5V	ASM1232LPS
ASM1232LPS-2	8L SOIC	0°C to +70° C	30	5V	ASM1232LPS-2
ASM1232LPSN	16L SOIC	-40°C to +85°C	30	5V	ASM1232LPSN
ASM1232LPSN-2	8L SOIC	-40°C to +85°C	30	5V	ASM1232LPSN-2
ASM1232LPU	8L MSOP	0°C to +70°C	30	5V	ASM1232LP
ASM1232LPUN	8L MSOP	-40°C to +85°C	30	5V	ASM1232LPN
LEAD FREE DEVICES					
ASM1232LPF	8L PDIP	0°C to +70°C	30	5V	ASM1232LPF
ASM1232LPNF	8L PDIP	-40°C to +85°C	30	5V	ASM1232LPNF
ASM1232LPS-2F	8L SOIC	0°C to +70°C	30	5V	ASM1232LPS-2F
ASM1232LPSF	16L SOIC	0°C to +70°C	30	5V	ASM1232LPSF
ASM1232LPSN-2F	8L SOIC	-40°C to +85°C	30	5V	ASM1232LPSN-2F
ASM1232LPSNF	16L SOIC	-40°C to +85°C	30	5V	ASM1232LPSNF
ASM1232LPUF	8L MSOP	0°C to +70°C	30	5V	ASM1232LPF
ASM1232LPUNF	8L MSOP	-40°C to +85°C	30	5V	ASM1232LPNF

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