



16-Bit, 1 LSB INL, 3 MSPS PuISAR™ ADC

Preliminary Technical Data

AD7621

FEATURES

- 16 Bits Resolution with No Missing Codes
- No Pipeline Delay (SAR architecture)
- Differential Input Range: $\pm V_{REF}$ (V_{REF} up to 2.5V)
- Throughput:
 - 3 MSPS (Wideband Warp and Warp Mode)
 - 2 MSPS (Normal Mode)
 - 1.25 MSPS (Impulse Mode)
- INL: ± 1 LSB Max ($\pm 0.0015\%$ of Full-Scale)
- S/(N+D): 90 dB Typ @ 100 kHz ($V_{REF} = 2.5V$)
- THD: -100 dB Typ @ 100 kHz
- Parallel (16 or 8bits bus) and Serial 5V/3.3V/2.5V Interface
- SPI/QSPI/MICROWIRE/DSP Compatible
- On-board Low Drift Reference with Buffer and Temperature sensor
- Single 2.5 V Supply Operation
- Power Dissipation: 100 mW Typ @ 3 MSPS
- Power-Down Mode
- Package: 48-Lead Quad Flat Pack (LQFP)
- 48-Lead Frame Chip Scale Package (LFCSP)
- Speed Upgrade of the AD7677

APPLICATIONS

- Medical Instruments
- High Speed Data Acquisition
- Communications
- Instrumentation
- Spectrum Analysis
- ATE

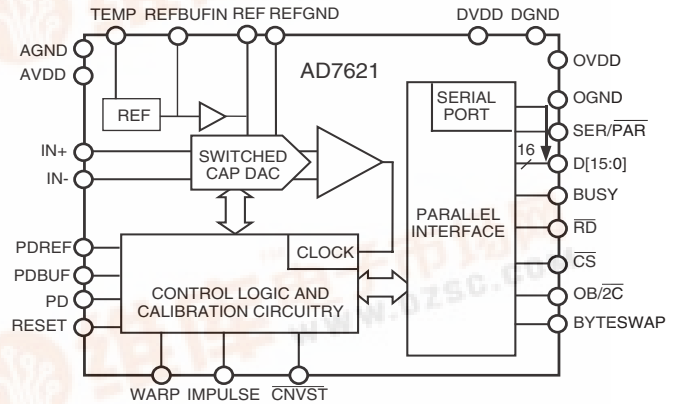
GENERAL DESCRIPTION

The AD7621 is a 16-bit, 3 MSPS, charge redistribution SAR, fully differential analog-to-digital converter that operates from a single 2.5 V power supply. The part contains a high-speed 16-bit sampling ADC, an internal conversion clock, an internal reference buffer, error correction circuits, and both serial and parallel system interface ports.

It features a very high sampling rate mode (Wideband Warp) for undersampling applications and, for asynchronous conversion rate applications, a fast mode (Normal) and, for low power applications, a reduced power mode (Impulse) where the power is scaled with the throughput.

It is available in a 48-lead LQFP or a 48-lead LFCSP with operation specified from -40°C to $+85^{\circ}\text{C}$.

FUNCTIONAL BLOCK DIAGRAM



PuISAR Selection

Type / kSPS	100 - 250	500 - 570	800 - 1000	>1000
Pseudo Differential	AD7651 AD7660/61	AD7650/52 AD7664/66	AD7653 AD7667	
True Bipolar	AD7663	AD7665	AD7671	
True Differential	AD7675	AD7676	AD7677	AD7621
18 Bit	AD7678	AD7679	AD7674	
Multichannel/ Simultaneous		AD7654	AD7655	

PRODUCT HIGHLIGHTS

1. High resolution and Fast Throughput
The AD7621 is a 3 MSPS, charge redistribution, 16-bit SAR ADC (no latency).
2. Excellent accuracy
The AD7621 has a maximum integral nonlinearity of 1 LSB with no missing 16-bit code.
3. Single-Supply Operation
The AD7621 operates from a single 2.5 V supply and typically dissipates only 100 mW. In impulse mode, its power dissipation decreases with the throughput and it features a power-down mode.
5. Serial or Parallel Interface
Versatile parallel (16 or 8 bits bus) or 2-wire serial interface arrangement compatible with either 2.5V, 3.3V or 5 V logic.

REV. Pr. D

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PRELIMINARY TECHNICAL DATA

AD7621—SPECIFICATIONS (-40°C to +85°C, $V_{REF} = AVDD$, $AVDD = DVDD = OVDD = 2.5 V$, unless otherwise noted.)

Parameter	Conditions	Min	Typ	Max	Unit
RESOLUTION		16			Bits
ANALOG INPUT					
Voltage Range	$V_{IN+} - V_{IN-}$	$-V_{REF}$		$+V_{REF}$	V
Operating Input Voltage	V_{IN+}, V_{IN-} to AGND	-0.1		AVDD	V
Analog Input CMRR	$f_{IN} = \text{TBD kHz}$		TBD		dB
Input Current	TBD MSPS Throughput		TBD		μA
Input Impedance			See Analog Input Section		
THROUGHPUT SPEED					
Complete Cycle	In WideBand Warp Mode			333	ns
Throughput Rate	In Wideband Warp Mode	0.1		3	MSPS
Throughput Rate	In Warp Mode	0.001		3	MSPS
Time Between Conversions	In Warp Mode			1	ms
Complete Cycle	In Normal Mode			500	ns
Throughput Rate	In Normal Mode	0		2	MSPS
Complete Cycle	In Impulse Mode			800	ns
Throughput Rate	In Impulse Mode	0		1.25	MSPS
DC ACCURACY					
Integral Linearity Error		-1	± 1	+1	LSB ¹
Differential Linearity Error		-1		+1	LSB
No Missing Codes		16			Bits
Transition Noise	$V_{REF} = AVDD$		0.7		LSB
Gain Error, T_{MIN} to T_{MAX} ²				$\pm \text{TBD}$	% of FSR
Gain Error Temperature Drift			$\pm \text{TBD}$		ppm/ $^{\circ}C$
Zero Error, T_{MIN} to T_{MAX} ²			$\pm \text{TBD}$	$\pm \text{TBD}$	LSB
Zero Error Temperature Drift			$\pm \text{TBD}$		ppm/ $^{\circ}C$
Power Supply Sensitivity	$AVDD = 2.5V \pm 5\%$		$\pm \text{TBD}$		LSB
AC ACCURACY					
Signal-to-Noise	$f_{IN} = 100 \text{ kHz}$, $V_{REF} = AVDD$	88	90		dB ³
	$V_{REF} = 2.048V$		88.3		dB
Spurious Free Dynamic Range	$f_{IN} = 100 \text{ kHz}$		100		dB
Total Harmonic Distortion	$f_{IN} = 100 \text{ kHz}$		-100		dB
Signal-to-(Noise+Distortion)	$f_{IN} = 100 \text{ kHz}$,		90		dB
	$f_{IN} = 100 \text{ kHz}, -60 \text{ dB Input}$		30		dB
-3 dB Input Bandwidth			50		MHz
SAMPLING DYNAMICS					
Aperture Delay			1		ns
Aperture Jitter			TBD		ps rms
Transient Response	Full-Scale Step			50	ns
Overshoot recovery				50	ns
REFERENCE					
External Reference Voltage Range	REF	TBD	2.048	AVDD	V
REF Current Drain	3 MSPS Throughput		TBD		μA
REF Voltage with reference buffer	REFBUFIN=1.2V	2	2.048	2.1	V
Reference Buffer Input Voltage	REFBUFIN	TBD	1.2	TBD	V
REFBUFIN Input Current		-1		+1	μA
INTERNAL REFERENCE					
Internal Reference Voltage	@ 25°C	TBD	1.2	TBD	V
Internal Reference Temp Drift	-40°C to +85°C		TBD		ppm/ $^{\circ}C$
Internal Reference Temp Drift	0°C to +70°C		TBD		ppm/ $^{\circ}C$
REFBUFIN Line Regulation	$AVDD = 2.5V \pm 5\%$		TBD		ppm/V
REFBUFIN Output Resistance			16		k Ω
Power Supply Rejection	@ TBD kHz		TBD		dB
Turn-on Settling Time			TBD		μs
Long-term Stability	1,000 Hours		TBD		ppm
Hysteresis			TBD		ppm
REFBUFIN Output Resistance			TBD		k Ω
Temperature Pin Voltage Output	@ 25°C		313		mV
Temperature Sensitivity			1		mV/ $^{\circ}C$
TEMP pin Output Resistance			4.3		k Ω

PRELIMINARY TECHNICAL DATA

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Parameter	Conditions	Min	Typ	Max	Unit
DIGITAL INPUTS					
Logic Levels					
V_{IL}		-0.3		+0.6	V
V_{IH}		+1.7		5.25	V
I_{IL}		-1		+1	μ A
I_{IH}		-1		+1	μ A
DIGITAL OUTPUTS					
Data Format		Parallel or Serial 16-Bits			
Pipeline Delay		Conversion Results Available Immediately After Completed Conversion			
V_{OL}	$I_{SINK} = 500 \mu A$			0.4	V
V_{OH}	$I_{SOURCE} = -500 \mu A$	OVDD - 0.3			V
POWER SUPPLIES					
Specified Performance					
AVDD		2.37	2.5	2.63	V
DVDD		2.37	2.5	2.63	V
OVDD		2.3		3.6	V
Operating Current ⁴					
AVDD	3 MSPS Throughput		15		mA
DVDD ⁵			4.5		mA
OVDD ⁵			130		μ A
Power Dissipation ⁵					
	PDBUF high @ 3 MSPS ⁴		100	TBD	mW
	PDBUF low @ 3 MSPS ⁴		108	TBD	mW
	PDBUF high @ 1.25 MSPS ⁶		TBD	TBD	mW
	PDBUF low @ 1.25 MSPS ⁶		TBD	TBD	mW
	In Power-Down Mode ⁷		TBD	TBD	μ W
TEMPERATURE RANGE⁸					
Specified Performance					
	T_{MIN} to T_{MAX}	-40		+85	°C

NOTES

¹LSB means Least Significant Bit. With the ± 2.5 V input range, one LSB is 76.294 μ V.

²See Definition of Specifications section. These specifications do not include the error contribution from the external reference.

³All specifications in dB are referred to a full-scale input FS. Tested with an input signal at 0.5 dB below full-scale unless otherwise specified.

⁴In warp mode.

⁵Tested in parallel reading mode.

⁶In impulse mode.

⁷With all digital inputs forced to DVDD or DGND respectively.

⁸Contact factory for extended temperature range.

Specifications subject to change without notice.

TIMING SPECIFICATIONS

(-40°C to +85°C, AVDD = DVDD = 2.5 V, OVDD = 2.3 V to 3.6 V, unless otherwise noted.)

	Symbol	Min	Typ	Max	Unit
REFER TO FIGURES 12 AND 13					
Convert Pulsewidth	t_1	5			ns
Time Between Conversions (Warp Mode/Normal Mode/Impulse Mode)	t_2	333/500/800		Note 1	ns
\overline{CNVST} LOW to BUSY HIGH Delay	t_3			30	ns
BUSY HIGH All Modes Except in Master Serial Read After Convert (Warp Mode/Normal Mode/Impulse Mode)	t_4			263/400/750	ns
Aperture Delay	t_5		1		ns
End of Conversion to BUSY LOW Delay	t_6	10			ns
Conversion Time (Warp Mode/Normal Mode/Impulse Mode)	t_7			263/400/750	ns
Acquisition Time (Warp Mode/Normal Mode/Impulse Mode)	t_8	70/100/50			ns
RESET Pulsewidth	t_9	10			ns
REFER TO FIGURES 14, 15, AND 16 (Parallel Interface Modes)					
\overline{CNVST} LOW to Data Valid Delay (Warp Mode/Normal Mode/Impulse Mode)	t_{10}			263/400/750	ns
Data Valid to BUSY LOW Delay	t_{11}	20			ns
Bus Access Request to Data Valid	t_{12}			40	ns
Bus Relinquish Time	t_{13}	2		15	ns

PRELIMINARY TECHNICAL DATA

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TIMING SPECIFICATIONS (continued)

	Symbol	Min	Typ	Max	Unit
REFER TO FIGURES 18 AND 19 (Master Serial Interface Modes) ²					
\overline{CS} LOW to SYNC Valid Delay	t ₁₄			TBD	ns
\overline{CS} LOW to Internal SCLK Valid Delay	t ₁₅			TBD	ns
\overline{CS} LOW to SDOUT Delay	t ₁₆			TBD	ns
\overline{CNVST} LOW to SYNC Delay (Warp Mode/Normal Mode/Impulse Mode)	t ₁₇		TBD		ns
SYNC Asserted to SCLK First Edge Delay ³	t ₁₈	TBD			ns
Internal SCLK Period ³	t ₁₉	TBD		TBD	ns
Internal SCLK HIGH ³	t ₂₀	TBD			ns
Internal SCLK LOW ³	t ₂₁	TBD			ns
SDOUT Valid Setup Time ³	t ₂₂	TBD			ns
SDOUT Valid Hold Time ³	t ₂₃	TBD			ns
SCLK Last Edge to SYNC Delay ³	t ₂₄	TBD			ns
\overline{CS} HIGH to SYNC HI-Z	t ₂₅			TBD	ns
\overline{CS} HIGH to Internal SCLK HI-Z	t ₂₆			TBD	ns
\overline{CS} HIGH to SDOUT HI-Z	t ₂₇			TBD	ns
BUSY HIGH in Master Serial Read after Convert ³	t ₂₈		See Table I		ns
\overline{CNVST} LOW to SYNC Asserted Delay (Warp Mode/Normal Mode/Impulse Mode)	t ₂₉		TBD		ns
SYNC Deasserted to BUSY LOW Delay	t ₃₀		TBD		ns
REFER TO FIGURES 20 AND 22 (Slave Serial Interface Modes)					
External SCLK Setup Time	t ₃₁	5			ns
External SCLK Active Edge to SDOUT Delay	t ₃₂	2		7	ns
SDIN Setup Time	t ₃₃	TBD			ns
SDIN Hold Time	t ₃₄	TBD			ns
External SCLK Period	t ₃₅	12.5			ns
External SCLK HIGH	t ₃₆	5			ns
External SCLK LOW	t ₃₇	5			ns

NOTES

¹In warp mode only, the maximum time between conversions is 1ms; otherwise, there is no required maximum time.

²In serial interface modes, the SYNC, SCLK, and SDOUT timings are defined with a maximum load C_L of 10 pF; otherwise, the load is 60 pF maximum.

³In serial master read during convert mode. See Table I for serial master read after convert mode.

Specifications subject to change without notice.

Table I. Serial clock timings in Master Read after Convert

DIVSCLK[1] DIVSCLK[0]	Symbol	Mode				unit
		0	0	1	1	
SYNC to SCLK First Edge Delay Minimum	t ₁₈	TBD	TBD	TBD	TBD	ns
Internal SCLK Period minimum	t ₁₉	TBD	TBD	TBD	TBD	ns
Internal SCLK Period Maximum	t ₁₉	TBD	TBD	TBD	TBD	ns
Internal SCLK HIGH Minimum	t ₂₀	TBD	TBD	TBD	TBD	ns
Internal SCLK LOW Minimum	t ₂₁	TBD	TBD	TBD	TBD	ns
SDOUT Valid Setup Time Minimum	t ₂₂	TBD	TBD	TBD	TBD	ns
SDOUT Valid Hold Time Minimum	t ₂₃	TBD	TBD	TBD	TBD	ns
SCLK Last Edge to SYNC Delay Minimum	t ₂₄	TBD	TBD	TBD	TBD	ns
Busy High Width Maximum (Warp)	t ₂₈	TBD	TBD	TBD	TBD	ns
Busy High Width Maximum (Normal)	t ₂₈	TBD	TBD	TBD	TBD	ns
Busy High Width Maximum (Impulse)	t ₂₈	TBD	TBD	TBD	TBD	ns

PRELIMINARY TECHNICAL DATA

AD7621

ABSOLUTE MAXIMUM RATINGS¹

Analog Inputs

IN⁺², IN⁻², REF, REFBUF_{IN}, TEMP, REF_{GND} to
AGND AVDD + 0.3 V to AGND - 0.3 V

Ground Voltage Differences

AGND, DGND, OGND ±0.3 V

Supply Voltages

AVDD, DVDD -0.3V to +2.7 V

OVDD -0.3V to +3.8 V

Digital Inputs -0.3 V to 5.5V

Internal Power Dissipation³ 700 mW

Internal Power Dissipation⁴ 2.5W

Junction Temperature 150°C

Storage Temperature Range -65°C to +150°C

Lead Temperature Range

(Soldering 10 sec) 300°C

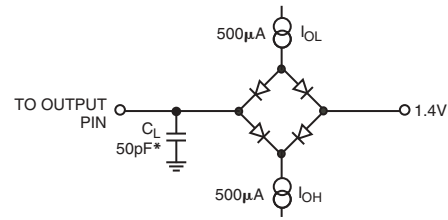
NOTES

¹Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

²See Analog Input section.

³Specification is for device in free air: 48-Lead LQFP: $\theta_{JA} = 91^{\circ}\text{C}/\text{W}$, $\theta_{JC} = 30^{\circ}\text{C}/\text{W}$.

⁴Specification is for device in free air: 48-Lead LFCSP: $\theta_{JA} = 26^{\circ}\text{C}/\text{W}$.



*IN SERIAL INTERFACE MODES, THE SYNC, SCLK, AND SDOUT TIMINGS ARE DEFINED WITH A MAXIMUM LOAD C_L OF 10pF; OTHERWISE, THE LOAD IS 50pF MAXIMUM.

Figure 1. Load Circuit for Digital Interface Timing, SDOUT, SYNC, SCLK Outputs, $C_L = 10\text{ pF}$

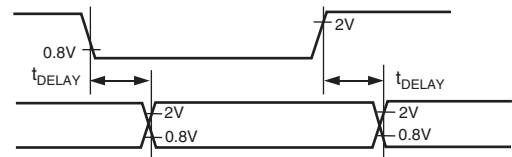


Figure 2. Voltage Reference Levels for Timing

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD7621AST	-40°C to +85°C	Quad Flatpack (LQFP)	ST-48
AD7621ASTRL	-40°C to +85°C	Quad Flatpack (LQFP)	ST-48
AD7621ACP	-40°C to +85°C	Chip Scale (LFCSP)	CP-48
AD7621ACPRL	-40°C to +85°C	Chip Scale (LFCSP)	CP-48
EVAL-AD7621CB ¹		Evaluation Board	
EVAL-CONTROL BRD3 ²		Controller Board	

NOTES

¹This board can be used as a standalone evaluation board or in conjunction with the EVAL-CONTROL BRD3 for evaluation/demonstration purposes.

²This board allows a PC to control and communicate with all Analog Devices evaluation boards ending in the CB designators.

CAUTION

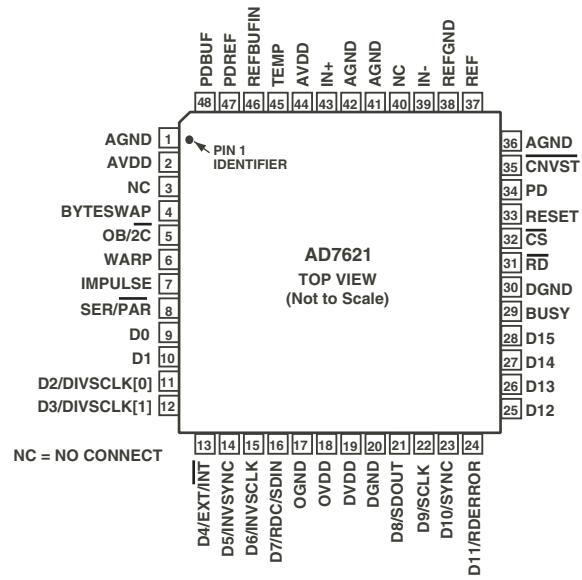
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7621 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PRELIMINARY TECHNICAL DATA

AD7621

PIN CONFIGURATION 48-Lead LQFP and 48-Lead LFCSP (ST-48 and CP-48)



PRELIMINARY TECHNICAL DATA

AD7621

PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Type	Description
1, 41, 42	AGND	P	Analog Power Ground Pin.
2, 44	AVDD	P	Input Analog Power Pins. Nominally 2.5 V.
3, 40	NC		No Connect.
4	BYTESWAP	DI	Parallel Mode Selection (8-bit/16-bit). When LOW, the LSB is output on D[7:0] and the MSB is output on D[15:8]. When HIGH, the LSB is output on D[15:8] and the MSB is output on D[7:0].
5	OB/ $\overline{2C}$	DI	Straight Binary/Binary Two's Complement. When OB/ $\overline{2C}$ is HIGH, the digital output is straight binary; when LOW, the MSB is inverted resulting in a two's complement output from its internal shift register.
6	WARP	DI	Conversion mode selection. When HIGH and IMPULSE LOW, this input selects the fastest mode, the maximum throughput is achievable, and a minimum conversion rate must be applied in order to guarantee full specified accuracy. When LOW, full accuracy is maintained independent of the minimum conversion rate.
7	IMPULSE	DI	Conversion mode selection. When HIGH and WARP LOW, this input selects a reduced power mode. In this mode, the power dissipation is approximately proportional to the sampling rate.
8	SER/ \overline{PAR}	DI	Serial/Parallel Selection Input. When LOW, the parallel port is selected; when HIGH, the serial interface is selected and some bits of the data bus are used as a serial port.
9, 10	D[0:1]	DO	Bit 0 and Bit 1 of the parallel port data output bus. When SER/ \overline{PAR} is HIGH, these outputs are in high impedance.
11,12	D[2:3]or DIVSCLK[0:1]	DI/O	When SER/ \overline{PAR} is LOW, these pins are Bit 2 and Bit 3 of the Parallel Port Data Output Bus. When SER/ \overline{PAR} is HIGH, EXT/ \overline{INT} is LOW, and RDC/SDIN is LOW, which is serial master read after convert, these inputs, part of the serial port, are used to slow down if desired the internal serial clock which clocks the data output. In other serial modes, these pins are high impedance outputs.
13	D4 or EXT/ \overline{INT}	DI/O	When SER/ \overline{PAR} is LOW, this output is used as Bit 4 of the Parallel Port Data Output Bus. When SER/ \overline{PAR} is HIGH, this input, part of the serial port, is used as a digital select input for choosing the internal or an external data clock. With EXT/ \overline{INT} tied LOW, the internal clock is selected on SCLK output. With EXT/ \overline{INT} set to a logic HIGH, output data is synchronized to an external clock signal connected to the SCLK input.
14	D5 or INVSYNC	DI/O	When SER/ \overline{PAR} is LOW, this output is used as Bit 5 of the Parallel Port Data Output Bus. When SER/ \overline{PAR} is HIGH, this input, part of the serial port, is used to select the active state of the SYNC signal. When LOW, SYNC is active HIGH. When HIGH, SYNC is active LOW.
15	D6 or INVCLK	DI/O	When SER/ \overline{PAR} is LOW, this output is used as Bit 6 of the Parallel Port Data Output Bus. When SER/ \overline{PAR} is HIGH, this input, part of the serial port, is used to invert the SCLK signal. It is active in both master and slave mode.
16	D7 or RDC/SDIN	DI/O	When SER/ \overline{PAR} is LOW, this output is used as Bit 7 of the Parallel Port Data Output Bus. When SER/ \overline{PAR} is HIGH, this input, part of the serial port, is used as either an external data input or a read mode selection input depending on the state of EXT/ \overline{INT} . When EXT/ \overline{INT} is HIGH, RDC/SDIN could be used as a data input to daisy chain the conversion results from two or more ADCs onto a single SDOUT line. The digital data level on SDIN is output on SDOUT with a delay of 16 SCLK periods after the initiation of the read sequence. When EXT/ \overline{INT} is LOW, RDC/SDIN is used to select the read mode. When RDC/SDIN is HIGH, the data is output on SDOUT during conversion. When RDC/SDIN is LOW, the data can be output on SDOUT only when the conversion is complete.
17	OGND	P	Input/Output Interface Digital Power Ground.
18	OVDD	P	Input/Output Interface Digital Power. Nominally at the same supply than the supply

PRELIMINARY TECHNICAL DATA

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Pin No.	Mnemonic	Type	Description
19	DVDD	P	of the host interface (2.5 V or 3 V). Digital Power. Nominally at 2.5 V.
20	DGND	P	Digital Power Ground.
21	D8 or SDOUT	D O	When $\overline{\text{SER/PA}}\overline{\text{R}}$ is LOW, this output is used as Bit 8 of the Parallel Port Data Output Bus. When $\overline{\text{SER/PA}}\overline{\text{R}}$ is HIGH, this output, part of the serial port, is used as a serial data output synchronized to SCLK. Conversion results are stored in an on-chip register. The AD7621 provides the conversion result, MSB first, from its internal shift register. The data format is determined by the logic level of $\text{OB}/\overline{\text{2C}}$. In serial mode, when $\overline{\text{EXT/INT}}$ is LOW, SDOUT is valid on both edges of SCLK. In serial mode, when $\overline{\text{EXT/INT}}$ is HIGH: If INVSCLK is LOW, SDOUT is updated on SCLK rising edge and valid on the next falling edge. If INVSCLK is HIGH, SDOUT is updated on SCLK falling edge and valid on the next rising edge.
22	D9 or SCLK	DI/O	When $\overline{\text{SER/PA}}\overline{\text{R}}$ is LOW, this output is used as the Bit 9 of the Parallel Port Data Output Bus. When $\overline{\text{SER/PA}}\overline{\text{R}}$ is HIGH, this pin, part of the serial port, is used as a serial data clock input or output, dependent upon the logic state of the $\overline{\text{EXT/INT}}$ pin. The active edge where the data SDOUT is updated depends upon the logic state of the INVSCLK pin.
23	D10 or SYNC	D O	When $\overline{\text{SER/PA}}\overline{\text{R}}$ is LOW, this output is used as the Bit 10 of the Parallel Port Data Output Bus. When $\overline{\text{SER/PA}}\overline{\text{R}}$ is HIGH, this output, part of the serial port, is used as a digital output frame synchronization for use with the internal data clock ($\overline{\text{EXT/INT}}$ = Logic LOW). When a read sequence is initiated and INVS $\overline{\text{SYNC}}$ is LOW, SYNC is driven HIGH and remains HIGH while SDOUT output is valid. When a read sequence is initiated and INVS $\overline{\text{SYNC}}$ is HIGH, SYNC is driven LOW and remains LOW while SDOUT output is valid.
24	D11 or RDERROR	D O	When $\overline{\text{SER/PA}}\overline{\text{R}}$ is LOW, this output is used as the Bit 11 of the Parallel Port Data Output Bus. When $\overline{\text{SER/PA}}\overline{\text{R}}$ is HIGH and when $\overline{\text{EXT/INT}}$ is HIGH, this output, part of the serial port, is used as an incomplete read error flag. In slave mode, when a data read is started and not complete when the following conversion is complete, the current data is lost and RDERROR is pulsed high.
25–28	D[12:15]	D O	Bit 12 to Bit 15 of the Parallel Port Data output bus. These pins are always outputs regard less of the interface mode.
29	BUSY	D O	Busy Output. Transitions HIGH when a conversion is started, and remains HIGH until the conversion is complete and the data is latched into the on-chip shift register. The falling edge of BUSY could be used as a data ready clock signal.
30	DGND	P	Must be tied to digital ground.
31	$\overline{\text{RD}}$	DI	Read Data. When $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are both LOW, the interface parallel or serial output bus is enabled.
32	$\overline{\text{CS}}$	DI	Chip Select. When $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are both LOW, the interface parallel or serial output bus is enabled. $\overline{\text{CS}}$ is also used to gate the external clock.
33	RESET	DI	Reset Input. When set to a logic HIGH, reset the AD7621. Current conversion if any is aborted. If not used, this pin could be tied to DGND.
34	PD	DI	Power-Down Input. When set to a logic HIGH, power consumption is reduced and conversions are inhibited after the current one is completed.
35	$\overline{\text{CNVST}}$	DI	Start Conversion. A falling edge on $\overline{\text{CNVST}}$ puts the internal sample/hold into the hold state and initiates a conversion. In impulse mode (IMPULSE HIGH and WARP LOW), if $\overline{\text{CNVST}}$ is held LOW when the acquisition phase (t_a) is complete, the internal sample/hold is put into the hold state and a conversion is immediately started.
36	AGND	P	Must be tied to analog ground.
37	REF	AI	Reference Input Voltage and Internal Reference Buffer Output. Apply an external reference on this pin if the internal reference buffer is not used. Should be decoupled effectively with or without the internal buffer.
38	REFGND	AI	Reference Input Analog Ground.

PRELIMINARY TECHNICAL DATA

AD7621

Pin No.	Mnemonic	Type	Description
39	IN-	AI	Differential Negative Analog Input.
43	IN+	AI	Differential Negative Analog Input.
45	TEMP	AO	Temperature sensor analog output typically 1mV/°C.
46	REFBUFIN	AI	Internal Reference Output and Reference Buffer Input Voltage. The internal reference buffer has a fixed gain. It outputs 2.048V typically when 1.2V is applied on this pin.
47	PDREF	DI	Allows choice of Internal or External voltage reference. When HIGH, the internal reference is switched off and an external reference must be used. When LOW, the on-chip reference is turned on.
48	PDBUF	DI	Allows choice of buffering reference. When LOW, the buffer is selected. When HIGH, the buffer is switched off.

NOTES

AI = Analog Input

AI/O = Bidirectional Analog

AO = Analog Output

DI = Digital Input

DI/O = Bidirectional Digital

DO = Digital Output

P = Power

PRELIMINARY TECHNICAL DATA

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DEFINITION OF SPECIFICATIONS

Integral nonlinearity error (INL)

Linearity error refers to the deviation of each individual code from a line drawn from “negative full scale” through “positive full scale”. The point used as “negative full scale” occurs 1/2 LSB before the first code transition. “Positive full scale” is defined as a level 1 1/2 LSB beyond the last code transition. The deviation is measured from the middle of each code to the true straight line.

Differential nonlinearity error (DNL)

In an ideal ADC, code transitions are 1 LSB apart. Differential nonlinearity is the maximum deviation from this ideal value. It is often specified in terms of resolution for which no missing codes are guaranteed.

Gain error

The first transition (from 000...00 to 000...01) should occur for an analog voltage 1/2 LSB above the nominal – full scale (-2.047962 V for the ±2.048V range). The last transition (from 111...10 to 111...11) should occur for an analog voltage 1 1/2 LSB below the nominal full scale (2.047886 V for the ±2.048V range). The gain error is the deviation of the difference between the actual level of the last transition and the actual level of the first transition from the difference between the ideal levels.

Zero error

The zero error is the difference between the ideal midscale input voltage (0 V) and the actual voltage producing the midscale output code.

Spurious free dynamic range (SFDR)

The difference, in decibels (dB), between the rms amplitude of the input signal and the peak spurious signal.

Effective number of bits (ENOB)

ENOB is a measurement of the resolution with a sine wave input. It is related to S/(N+D) by the following formula:

$$\text{ENOB} = (S/[N+D]_{\text{dB}} - 1.76)/6.02$$

and is expressed in bits.

Total harmonic distortion (THD)

THD is the ratio of the rms sum of the first five harmonic components to the rms value of a full-scale input signal and is expressed in decibels.

Dynamic range

Dynamic range is the ratio of the rms value of the full scale to the rms noise measured with the inputs shorted together. The value for dynamic range is expressed in decibels.

Signal-to-noise ratio (SNR)

SNR is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics and dc. The value for SNR is expressed in decibels.

Signal to (noise + distortion) ratio (S/[N+D])

S/(N+D) is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for S/(N+D) is expressed in decibels.

Aperture delay

Aperture delay is a measure of the acquisition performance and is measured from the falling edge of the CNVST input to when the input signal is held for a conversion.

Transient response

The time required for the AD7621 to achieve its rated accuracy after a full-scale step function is applied to its input.

Reference Voltage Temperature Coefficient

The change of the internal reference output voltage V over the operating temperature range and normalized by the output voltage at 25°C, expressed in ppm/°C. The equation follows:

$$TCV(\text{ppm}/^\circ\text{C}) = \frac{V(T_2) - V(T_1)}{V(25^\circ\text{C}) \times (T_2 - T_1)} \times 10^6$$

where

V(25°C) = V at 25°C

V(T₂) = V at Temperature 2

V(T₁) = V at Temperature 1

Reference Voltage Long-Term Stability

Typical shift of output voltage at 25°C on a sample of parts subjected to operation life test of 1000 hours at 125°C:

$$\Delta V(\text{ppm}) = \frac{V(t_1) - V(t_0)}{V(t_0)} \times 10^6$$

where

V(t₀) = V at 25°C at Time 0

V(t₁) = V at 25°C after 1,000 hours operation at 125°C

Reference Voltage Thermal Hysteresis

Thermal hysteresis is defined as the change of output voltage after the device is cycled through temperature from +25°C to -40°C to +125°C and back to +25°C. This is a typical value from a sample of parts put through such a cycle

$$V_{\text{HYS}}(\text{ppm}) = \frac{V_{\text{TC}} - V(25^\circ\text{C})}{V(25^\circ\text{C})} \times 10^6$$

where

V(25°C) = V at 25°C

V_{TC} = V at 25°C after temperature cycle at +25°C to -40°C to +125°C and back to +25°C

PRELIMINARY TECHNICAL DATA

Typical Performance Characteristics- AD7621

To Be Supplied

TPC 1. Integral Nonlinearity vs. Code

To Be Supplied

TPC 4. Differential Nonlinearity vs. Code

To Be Supplied

TPC 2. Histogram of 131,072 Conversions of a DC Input at the Code Transition

To Be Supplied

TPC 5. Histogram of 131,072 Conversions of a DC Input at the Code Center

To Be Supplied

TPC 3. Typical Positive INL Distribution (TBD Units)

To Be Supplied

TPC 6. Typical Negative INL Distribution (TBD Units)

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To Be Supplied

TPC 7. Typical INL and DNL vs Temperature

To Be Supplied

TPC 10. Typical INL and DNL vs Sampling rate

To Be Supplied

TPC 8. FFT

To Be Supplied

TPC 11. SNR, S/(N+D) and ENOB vs. Frequency

To Be Supplied

TPC 9. FFT

To Be Supplied

TPC 12. THD, SFDR and Harmonics vs. Frequency

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To Be Supplied

TPC 13. SNR, S/(N+D) and THD vs. Input Level

To Be Supplied

TPC 16. Operating Current vs. Sampling Rate

To Be Supplied

TPC 14. SNR, S/(N+D) and ENOB vs Temperature

To Be Supplied

TPC 17. Power-Down Operating Currents vs. Temperature

To Be Supplied

TPC 15. THD, SFDR and Harmonics vs Temperature

To Be Supplied

TPC 18. Positive and Negative Full Scale, Offset and Reference Buffer Gain vs. Temperature

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To Be Supplied

TPC 19. Positive and Negative Full Scale, Offset and Reference Buffer Gain vs. Supply .

To Be Supplied

TPC 22. Typical Internal Reference Temperature Drift Distribution (TBD Units)

To Be Supplied

TPC 20. Typical Delay vs. Load Capacitance CL

To Be Supplied

TPC 23. Typical Internal Reference Hysteresis Distribution (TBD Units)

To Be Supplied

TPC 21. Typical Internal Reference voltage vs. Tem-

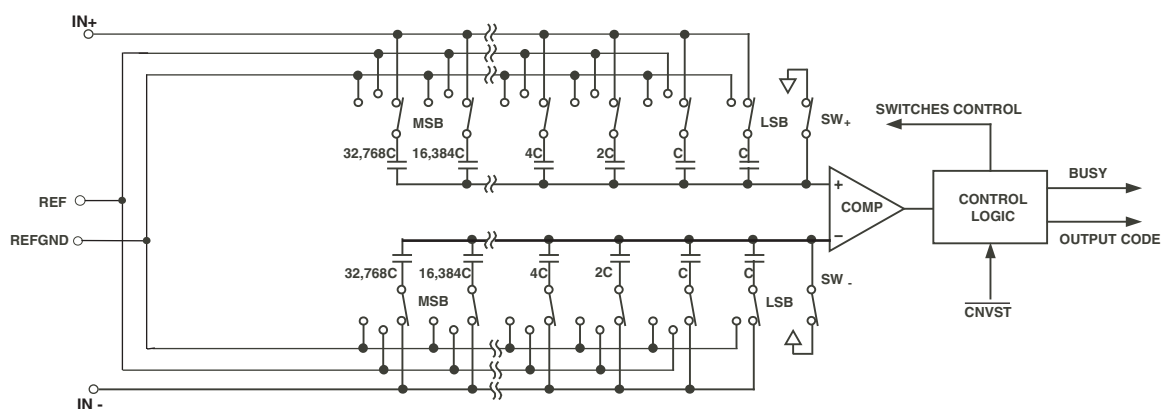


Figure 3. ADC Simplified Schematic

CIRCUIT INFORMATION

The AD7621 is a very fast, low-power, single-supply, precise 16-bit analog-to-digital converter (ADC) using successive approximation architecture.

The AD7621 features different modes to optimize performances according to the applications.

In Warp mode, the AD7621 is capable of converting 3,000,000 samples per second (3 MSPS).

The AD7621 provides the user with an on-chip track/hold, successive approximation ADC that does not exhibit any pipeline or latency, making it ideal for multiple multiplexed channel applications.

The AD7621 can be operated from a single 2.5 V supply and be interfaced to either 5 V or 3.3 V or 2.5 V digital logic. It is housed in a 48-lead LQFP or a tiny LFCSP packages that combines space savings and allows flexible configurations as either serial or parallel interface. The AD7621 is pin-to-pin-compatible with the AD7674.

CONVERTER OPERATION

The AD7621 is a successive approximation analog-to-digital converter based on a charge redistribution DAC. Figure 3 shows the simplified schematic of the ADC. The capacitive DAC consists of two identical arrays of 16 binary weighted capacitors which are connected to the two comparator inputs.

During the acquisition phase, terminals of the array tied to the comparator's input are connected to AGND via SW₊ and SW₋. All independent switches are connected to the analog inputs. Thus, the capacitor arrays are used as sampling capacitors and acquire the analog signal on IN₊ and IN₋ inputs. When the acquisition phase is complete and the CNVST input goes low, a conversion phase is initiated. When the conversion phase begins, SW₊ and SW₋ are opened first. The two capacitor arrays are then discon-

nected from the inputs and connected to the REFVDD input. Therefore, the differential voltage between the inputs IN₊ and IN₋ captured at the end of the acquisition phase is applied to the comparator inputs, causing the comparator to become unbalanced. By switching each element of the capacitor array between REFVDD or REFVSS, the comparator input varies by binary weighted voltage steps ($V_{REF}/2$, $V_{REF}/4$. . . $V_{REF}/65536$). The control logic toggles these switches, starting with the MSB first, in order to bring the comparator back into a balanced condition. After the completion of this process, the control logic generates the ADC output code and brings BUSY output low.

Modes of Operation

The AD7621 features three modes of operations, Warp, Normal, and Impulse. Each of these modes is more suitable for specific applications.

The Warp mode allows the fastest conversion rate up to 3 MSPS. However, in this mode, and this mode only, the full specified accuracy is guaranteed only when the time between conversion does not exceed 1 ms. If the time between two consecutive conversions is longer than 1 ms, for instance, after power-up, the first conversion result should be ignored. This mode makes the AD7621 ideal for applications where fast sample rate are required.

The normal mode is the fastest mode (2 MSPS) without any limitation about the time between conversions. This mode makes the AD7621 ideal for asynchronous applications such as data acquisition systems, where both high accuracy and fast sample rate are required.

The impulse mode, the lowest power dissipation mode, allows power saving between conversions. The maximum throughput in this mode is 1.25 MSPS. This feature makes the AD7621 ideal for battery-powered applications.

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Transfer Functions

Using the $OB/\overline{2C}$ digital input, the AD7621 offers two output codings: straight binary and two's complement. The ideal transfer characteristic for the AD7621 is shown in Figure 4 and Table III.

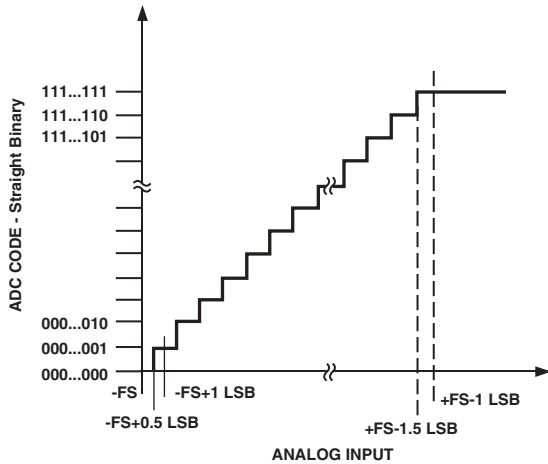


Figure 4. ADC Ideal Transfer Function

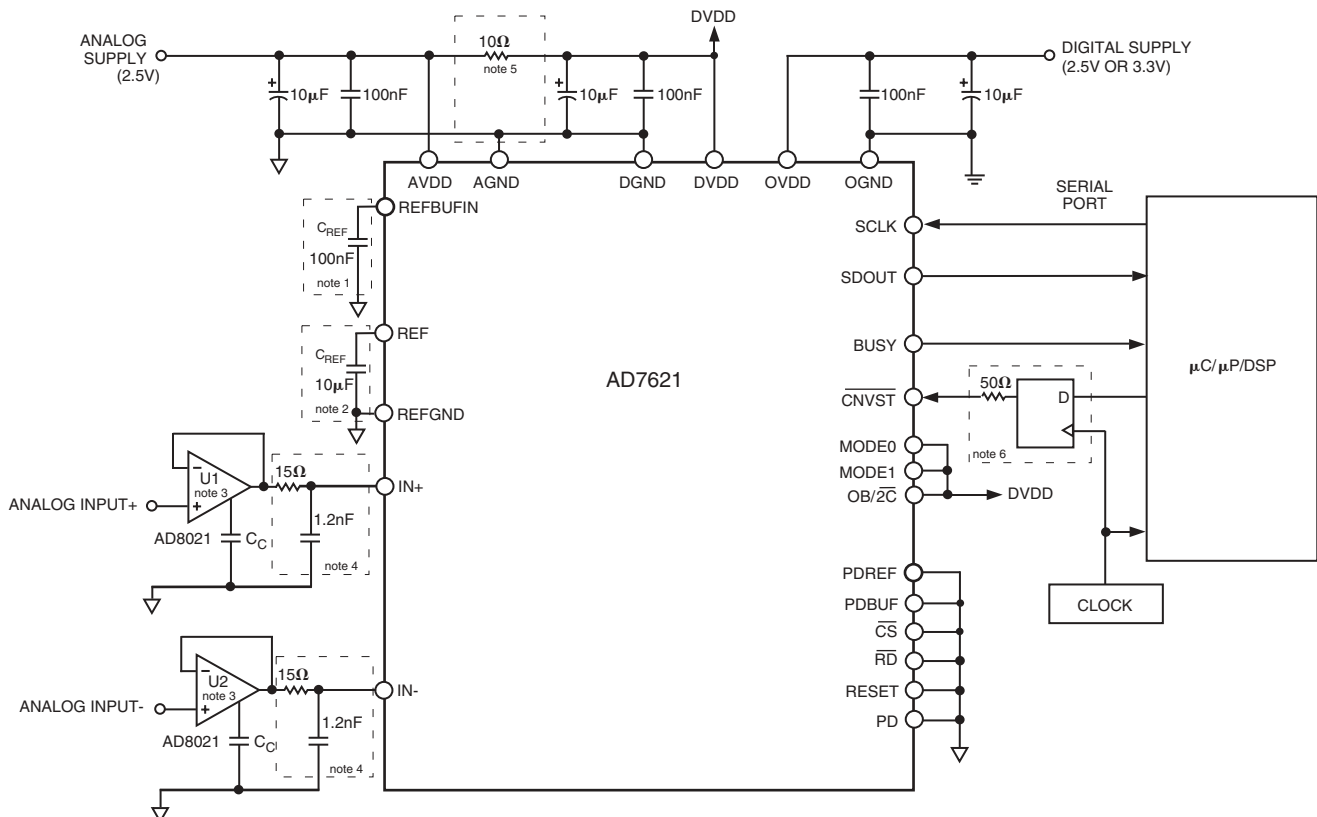
Table III. Output Codes and Ideal Input Voltages

Description	Digital Output Code		
	Analog Input $V_{REF} = 2.048V$	Straight Binary	Two's Complement
FSR - 1 LSB	2.047924 V	3FFFF ¹	1FFFF ¹
FSR - 2 LSB	2.047849 V	3FFFE	1FFE
Midscale + 1 LSB	75.684 μ V	20001	00001
Midscale	0 V	20000	00000
Midscale - 1 LSB	-75.684 μ V	1FFFF	3FFFF
-FSR + 1 LSB	-2.047924 V	00001	20001
-FSR	-2.048 V	00000 ²	20000 ²

NOTES

¹This is also the code for overrange analog input ($V_{IN+} - V_{IN-}$ above $V_{REF} - V_{REFGND}$).

²This is also the code for underrange analog input ($V_{IN+} - V_{IN-}$ below $-V_{REF} + V_{REFGND}$).



NOTES :

Note 1 : See Voltage Reference Input Section.

Note 2 : C_{REF} is 10 μ F ceramic capacitor or low esr tantalum. Ceramic size 1206 Panasonic ECJ-3xB0J106 is recommended. See Voltage Reference Input Section.

Note 3 : The AD8021 is recommended. See Driver Amplifier Choice Section.

Note 4 : See Analog Inputs Section.

Note 5 : Option. See Power Supply Section.

TYPICAL CONNECTION DIAGRAM

Figure 5 shows a typical connection diagram for the AD7621. Different circuitry shown on this diagram are optional and are discussed below.

Analog Inputs

Figure 6 shows a simplified analog input section of the AD7621.

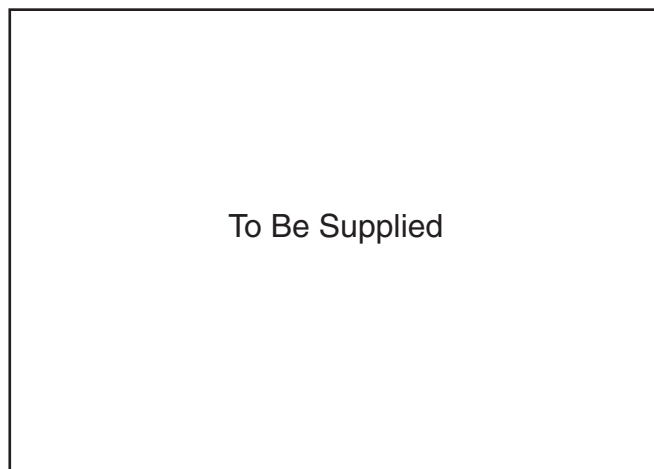


Figure 6. AD7621 simplified Analog Input.

The diodes shown in Figure 6 provide ESD protection for the inputs. Care must be taken to ensure that the analog input signal never exceeds the absolute ratings on these inputs. This will cause these diodes to become forward-biased and start conducting current. These diodes can handle a forward-biased current of 150 mA maximum. This condition could eventually occur when the input buffer's (U1) or (U2) supplies are different from AVDD. In such case, an input buffer with a short-circuit current limitation can be used to protect the part.

This analog input structure is a true differential structure. By using these differential inputs, signals common to both inputs are rejected as shown in Figure 7 which represents the typical CMRR over frequency.

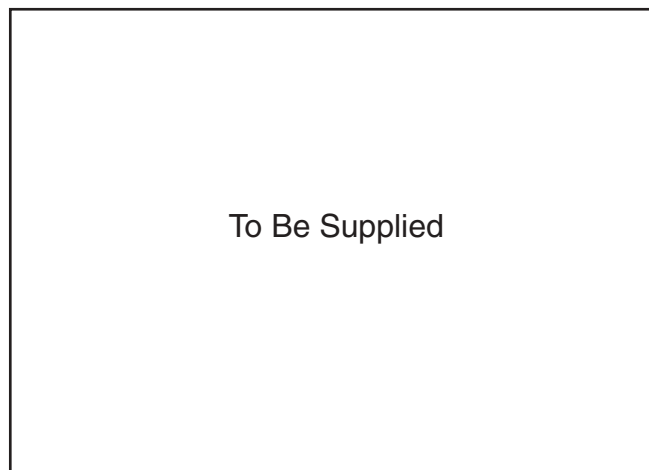


Figure 7. Analog Input CMRR vs. Frequency

During the acquisition phase, for AC signals, the AD7621 behaves like a one pole RC filter consisted of the equivalent resistance R^+ , R^- and C_S . The resistors R^+ and R^- are typically TBD Ω and are lumped component made up of some serial resistor and the on resistance of the switches. The capacitor C_S is typically TBD pF and is mainly the ADC sampling capacitor. This one pole filter with a typical -3dB cutoff frequency of 50 MHz reduces undesirable aliasing effect and limits the noise coming from the inputs.

Because the input impedance of the AD7621 is very high, the AD7621 can be driven directly by a low impedance source without gain error. That allows to put, as shown in Figure 5, an external one-pole RC filter between the output of the amplifier output and the ADC analog inputs to even further improve the noise filtering done by the AD7621 analog input circuit. However, the source impedance has to be kept low because it affects the ac performances, especially the total harmonic distortion. The maximum source impedance depends on the amount of total harmonic distortion (THD) that can be tolerated. The THD degrades as a function of the source impedance and the maximum input frequency.

Driver Amplifier Choice

Although the AD7621 is easy to drive, the driver amplifier needs to meet at least the following requirements:

- The driver amplifier and the AD7621 analog input circuit have to be able together to settle for a full-scale step the capacitor array at a 16-bit level (0.0015%). In the amplifier's datasheet, the settling at 0.1% or 0.01% is more commonly specified. It could significantly differ from the settling time at 16 bit level and, therefore, it should be verified prior to the driver selection. The tiny op-amp AD8021 which combines ultra low noise and a high gain bandwidth meets this settling time requirement.

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- The noise generated by the driver amplifier needs to be kept as low as possible in order to preserve the SNR and transition noise performance of the AD7621. The noise coming from the driver is filtered by the AD7621 analog input circuit one-pole low-pass filter made by R_+ , R_- and C_S . The SNR degradation due to the amplifier is :

$$SNR_{LOSS} = 20 \text{LOG} \left(\frac{56}{\sqrt{3136 + \pi^2 f_{-3dB}^2 (Ne_N)^2}} \right),$$

where :

f_{-3dB} is the -3dB input bandwidth in MHz of the AD7621 (50 MHz) or the cutoff frequency of the input filter if any used

N is the noise factor of the amplifiers (1 if in buffer configuration)

e_N is the equivalent input noise voltage of each op-amp in $nV/(Hz)^{1/2}$

For instance, a driver with an equivalent input noise of $2nV/\sqrt{Hz}$ like the AD8021 and configured as a buffer, thus with a noise gain of +1, the SNR degrades by only 0.17 dB with the filter in figure 5, and 0.8 dB without.

- The driver needs to have a THD performance suitable to that of the AD7621.

The [AD8021](#) meets these requirements and is usually appropriate for almost all applications. The AD8021 needs an external compensation capacitor of 10 pF. This capacitor should have good linearity as an NPO ceramic or mica type.

The [AD8022](#) could also be used where dual version is needed and gain of 1 is used.

Single to Differential Driver

For applications using unipolar analog signals, a single-ended to differential driver will allow for a differential input into the part. The schematic is shown in Figure 8. This configuration, when provided an input signal of 0 to V_{REF} , will produce a differential $\pm V_{REF}$ with midscale at $V_{REF}/2$.

If the application can tolerate more noise, the AD8138, differential driver, can be used.

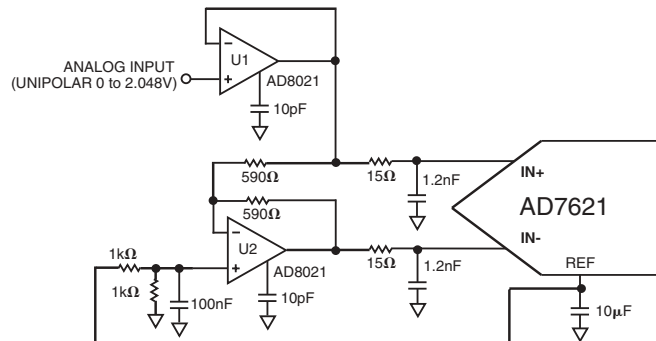


Figure 8. Single Ended to Differential Driver Circuit (internal reference buffer used)

Voltage Reference

The AD7621 allows the choice of either a very low temperature drift internal voltage reference or an external reference.

Unlike many ADC with internal reference, the internal reference of the AD7621 provides excellent performances and can be used in almost all applications. It is temperature compensated to $1.2V \pm TBD$ mV with a typical drift of TBD ppm/°C, a typical long-term stability of TBD ppm and a typical hysteresis of TBD ppm.

However, the advantages to use the external reference voltage directly are :

- The power saving of about 8mW typical when the internal reference and its buffer are powered down (PDREF and PDBUF High)
- The SNR and dynamic range improvement of about 1.7 dB resulting of the use of a reference voltage very close to the supply (2.5V) instead of a typical 2.048V reference when the internal buffer is used.

To use the internal reference along with the internal buffer, PDREF and PDBUF should both be LOW. This will produce a voltage on REFBUFIN of 1.2 V and the buffer will gain it up, resulting in a 2.048 V reference on REF pin.

It is useful to decouple the REFBUFIN pin with a 100 nF ceramic capacitor. The output impedance of the REFBUFIN pin is 16 kΩ. Thus, the 100 nF capacitor provides an RC filter for noise reduction.

To use an external reference along with the internal buffer, PDREF should be HIGH and PDBUF should be low. This powers down the internal reference and allows for the 1.2 V reference to be applied to REFBUFIN.

To use an external reference directly on REF pin, PDREF and PDBUF should both be HIGH.

It should be noted that the internal reference and internal buffer are independent of the power down (PD) pin of the part. Furthermore, powering up the internal reference and internal buffer requires time due to the charge of the REF decoupling.

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In both cases, the voltage reference input REF has a dynamic input impedance and requires, therefore, an efficient decoupling between REF and REFGND inputs. When the internal reference buffer is used, this decoupling consists of a 10 μF ceramic capacitor (e.g. : Panasonic ECJ-3xB0J106 1206 size).

When external reference is used, the decoupling consists of a low ESR 47 μF tantalum capacitor connected to the REF and REFGND inputs with minimum parasitic inductance.

Temperature Sensor

The TEMP pin, which measures the temperature of the AD7621, can be used as shown in figure 9. The output of the TEMP pin is applied to one of the inputs of the analog switch (e.g. : ADG779) and the ADC itself is used to measure its own temperature. This configuration could be very useful to improve the calibration accuracy over the temperature range.

To Be Supplied

Figure 9. Use of the Temperature Sensor

Power Supply

The AD7621 uses three sets of power supply pins: an analog 2.5 V supply AVDD, a digital 2.5 V core supply DVDD, and a digital input/output interface supply OVDD. The OVDD supply allows direct interface with any logic working between 2.3 V and 5.25 V. To reduce the number of supplies needed, the digital core (DVDD) can be supplied through a simple RC filter from the analog supply as shown in Figure 5. The AD7621 is independent of power supply sequencing and thus free from supply voltage induced latchup. Additionally, it is very insensitive to power supply variations over a wide frequency range as shown in Figure 10.

To Be Supplied

Figure 10. PSRR vs. Frequency

POWER DISSIPATION vs. THROUGHPUT

In Impulse mode, the AD7621 automatically reduces its power consumption at the end of each conversion phase. During the acquisition phase, the operating currents are very low which allows a significant power saving when the conversion rate is reduced as shown in Figure 11. This feature makes the AD7621 ideal for very low-power battery applications.

It should be noted that the digital interface remains active even during the acquisition phase. To reduce the operating digital supply currents even further, the digital inputs need to be driven close to the power rails (i.e., DVDD and DGND).

To Be Supplied

Figure 11. Power Dissipation vs. Sample Rate

AD7621

CONVERSION CONTROL

Figure 12 shows the detailed timing diagrams of the conversion process. The AD7621 is controlled by the signal $\overline{\text{CNVST}}$ which initiates conversion. Once initiated, it cannot be restarted or aborted, even by the power-down input PD, until the conversion is complete. The $\overline{\text{CNVST}}$ signal operates independently of $\overline{\text{CS}}$ and $\overline{\text{RD}}$ signals.

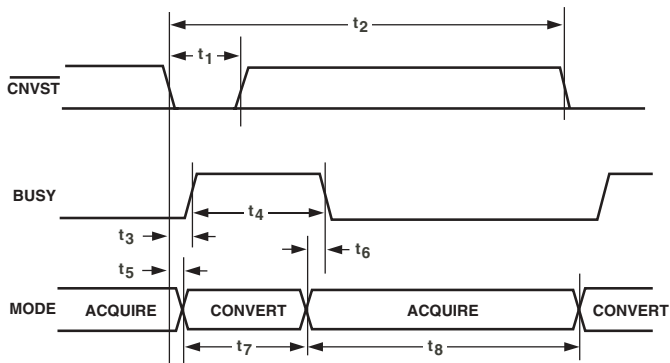


Figure 12. Basic Conversion Timing

Although $\overline{\text{CNVST}}$ is a digital signal, it should be designed with this special care with fast, clean edges and levels, with minimum overshoot and undershoot or ringing.

For applications where the SNR is critical, the $\overline{\text{CNVST}}$ signal should have a very low jitter. Some solutions to achieve that are to use a dedicated oscillator for $\overline{\text{CNVST}}$ generation or, at least, to clock it with a high frequency low jitter clock as shown in Figure 5.

In impulse mode, conversions can be automatically initiated. If $\overline{\text{CNVST}}$ is held low when BUSY is low, the AD7621 controls the acquisition phase and then automatically initiates a new conversion. By keeping $\overline{\text{CNVST}}$ low, the AD7621 keeps the conversion process running by itself. It should be noted that the analog input has to be settled when BUSY goes low. Also, at power-up, $\overline{\text{CNVST}}$ should be brought low once to initiate the conversion process. In this mode, the AD7621 could sometimes run slightly faster than the guaranteed limits in the impulse mode. This feature does not exist in warp or normal modes.

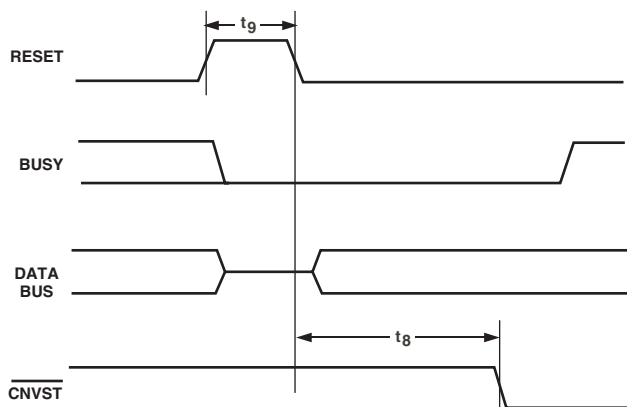


Figure 13. RESET Timing

DIGITAL INTERFACE

The AD7621 has a versatile digital interface; it can be interfaced with the host system by using either a serial or parallel interface. The serial interface is multiplexed on the parallel data bus. The AD7621 digital interface also accommodates both 2.5V, 3.3V or 5V logic with either OVDD at 2.5V or 3.3V. OVDD defines the logic high output voltage. In most applications, the OVDD supply pin of the AD7621 is connected to the host system interface 2.5V or 3.3V digital supply. Finally, by using the $\text{OB}/\overline{2\text{C}}$ input pin, both two's complement or straight binary coding can be used.

The two signals $\overline{\text{CS}}$ and $\overline{\text{RD}}$ control the interface. When at least one of these signals is high, the interface outputs are in high impedance. Usually, $\overline{\text{CS}}$ allows the selection of each AD7621 in multi-circuits applications and is held low in a single AD7621 design. $\overline{\text{RD}}$ is generally used to enable the conversion result on the data bus.

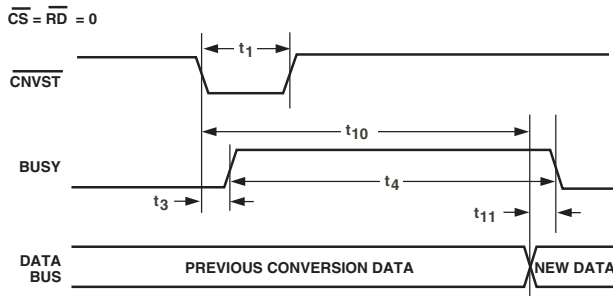


Figure 14. Master Parallel Data Timing for Reading (Continuous Read)

PARALLEL INTERFACE

The AD7621 is configured to use the parallel interface with either a 16-bit or 8-bit bus width. The data can be read either after each conversion, which is during the next acquisition phase, or during the following conversion as shown, respectively, in Figure 15 and Figure 16. When the data is read during the conversion, however, it is recommended that it is read only during the first half of the conversion phase. That avoids any potential feedthrough between voltage transients on the digital interface and the most critical analog conversion circuitry.

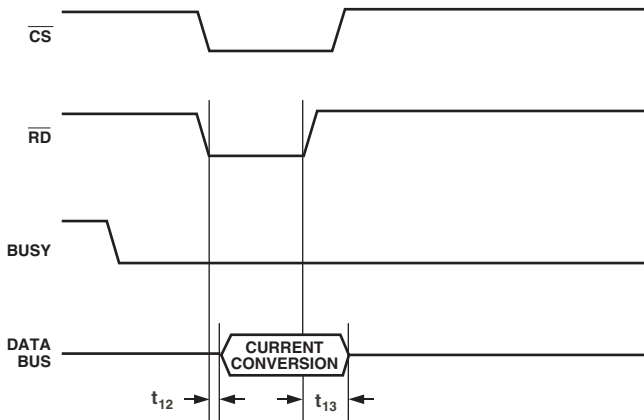


Figure 15. Slave Parallel Data Timing for Reading (Read After Convert)

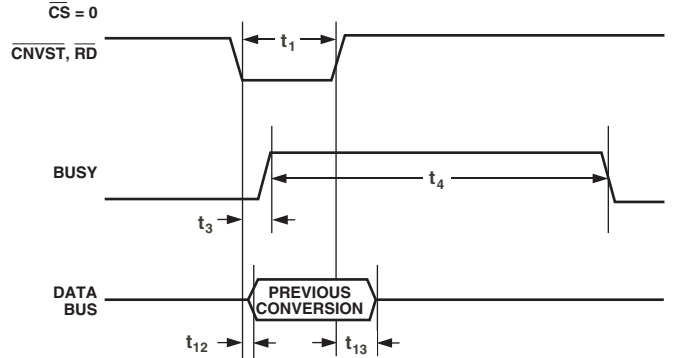


Figure 16. Slave Parallel Data Timing for Reading (Read During Convert)

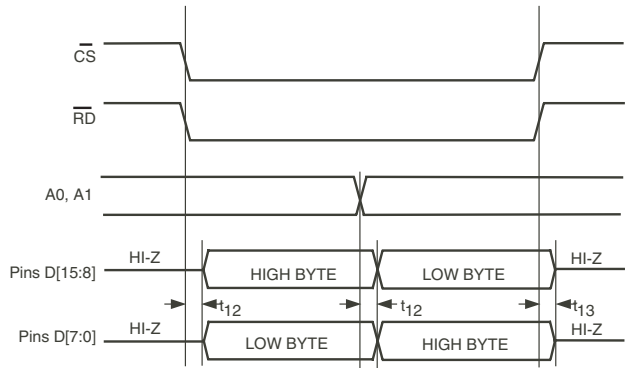


Figure 17. 8-Bit and 16-Bit Parallel Interface

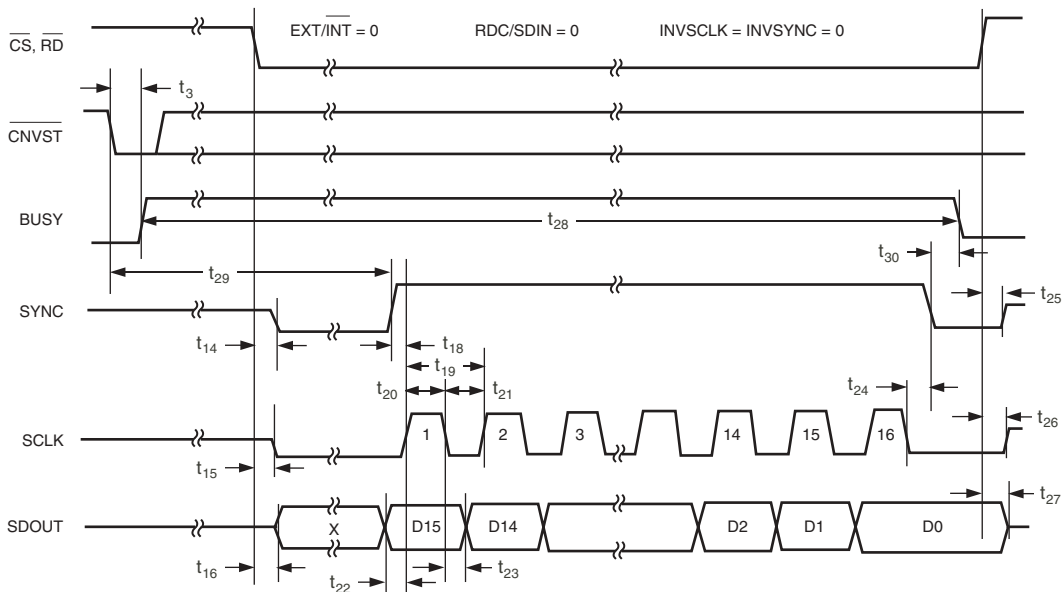


Figure 18. Master Serial Data Timing for Reading (Read After Convert)

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SERIAL INTERFACE

The AD7621 is configured to use the serial interface when $\overline{\text{SER/PAR}}$ is held high. The AD7621 outputs 16 bits of data, MSB first, on the SDOUT pin. This data is synchronized with the 16 clock pulses provided on SCLK pin. The output data is valid on both the rising and falling edge of the data clock. That allows a fast serial interface speed by using the same clock edge to output the data from the ADC and to sample the previous bit by the digital host.

MASTER SERIAL INTERFACE

Internal Clock

The AD7621 is configured to generate and provide the serial data clock SCLK when the $\overline{\text{EXT/INT}}$ pin is held low. The AD7621 also generates a SYNC signal to indicate to the host when the serial data is valid. The serial clock SCLK and the SYNC signal can be inverted if desired. Depending on RDC/SDIN input, the data can be read after each conversion or during the following conversion. Figure 18 and Figure 19 show the detailed timing diagrams of these two modes.

Usually, because the AD7621 is used with a fast throughput, the mode master, read during conversion is the most recommended serial mode when it can be used.

In read-during-conversion mode, the serial clock and data toggle at appropriate instants which minimize potential feedthrough between digital activity and the critical conversion decisions.

In read-after-conversion mode, it should be noted that, unlike in other modes, the signal BUSY returns low after the 16 data bits are pulsed out and not at the end of the conversion phase which results in a longer BUSY width.

To accommodate slow digital hosts, the serial clock can be slowed down by using DIVSCLK.

SLAVE SERIAL INTERFACE

External Clock

The AD7621 is configured to accept an externally supplied serial data clock on the SCLK pin when the $\overline{\text{EXT/INT}}$ pin is held high. In this mode, several methods can be used to read the data. The external serial clock is gated by $\overline{\text{CS}}$. When $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are both low, the data can be read after each conversion or during the following conversion. The external clock can be either a continuous or discontinuous clock. A discontinuous clock can be either normally high or normally low when inactive. Figure 20 and Figure 22 show the detailed timing diagrams of these methods.

While the AD7621 is performing a bit decision, it is important that voltage transients not occur on digital input/output pins or degradation of the conversion result could occur. This is particularly important during the second half of the conversion phase because the AD7621 provides error correction circuitry that can correct for an improper bit decision made during the first half of the conversion phase. For this reason, it is recommended that when an external clock is being provided, it is a discontinuous clock that is toggling only when BUSY is low or, more importantly, that it does not transition during the latter half of BUSY high.

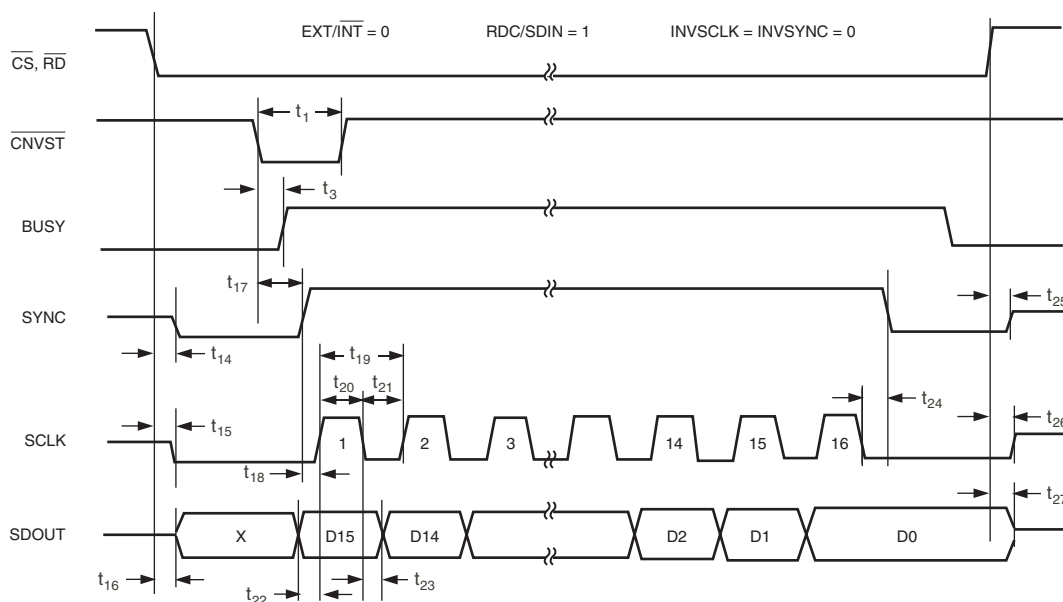


Figure 19. Master Serial Data Timing for Reading (Read Previous Conversion During Convert)

External Discontinuous Clock Data Read After Conversion

Though the maximum throughput cannot be achieved using this mode, it is the most recommended of the serial slave modes. Figure 20 shows the detailed timing diagrams of this method. After a conversion is complete, indicated by $\overline{\text{BUSY}}$ returning low, the result of this conversion can be read while both $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are low. The data is shifted out, MSB first, with 16 clock pulses and is valid on both rising and falling edge of the clock.

Among the advantages of this method, the conversion performance is not degraded because there are no voltage transients on the digital interface during the conversion process.

Another advantage is to be able to read the data at any speed up to 80 MHz which accommodates both slow digital host interface and the fastest serial reading.

Finally, in this mode only, the AD7621 provides a “daisy-chain” feature using the RDC/SDIN input pin for cascading multiple converters together. This feature is useful for reducing component count and wiring connections when desired as, for instance, in isolated multiconverter applications.

An example of the concatenation of two devices is shown in Figure 21. Simultaneous sampling is possible by using a common $\overline{\text{CNVST}}$ signal. It should be noted that the RDC/SDIN input is latched on the edge of SCLK opposite to the one used to shift out the data on SDOOUT. Hence, the MSB of the “upstream” converter just follows the LSB of the “downstream” converter on the next SCLK cycle.

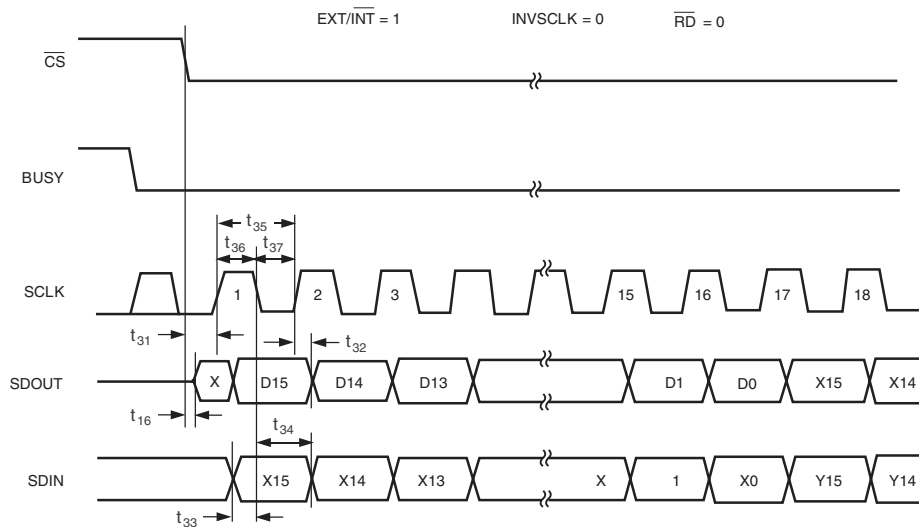


Figure 20. Slave Serial Data Timing for Reading (Read After Convert)

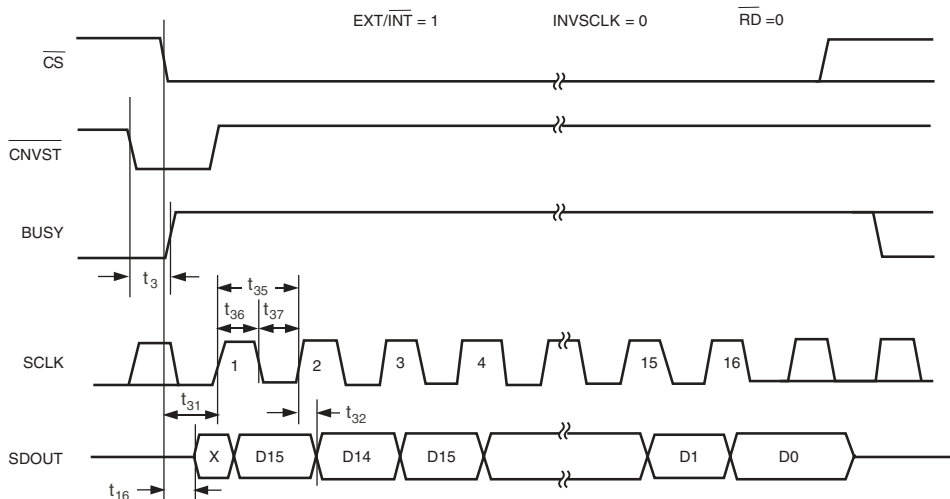


Figure 22. Slave Serial Data Timing for Reading (Read Previous Conversion During Convert)

AD7621

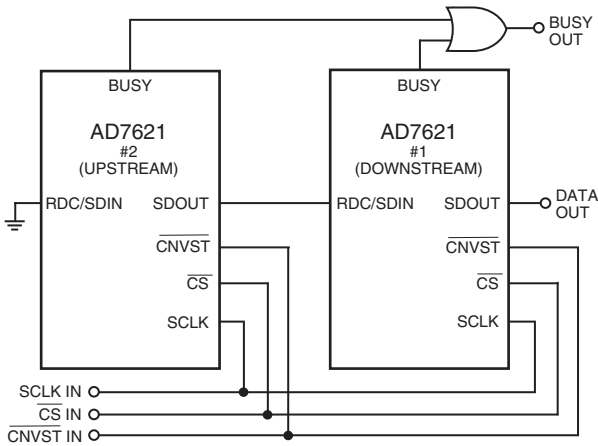


Figure 21. Two AD7621s in a "Daisy-Chain" Configuration

External Clock Data Read During Conversion

Figure 22 shows the detailed timing diagrams of this method. During a conversion, while both \overline{CS} and \overline{RD} are both low, the result of the previous conversion can be read. The data is shifted out, MSB first, with 16 clock pulses and is valid on both rising and falling edge of the clock. The 16 bits have to be read before the current conversion is complete. If that is not done, RDERROR is pulsed high and can be used to interrupt the host interface to prevent incomplete data reading. There is no "daisy chain" feature in this mode and RDC/SDIN input should always be tied either high or low.

To reduce performance degradation due to digital activity, a fast discontinuous clock of is recommended to ensure that all the bits are read during the first half of the conversion phase. It is also possible to begin to read the data after conversion and continue to read the last bits even after a new conversion has been initiated.

MICROPROCESSOR INTERFACING

The AD7621 is ideally suited for traditional dc measurement applications supporting a microprocessor, and ac signal processing applications interfacing to a digital signal processor. The AD7621 is designed to interface either with a parallel 8-bit or 16-bit wide interface or with a general purpose serial port or I/O ports on a microcontroller. A variety of external buffers can be used with the AD7621 to prevent digital noise from coupling into the ADC. The following section illustrates the use of the AD7621 with an SPI equipped DSP, the ADSP-219x.

SPI Interface (ADSP-219x)

Figure 22 shows an interface diagram between the AD7621 and an SPI-equipped DSP, ADSP219x. To accommodate the slower speed of the DSP, the AD7621 acts as a slave device and data must be read after conversion. This mode also allows the "daisy chain" feature. The convert command could be initiated in response to an internal timer interrupt. The reading process could be initiated in response to the end-of-conversion signal (BUSY going low) using an interrupt line of the DSP. The Serial Peripheral Interface (SPI) on the ADSP-219x is configured for master mode (MSTR) = 1, Clock Polarity Bit (CPOL) = 0, Clock Phase Bit (CPHA) = 1 and SPI interrupt enable (TIMOD) =00 by writing to the SPI Control Register (SPICLTx). It should be noted that to meet all timing requirements, the SPI clock should be limited to 17Mbits/s which allow to read an ADC result in about 1.1 μ s. When higher sampling rate is desired, it is recommended to use one of the parallel interface mode with the ADSP-219x.

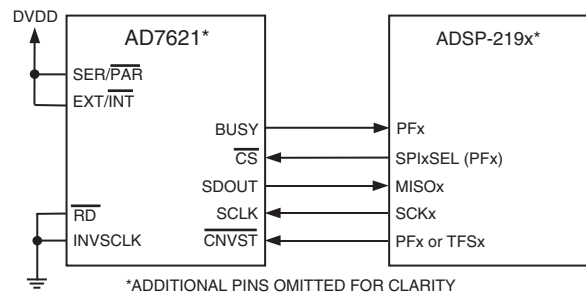


Figure 23. Interfacing the AD7621 to SPI Interface

APPLICATION HINTS**Layout**

The AD7621 has very good immunity to noise on the power supplies. However, care should still be taken with regard to grounding layout.

The printed circuit board that houses the AD7621 should be designed so the analog and digital sections are separated and confined to certain areas of the board. This facilitates the use of ground planes that can be easily separated. Digital and analog ground planes should be joined in only one place, preferably underneath the AD7621, or, at least, as close as possible to the AD7621. If the AD7621 is in a system where multiple devices require analog to digital ground connections, the connection should still be made at one point only, a star ground point, which should be established as close as possible to the AD7621.

It is recommended to avoid running digital lines under the device as these will couple noise onto the die. The analog ground plane should be allowed to run under the AD7621 to avoid noise coupling. Fast switching signals like $\overline{\text{CNVST}}$ or clocks should be shielded with digital ground to avoid radiating noise to other sections of the board, and should never run near analog signal paths. Crossover of digital and analog signals should be avoided. Traces on different but close layers of the board should run at right angles to each other. This will reduce the effect of feedthrough through the board. The power supply lines to the AD7621 should use as large a trace as possible to provide low impedance paths and reduce the effect of glitches on the power supply lines. Good decoupling is also important to lower the supplies impedance presented to the AD7621 and reduce the magnitude of the supply spikes. Decoupling ceramic capacitors, typically 100 nF, should be placed on each power supplies pins AVDD, DVDD and OVDD close to, and ideally right up against these pins and their corresponding ground pins. Additionally, low ESR 10 μF capacitors should be located in the vicinity of the ADC to further reduce low frequency ripple.

The DVDD supply of the AD7621 can be either a separate supply or come from the analog supply, AVDD, or from the digital interface supply, OVDD. When the system digital supply is noisy, or fast switching digital signals are present, it is recommended if no separate supply available, to connect the DVDD digital supply to the analog supply AVDD through an RC filter as shown in Figure 5, and connect the system supply to the interface digital supply OVDD and the remaining digital circuitry. When DVDD is powered from the system supply, it is useful to insert a bead to further reduce high-frequency spikes.

The AD7621 has four different ground pins; REFGND, AGND, DGND, and OGND. REFGND senses the reference voltage and should be a low impedance return to the reference because it carries pulsed currents. AGND is the ground to which most internal ADC analog signals are referenced. This ground must be connected with the least resistance to the analog ground plane. DGND must be tied to the analog or digital ground plane depend-

ing on the configuration. OGND is connected to the digital system ground.

The layout of the decoupling of the reference voltage is important. The decoupling capacitor should be close to the ADC and connected with short and large traces to minimize parasitic inductances.

Evaluating the AD7621 Performance

A recommended layout for the AD7621 is outlined in the documentation of the [EVAL-AD7621-CB](#), evaluation board for the AD7621. The evaluation board package includes a fully assembled and tested evaluation board, documentation, and software for controlling the board from a PC via the Eval Control Brd3.

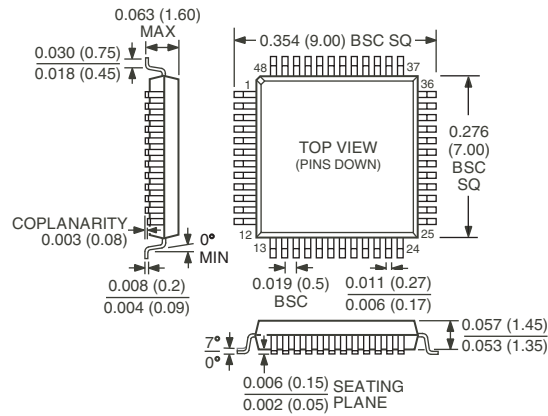
PRELIMINARY TECHNICAL DATA

AD7621

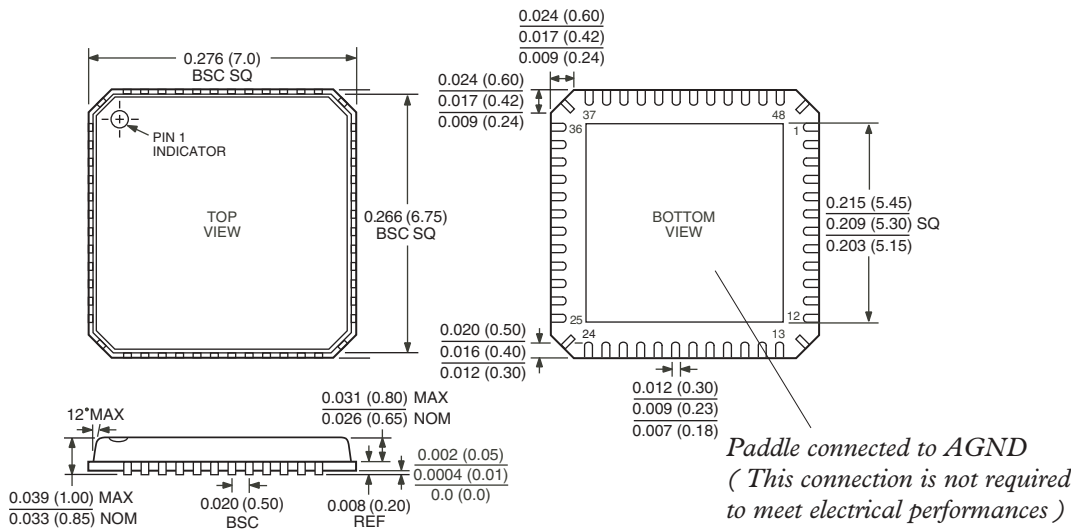
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

48-Lead Quad Flatpack (LQFP) (ST-48)



48-Lead Frame Chip Scale Package (LFCSP) (CP-48)



CONTROLLING DIMENSIONS ARE IN MILLIMETERS