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PHASE CONTROL THYRISTOR

AT405

Repetitive voltage up to	**1200 V**
Mean on-state current	**305 A**
Surge current	**2.8 kA**

FINAL SPECIFICATION

gen 03 - ISSUE : 05

Symbol	Characteristic	Conditions	Tj [°C]	Value	Unit
BLOCKING					
V_{RRM}	Repetitive peak reverse voltage		125	1200	V
V_{RSM}	Non-repetitive peak reverse voltage		125	1300	V
V_{DRM}	Repetitive peak off-state voltage		125	1200	V
I_{RRM}	Repetitive peak reverse current	V=VRRM	125	30	mA
I_{DRM}	Repetitive peak off-state current	V=VDRM	125	30	mA
CONDUCTING					
$I_{T(AV)}$	Mean on-state current	180° sin, 50 Hz, Th=55°C, double side cooled		305	A
$I_{T(AV)}$	Mean on-state current	180° sin, 50 Hz, Tc=85°C, double side cooled		245	A
I_{TSM}	Surge on-state current	sine wave, 10 ms	125	2.8	kA
I^2t	I^2t	without reverse voltage		39 x1E3	A^2s
V_T	On-state voltage	On-state current = 600 A	25	1.88	V
$V_{T(TO)}$	Threshold voltage		125	1.0	V
r_T	On-state slope resistance		125	1.900	mohm
SWITCHING					
di/dt	Critical rate of rise of on-state current, min.	From 75% VDRM up to 300 A, gate 10V 5ohm	125	200	A/μs
dv/dt	Critical rate of rise of off-state voltage, min.	Linear ramp up to 70% of VDRM	125	500	V/μs
td	Gate controlled delay time, typical	VD=100V, gate source 10V, 10 ohm , tr=.5 μs	25	0.7	μs
tq	Circuit commutated turn-off time, typical	dV/dt = 20 V/μs linear up to 75% VDRM	125	200	μs
Q_{rr}	Reverse recovery charge	di/dt=-20 A/μs, I= 195 A			μC
I_{rr}	Peak reverse recovery current	VR= 50 V			A
I_H	Holding current, typical	VD=5V, gate open circuit	25	300	mA
I_L	Latching current, typical	VD=5V, tp=30μs	25	700	mA
GATE					
V_{GT}	Gate trigger voltage	VD=5V	25	3.5	V
I_{GT}	Gate trigger current	VD=5V	25	200	mA
V_{GD}	Non-trigger gate voltage, min.	VD=VDRM	125	0.25	V
V_{FGM}	Peak gate voltage (forward)			20	V
I_{FGM}	Peak gate current			8	A
V_{RGM}	Peak gate voltage (reverse)			5	V
P_{GM}	Peak gate power dissipation	Pulse width 100 μs		75	W
P_G	Average gate power dissipation			1	W
MOUNTING					
$R_{th(j-h)}$	Thermal impedance, DC	Junction to heatsink, double side cooled		95	°C/kW
$R_{th(c-h)}$	Thermal impedance	Case to heatsink, double side cooled		20	°C/kW
T_j	Operating junction temperature			-30 / 125	°C
F	Mounting force			4.9 / 5.9	kN
	Mass			55	g

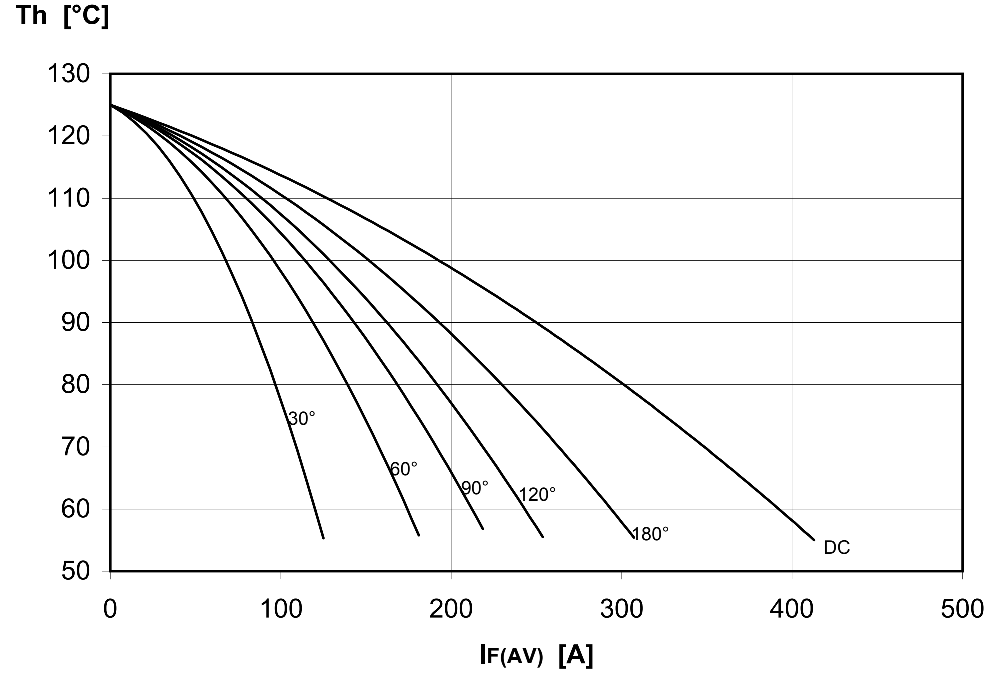
ORDERING INFORMATION : AT405 S 12

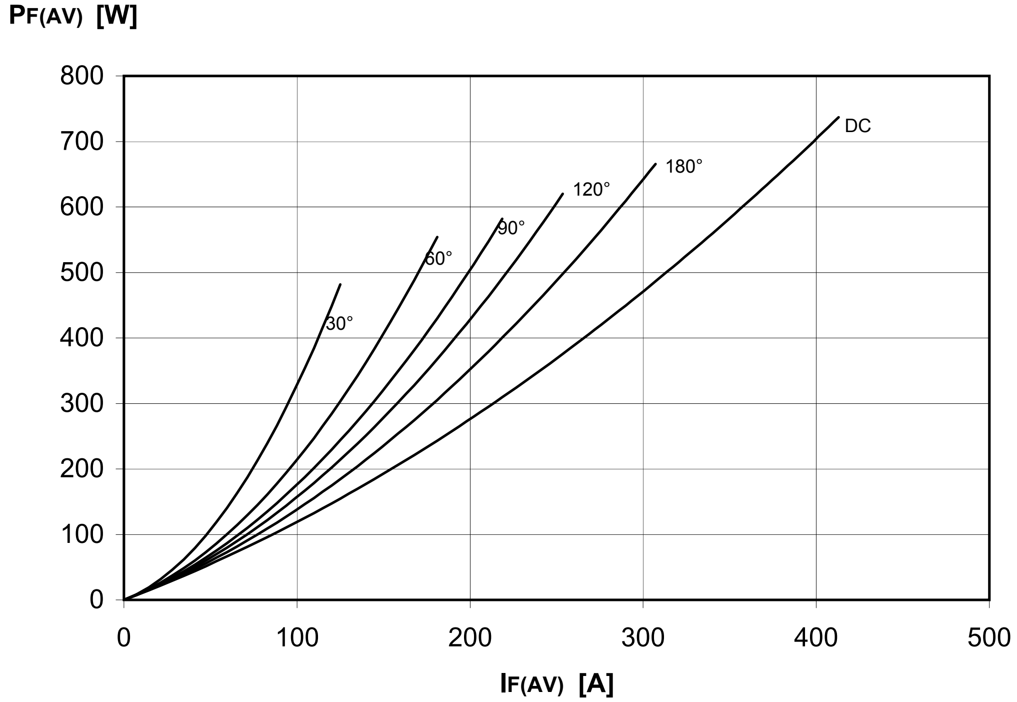
standard specification

VDRM&VRRM/100

DISSIPATION CHARACTERISTICS

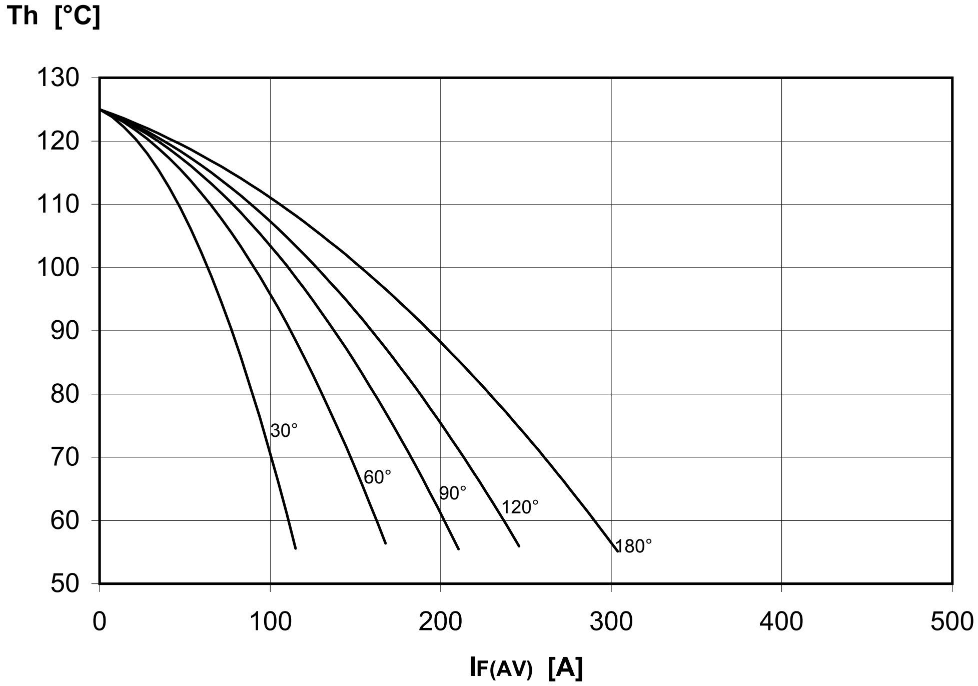
SQUARE WAVE

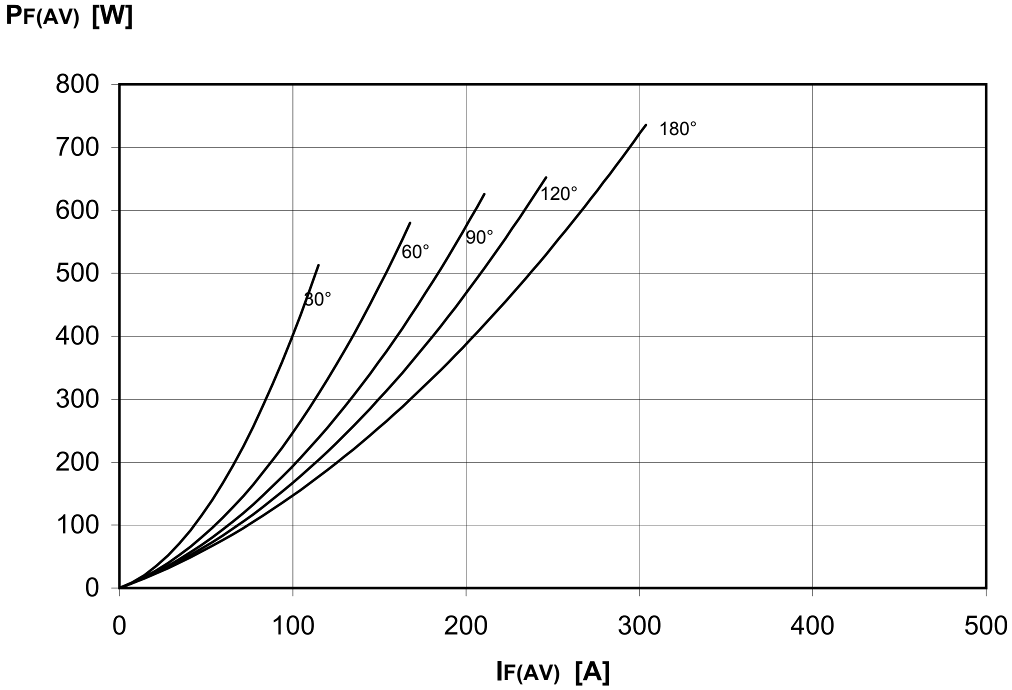




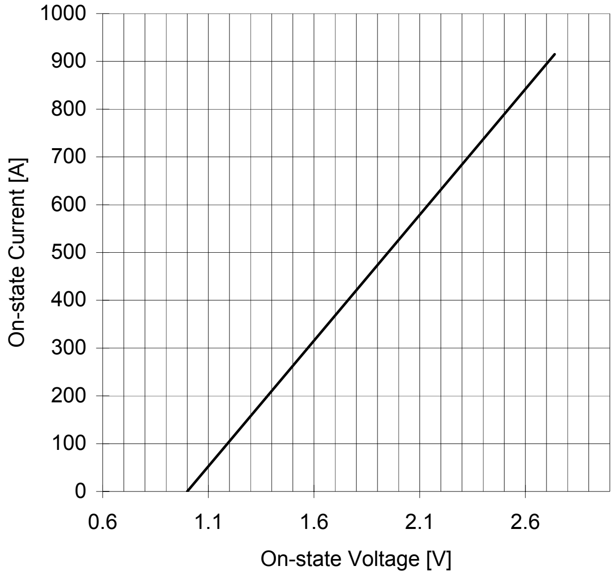
DISSIPATION CHARACTERISTICS

SINE WAVE

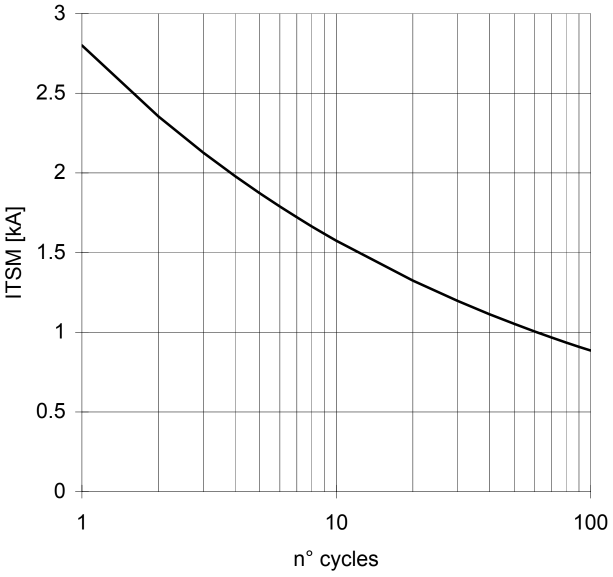




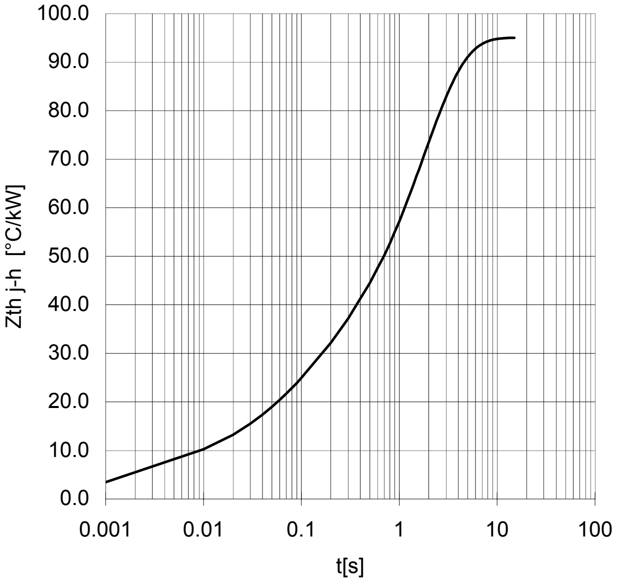
ON-STATE CHARACTERISTIC
Tj = 125 °C

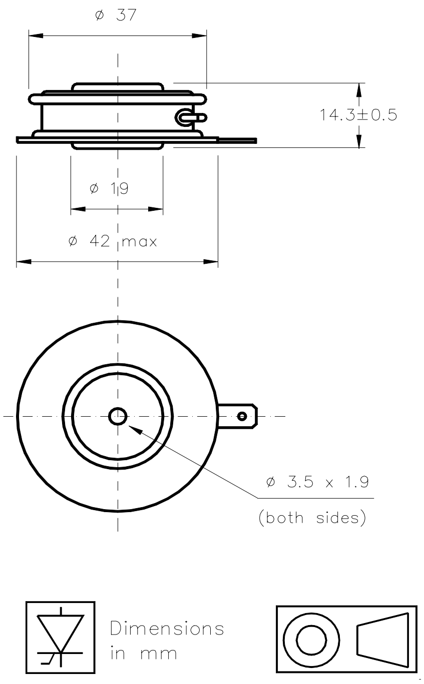


SURGE CHARACTERISTIC
Tj = 125 °C



TRANSIENT THERMAL IMPEDANCE
DOUBLE SIDE COOLED





Cathode terminal type DIN 46244 - A 4.8 - 0.8

Gate terminal type AMP 60598 - 1

All the characteristics given in this data sheet are guaranteed only with uniform clamping force, cleaned and lubricated heatsink, surfaces with flatness < .03 mm and roughness < 2 µm.
In the interest of product improvement POSEICO S.p.A. reserves the right to change any data given in this data sheet at any time without previous notice.
If not stated otherwise the maximum value of ratings (simbols over shaded background) and characteristics is reported.

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