Digital Attenuator, 15.5 dB, 5-Bit, TTL Driver, DC - 2.0 GHz

V 6.00

AT65-0283

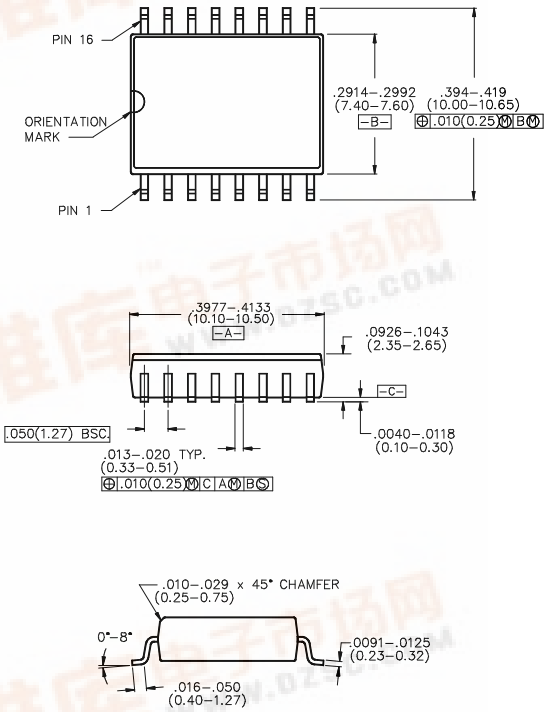
Features

- Attenuation: 0.5 dB Steps to 15.5 dB
- Low DC Power Consumption
- Plastic SOIC, Wide Body, SMT Package
- Integral TTL Driver
- 50 ohm Impedance
- Test Boards are Available
- Tape and Reel Packaging Available

Description

M/A-COM's AT65-0283 is a GaAs FET 5-bit digital attenuator with integral TTL driver. Step size is 0.5 dB providing a 15.5 dB total attenuation range. This device is in a SOIC-16 plastic surface mount package. The AT65-0283 is ideally suited for use where accuracy, fast speed, very low power consumption and low costs are required.

SOW-16



Package outline conforms to JEDEC standard MS-013AA.

Electrical Specifications: T_A = 25°C

Parameter	Test Conditions	Frequency	Units	Min	Typical	Max
Insertion Loss	—	DC - 1.0 GHz DC - 2.0 GHz	dB dB	— —	2.0 2.3	2.5 2.7
Attenuation Accuracy	Any Bit Any Combination of Bits	DC - 2.0 GHz DC -2.0 GHz	dB dB	— —	— —	±(.3 +4% of atten) ± (.3 +6% of atten)
VSWR	Full Range	DC - 2.0 GHz	Ratio	—	1.5:1	1.8:1
Switching Speed [1]	50% Cntl to 90%/10% RF 10% to 90% or 90% to 10%	— —	nS nS	— —	75 20	150 50
1 dB Compression	— —	50 MHz 0.5 - 2.0 GHz	dBm dBm	— —	+21 +29	— —
Input IP_3	Two-tone inputs up to +5 dBm	50 MHz 0.5-2.0 GHz	dB dB	— —	+35 +48	— —
Vcc -Vee	— —	— —	V V	4.75 -8.0	5.0 -5.0	5.25 -4.75
Logic “0”	Sink Current is 20 µA max.	—	V	0.0	—	0.8
Logic “1”	Source Current is 20 µA max.	—	V	2.0	—	5.0
Icc	Vcc min to max, Logic “0” or “1”	—	mA	—	0.2	6
-Iee	-Iee min to max, Logic “0” or “1”	—	mA	—	-0.2	-1

1. Decoupling capacitors (.01 µF) are required on power supply lines.

Pin Configuration

Pin #	Function	Pin #	Function
1	RF	9	C8
2	GND	10	Vcc
3	GND	11	Vee
4	GND	12	C4
5	GND	13	C2
6	GND	14	C1
7	GND	15	C0.5
8	RF	16	GND

Absolute Maximum Ratings [2]

Parameter	Absolute Maximum
Max. Input Power 0.05 GHz 0.5 - 2.0 GHz	 +27 dBm +34 dBm
+Vcc	+5.5V
-Vee	-8.5V
Logic Voltages [3]	-0.5 to Vcc + 0.5V
Operating Temperature	-40°C to +85°C
Storage Temperature	-65°C to +125°C

2. Operation of this device above any one of these parameters may cause permanent damange.
3. Standard CMOS TTL interface, latch-up will occur if logic signal is applied prior to power supply.

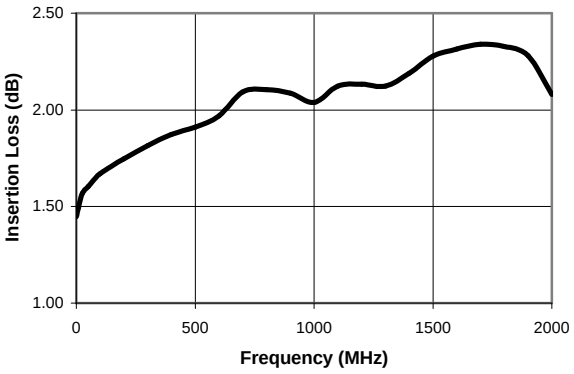
Truth Table

C8	C4	C2	C1	C0.5	Attenuation
0	0	0	0	0	Loss, Reference
0	0	0	0	1	0.5 dB
0	0	0	1	0	1.0 dB
0	0	1	0	0	2.0 dB
0	1	0	0	0	4.0 dB
1	0	0	0	0	8.0 dB
1	1	1	1	1	15.5 dB

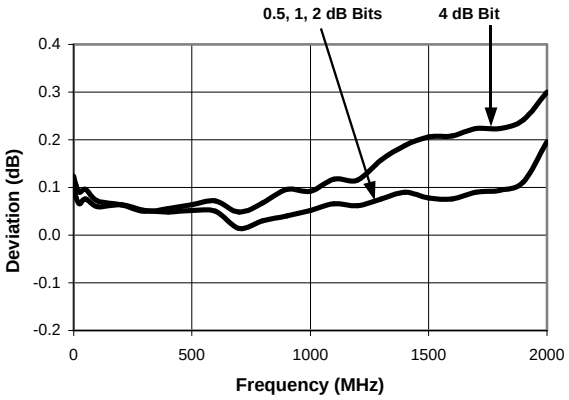
0 = TTL Low; 1 = TTL High

Typical Performance Curves

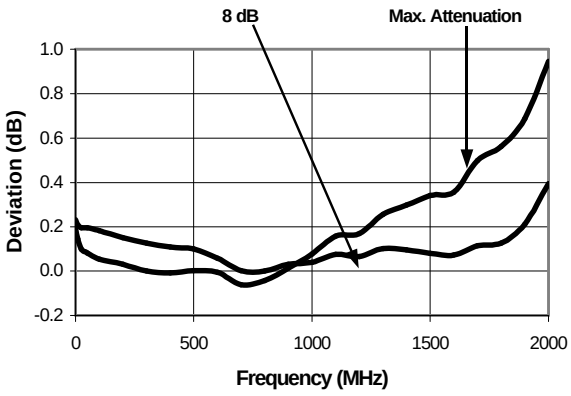
Insertion Loss



Attenuation Accuracy

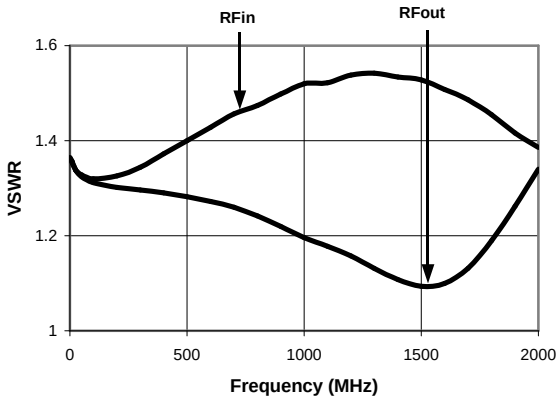


Attenuation Accuracy

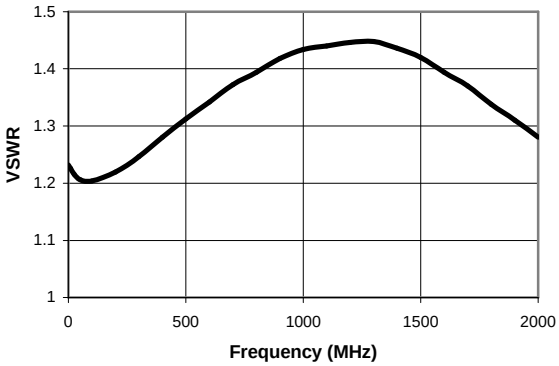


Typical Performance Curves

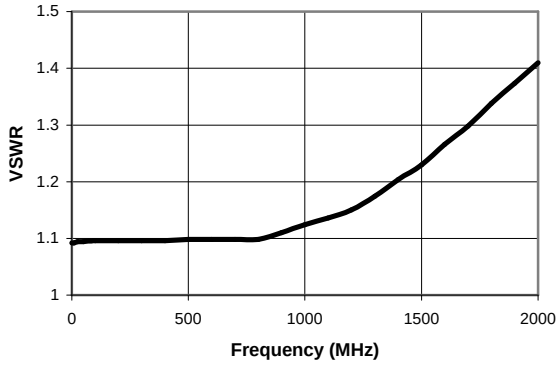
VSWR @ Insertion Loss



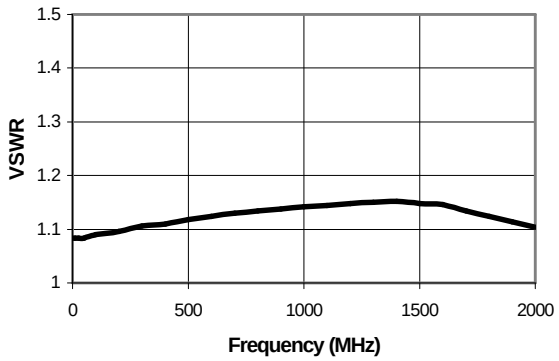
VSWR RFout, 0.5, 1, 2 & 4 dB Bits



VSWR RFin, 0.5, 1, 2, 4, 8 dB Bits and Max Attenuation



VSWR RFout, 8 dB Bit & Max Attenuation



Ordering Information

Part Number	Package
AT65-0283	Bulk Packaging
AT65-0283TR	Tape and Reel (1K Reel)
AT65-0283-TB	Units Mounted on Test Board