

Features

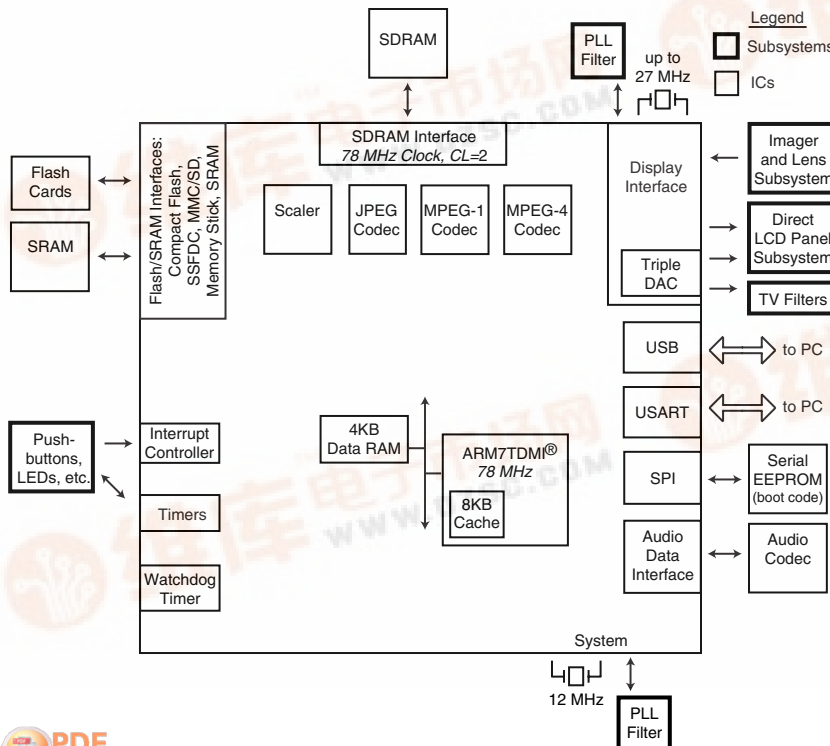
- Supports Image (Up to 16 Mpixels) and Video Playback Applications
- ARM7TDMI® CPU Running at a Maximum Rate of 78 MHz
- 16/8-bit CCIR Digital Video Input Interface for Video/Still-Picture Capture
- Video Encoder for NTSC/PAL TV Signal
- Digital Video Outputs Include: Composite, 16/8-bit YC (CCIR-656), RGB 565, 24-bit RGB, Component (Y/Pr/Pb), VESA Up to XGA Resolutions
- Integrated Triple Video DAC for Composite, Component, RGB, or S-Video Outputs
- Direct Interface to Epson, Casio, or AU LCDs
- Image Scaling and Rotation Hardware
- Baseline JPEG Compression/Decompression
- MPEG-1 Encode/Decode at 24 fps VGA
- MPEG-4 Codec Simple Profile at 30 fps CIF Resolution
- SDRAM Interface Supports Up to 512 Mbit Devices
- Unified Memory Architecture (All Program and Data Stored in SDRAM)
- Static Memory Controller (Flash/SRAM) Supports Up to Four 16 MB Devices
- Support for All Flash Card Interfaces (MMC/SD, Memory Stick Pro™, SSFDC/Smartmedia, CompactFlash® with IDE I/O Mode Support)
- Audio Data Interface for Connection to External Stereo ADC/DAC
- USB 2.0 High-speed Slave Controller for PC Card Reading Applications - OR -
- USB 1.1 Full-speed Host/Slave Controller for Direct Connection to Digital Cameras
- USART Interface
- Serial Peripheral Interface for Loading Boot Code and Controlling External Devices
- Three General-purpose Timers for Waveform Generation and Event Monitoring
- Programmable Watchdog Timer
- Up to Eight External Interrupts
- Up to 102 Pins Configurable as General-purpose I/Os
- All Low-level Software and Application Samples are Provided
- 1.8 V Core and 3.3 V I/O Operation
- 208-ball BGA Package



High-Performance Digital Imaging and Video Processor

AT76C120 Summary

Figure 1. Typical DSC Application Using The AT76C120





Description

The AT76C120 is a highly integrated solution for still-image and video playback applications. It can also operate as a video capture device for low-cost Personal Video Recording (PVR) applications. It combines a number of functions that are required in such devices:

- The design is based on an ARM7[®] microprocessor that controls the entire chip. A number of hardware resources, controlled by the ARM processor, perform digital imaging functions such as image signal processing, JPEG coding/decoding, MPEG-1 coding/decoding, DMA access to the SDRAM, and video encoding. All of these computationally-intensive functions are implemented in hardware which can be programmed according to user specifications, thus allowing the ARM processor to be free for other user-defined functions. The processor has 8 KB of internal instruction/data cache that helps it to operate efficiently and use minimal SDRAM bandwidth.
- The device also features Personal Video Recording capabilities. It has a 16/8-bit CCIR digital video input interface (shared with the display interface) that can capture still-image/video data from either a CMOS sensor or a video decoder. The video data can then be compressed using the MPEG engine.
- The device has numerous display capabilities. It has an integrated video encoder (double sampling) and 10-bit differential video DACs running at 78 MHz to support direct display to high-definition TVs and projectors at different VESA rates up to XGA (1024 x 768) resolutions. The device also has a 24-bit RGB output to interface to flat-panel TVs (LCDs and Plasma). It supports both square pixel and CCIR-type formats and can display in NTSC or PAL modes with the same crystal. It also has an LCD controller that supports a variety of LCD panels (Epson, Casio, AU) without the need for external ICs. Finally, it has an 8/16-bit CCIR-type output interface.
- The device has a high-performance image scaler that can do up-and-down scaling at floating point resolutions. This is very useful for playback applications, where images of arbitrary sizes need to be displayed on fixed resolution displays. In addition, the device supports hardware rotation, as well as flipping and mirroring in both vertical and horizontal dimensions. It takes about 120 ms to rotate a 2M image (1600 pixels) in any direction.
- The AT76C120 has a hardware JPEG compression/decompression engine that can decode a 2M pixel image in less than 150 ms. Non-standard Huffman JPEG tables are also supported using a combination of hardware and software resources. The engine can also do motion JPEG encoding and decoding.
- The integrated MPEG decoder can be used to play video clips taken from digital cameras and mobile phones. It supports Simple Profile MPEG-4 bitstreams at 30 fps CIF (I and P frames) and MPEG-1 video at 24 fps VGA (I frames only).
- The device utilizes a unified memory architecture using the SDRAM to process, capture, and play images and video, as well as to store program code and variables. It supports SDRAM configurations of up to 512 Mbits.
- A static memory controller is included that supports up to four 16 MB Flash or SRAM devices. Both 8-bit and 16-bit data buses are supported, with data accesses of up to 32 bits. The number of wait states and setup, hold, and data float times are programmable on a per device (chip select) basis.
- The device supports all Flash cards, including MultiMedia Card (MMC), Secure Digital (SD), Memory Stick Pro[™], Smartmedia/SSFDC/NAND Flash, and Compact Flash, including IDE I/O mode for streaming video. The Flash card interfaces can support read/write operations at the maximum speeds specified by the Flash cards. Data transfers between the Flash cards and the SDRAM are handled using high-

speed DMAs with FIFOs that leave the main processor free for other system applications.

- The I²S-compatible audio data interface allows the device to connect with an external stereo ADC/DAC to capture or play voice or audio. The device can encode captured audio in various popular formats, and can package it in the same bitstream as the video or the compressed JPEG pictures. It can also play back stand-alone audio, such as MP3 files or audio embedded in MPEG bitstreams.
- The USB 1.1 full-speed host controller allows the playback device to connect directly to digital cameras and either display images from the DSC or download them to the playback device. The USB 1.1 full-speed slave controller can be used to connect to a PC for downloading of images from the playback device to the PC.
- The USB 2.0 high-speed slave controller can also be used to connect to a PC for the downloading of images from the playback device to the PC. This interface is mutually exclusive from the USB 1.1 interfaces (see “Part Versions” below).
- An USART interface is included for serial communication. It supports standard baud rates of up to 460.8 Kbps or non-standard rates of up to 4.875 Mbps in asynchronous mode. It supports rates of up to 19.5 Mbps in synchronous mode.
- The serial peripheral interface (SPI) is used to boot from an external EEPROM. Once the boot code is loaded inside the program memory, the CPU can download its code from any peripheral supported by the device, including non-volatile storage media. With two chip select pins, the SPI can also be used to control other external devices at speeds of up to 19.2 Mbps with 64-bit transfers. Throughput decreases if the transfer size is reduced or the delay between transfers is increased.
- Three 16-bit general-purpose timers are included and can be used to generate interrupts to the internal CPU. They can generate waveforms on their associated pins via Pulse-width Modulation (PWM) or other techniques. They can also monitor and count external events on these pins.
- A dedicated watchdog timer is available which can provide an interrupt, an event on an external pin, or a reset to the internal CPU in the event that software is not responding as expected. Write access to the watchdog is protected by control access keys to prevent corruption of the watchdog should an error condition occur.
- The device provides up to eight external interrupt pins, depending on the system configuration, which can be handled by the interrupt controller as either edge or level sensitive.
- Up to 102 pins can also be configured as GPIOs, depending on the application.
- During normal operation, power consumption may be minimized by disabling the clock of any internal module that is not in use. In order to further reduce power consumption, the main CPU clock can be divided to run at a slower speed. In order to minimize power consumption when the device is not in use, a “sleep mode” is available that halts the operation of all logic and shuts down the oscillators and PLLs. Recovery from sleep mode occurs via the WKP (“wake-up”) pin, at which time the device begins execution from its previous state.

Part Versions

The AT76C120 device comes in two versions. One version has USB 1.1 full-speed host and slave interfaces, while the other version has a USB 2.0 high-speed slave interface. The corresponding part numbers are the AT76C120-U1 and the AT76C120-U2, respectively. The pin configuration of each version is mostly the same, but with a few differences as noted below.

Technology

- The device is fabricated in a 0.18 micron process. It is expected that the device will operate at less than 60 mA when fully active (video compression/decompression).



- The core requires a 1.8 V power supply, while most I/O pads require a 3.3 V supply.
- The package is a 208-ball BGA.



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