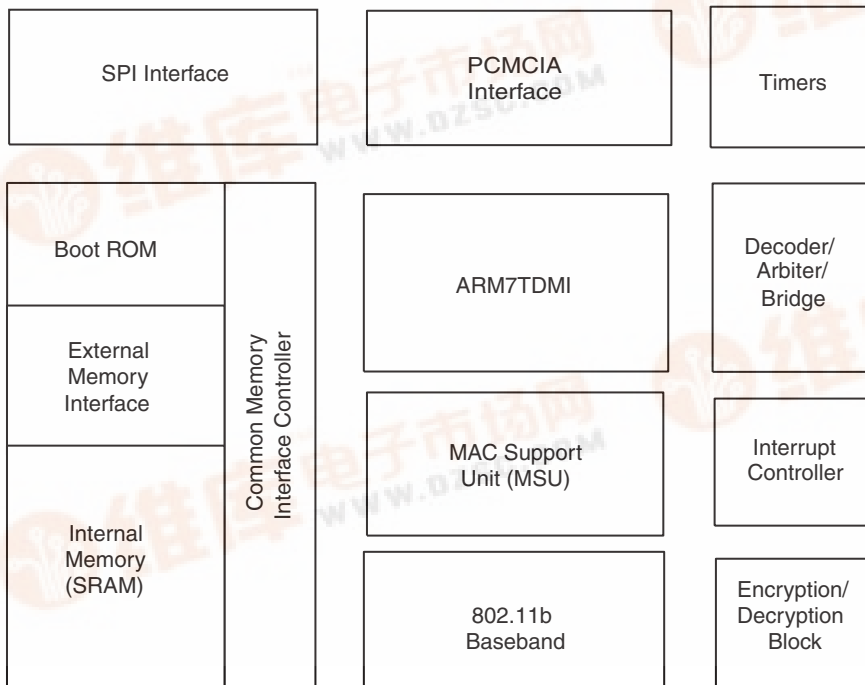


Features

- Integrates the IEEE 802.11b Physical Layer (Baseband) and the Media Access Controller (MAC) for Supporting Standard Rates up to 11 Mbps
- Supports Antenna Diversity Algorithm, Automatic Receive Gain Control, Transmit Gain Control, Transmit Filter for Japanese Regulatory and Differential or Single-ended I- and Q-Baseband Signals
- Integrates 160 KBytes of SRAM which Are Organized in Five Banks of 32 KBytes Each, Offering the Flexibility for individually Configuring Each of them as Program or Data Memory
- Zero Wait States for Program Execution
- Fast Data Transfers through DMA Channels
- Low Power ARM7TDMI® RISC Processor
- The Bootstrap Code Supports External SPI EEPROM for the Custom Configuration Parameters Used during the Device Enumeration Phase as Well as Default Parameters for First Time EEPROM Programming
- Glueless Parallel Flash Memory Interface, Supporting up to 128 KBytes of Nonvolatile Memory
- Glueless External SRAM Interface for all MAC Operations, Supporting up to 128 KBytes of External Memory
- Wired Equivalency Privacy (WEP) in Hardware Supporting 64-bit and 128-bit Keys
- Hardware Implementation of TKIP
- Hardware Implementation of AES Encryption Supporting Various Modes (CCM/CTR/CBC)
- The WLAN Functions Can Be Easily Changed or Updated to New Requirements Since They are Implemented in Microcode
- Supports 11 Mbps Rates with Automatic Fallback to 5.5, 2 and 1 Mbps
- SPI Interface and 13 GPIO Pins
- 176-ball LFBGA Package
- Low-voltage 1.8V Core Operation

Block Diagram



802.11b Baseband and Media Access Controller (MAC) for PCMCIA Bus

AT76C504A Summary





Description

The AT76C504A is a single-chip baseband controller that can handle IEEE 802.11b standard compliant data rates of up to 11 Mbps and provides all processing and functionality needed for the MAC protocol of IEEE 802.11b. AT76C504A provides a glueless interface conforming to PC Card 95 and can support a variety of RF interfaces.

The AT76C504A incorporates an ARM7TDMI processor using a sophisticated architecture to control the on-chip peripherals, manage the internal memory and allocate data queue buffers as well as to communicate with the host through the PCMCIA parallel bus. The processor peripheral logic consists of a PCMCIA bus interface, a Serial Peripheral Interface (SPI), a MAC unit, a 802.11b baseband controller, a WEP/TKIP engine block, an AES engine block, two memory controllers and the ARM[®] subsystem consisting of an Interrupt Controller, two 32-bit timers and an address decoder unit.

The ARM7TDMI core supports two alternative instruction sets. Powerful 32-bit code can be executed by the processor in ARM operating mode. However, a 16-bit instruction subset is also available in Thumb[®] mode. Thumb mode can be selected to exploit full processor power with limited external memory resources. Note that ARM7TDMI operating mode can be changed at run time with negligible overhead.



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