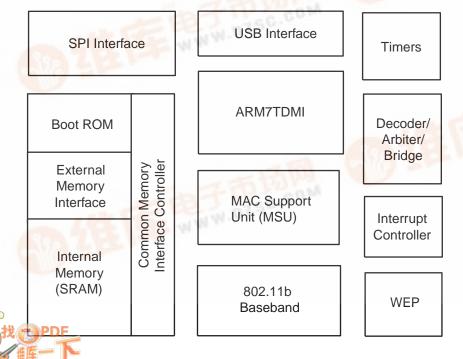
## **Features**

- IEEE 802.11b MAC and Baseband for Supporting Standard Rates Up to 11 Mbps
- Wireless Interface Following the IEEE 802.11b Standard
- Wireless LAN MAC Unit with ARM7TDMI<sup>®</sup> RISC Processor
- Integrated 128-byte Transmit and 128-byte Receive FIFOs for Wireless MAC Layer Functions
- Delivers Standard Wireless Networking to Any Host that Supports a Full-speed (12 Mbps) USB Interface
- The On-chip Boot-ROM Implements the Device Upgrade Protocol (DFU) Spec Making the AT76C505 Ideal for Low-cost Terminal Adaptors without Requiring External Program Flash Since the Host Driver Downloads the Code During the Start-up Phase
- Support of an External Serial EEPROM for Configuration Settings
- Glueless SRAM Interface for All MAC Operations, Supporting Up to 1M Byte of External Memory
- Integrated 6K x 32-bit Internal SRAM, Used for Fast Program Code Execution and Temporary Storage of Data
- Glueless Flash Memory Interface, Supporting Up to 1M Byte of Nonvolatile Memory for Permanent Storage of Program Code
- Wired Equivalency Privacy (WEP) in Hardware Supporting 64-bit and 128-bit Encryption
- Hardware Implementation of Time Critical MAC Functions by the MAC Support Unit (MSU) Guarantees Maximum Robustness
- The WLAN and Inter-networking Functions Can Be Changed and Updated Easily to New Requirements Since They are Implemented in Microcode
- Supports 11 Mbps Rates with Automatic Fallback to 5.5, 2 and 1 Mbps
- 128-ball CABGA Package
- Low-voltage 3.3V Operation
- SPI Interface and 8 GPIO Pins
- Baseband Supports Antenna Diversity Algorithm
- Baseband Supports Japan Filter
- Baseband Supports Differential or Single-ended I- and Q-Baseband Signals
- Integrated 802.11b Baseband Processor

# **Block Diagram**





802.11b Media Access Controller (MAC) and Baseband with USB Interface

# AT76C505 Summary

2364DS-WLAN-07/03



# Description

The AT76C505 is a single-chip baseband controller that can handle IEEE 802.11b standard compliant data rates of up to 11 Mbps and provides all processing and functionality needed for the MAC protocol of IEEE 802.11b. The AT76C505 is a full-speed USB device that can support up to four configurable Endpoints (EP) plus one Control EP. The AT76C505 USB interface can support Suspend and Resume bus condition for saving power during host idle periods.

Besides the USB interface unit, the AT76C505 chip contains a WEP engine block, a MAC Support Unit (MSU), a 802.11b baseband controller, a memory controller and the ARM<sup>®</sup> subsystem consisting of an Interrupt Controller, two 32-bit timers and an address decoder unit.

The ARM7TDMI core supports two alternative instruction sets. Powerful 32-bit code can be executed by the processor in ARM operating mode. However, a 16-bit instruction subset is also available in Thumb<sup>®</sup> mode. Thumb mode can be selected to exploit full processor power with limited external memory resources. Note that ARM7TDMI operating mode can be changed at run time with negligible overhead.



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