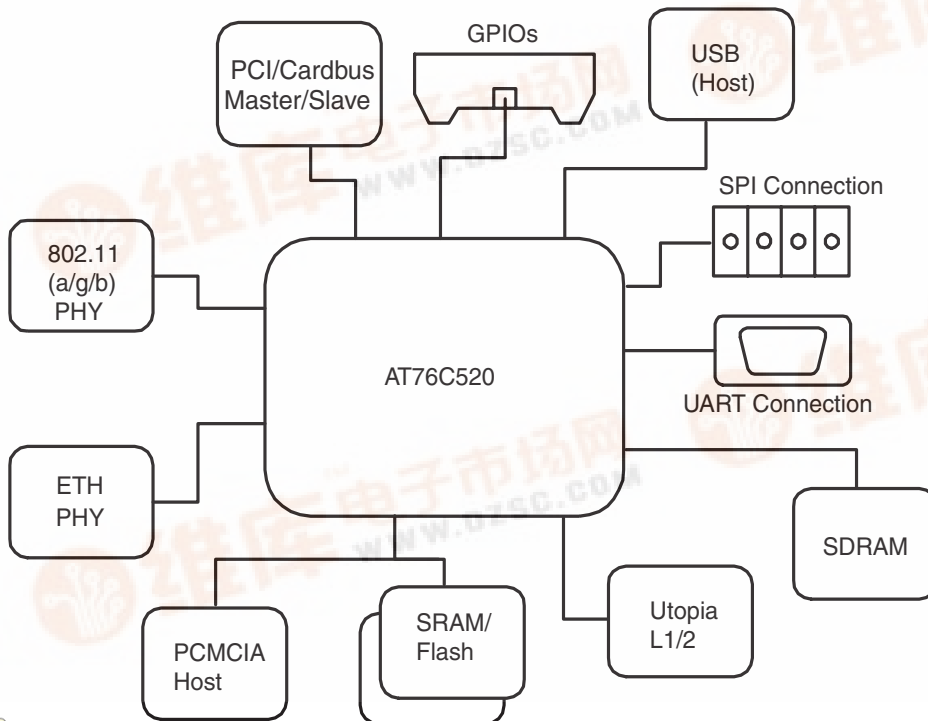


Features

- Routing Functions Running on ARM946ES™ Interworking Processor with 8K Data Cache and 8K Instruction Cache Memory
- Two Ethernet 10/100T-Base MAC Units with MII Interface to External PHY
- Maximum Sustainable Wired Bandwidth: 200Mbps (Half Duplex) or 400 Mbs (Full Duplex)
- WLAN ARM7TDMI™ with Direct Access to Communication Peripherals
- WLAN Hardware MAC Block (WHMB) Controlled by ARM7®, Supports 802.11a/b/g MAC Functions and Provides Serial or Parallel Interface to External 802.11 PHYs
- Atmel Common Memory Bus Architecture (COMBA) Guarantees No Bottleneck when All Communication Peripherals are Concurrently Used
- Hardware Security Accelerators Attached to the Common Bus Offer Instantaneous Encryption/Decryption and Authentication Support for the Following Algorithms:
 - CCM/CTR/CBC Modes of Advanced Encryption Standard (AES)
 - IPSEC Block Supports DES/3DES and Hash Functions (MD5, SHA-1)
 - TKIP
 - RC-4, WEP 64/128 Bit-Key (Part of the WHMB)
- PCI Bus Interface (Master/Slave) Compliant with PCI v 2.2
- SPI Master/Slave Interface, UART, and Watchdog Timer Interface
- UTOPIA Level 1 or 2 Interface Supporting up to 3 PHYs
- Two USB Full-speed (12 Mbps) Ports
- 24 GPIOs Can Be Configured to Provide Specific Functions such as UART Interface wWith Full Modem Control Signaling or 8-bit SRAM/ Flash Interface
- 32-bit SDRAM Interface
- 32-bit SRAM Interface
- 1.8 Volt Core Voltage Supply
- 3.3 Volt I/O Voltage Supply
- 324-pin BGA package

Network Processor Interfaces



Network Processor

AT76C520 Summary





Description

The AT76C520 is a powerful device which provides a rich set of features typically required by routing and gateway applications. The main CPU of the device is a high performing ARM946 processor. This processor runs at up to 100 MHz and offers more than 110 MIPS to Network and Transport Layer algorithms of an operating system as most of the common Physical and Data Link (PDL) layer functions are implemented by hardware units.

In addition to the main CPU, a second one complements the operation of the device by handling time critical tasks, such as interrupts by the low-layer functions of the various communication peripherals, minimizing the latency from which an overloaded processor may suffer. The second CPU is an ARM7[®] that is used for the implementation of 802.11a/b/g MAC functions when it runs at 80 MHz. This CPU can be also used for the implementation of a segmentation and reassembly sublayer above the Utopia interface or the USB Host control functions. In addition, it can simultaneously handle other I/O functions.

This multiprocessor system offers more than 150 MIPS so that it can cover the most demanding networking applications, considering also the high number of hardware blocks which support the PDL layer functions without CPU intervention.

Block interconnection is achieved using a Common Bus Architecture (COMBA), which guarantees data transferring without any bottleneck, as shown in Functional Diagram. This scheme allows the sharing of common system resources without affecting the performance, keeps the isolation of the processing units and arbitrates their requests for granting hardware accelerating blocks fairly in order to achieve high degree of parallel processing and maximum performance.

The AT76C520 can simultaneously service packets exchanged among two Ethernet 10/100T-Base, 80211.a/b/g WLAN networks, a UTOPIA Level 1 or 2 port for interfacing to DSL modems, and external network devices through extension ports able to support standard interfaces like USB, PCI/PCMCIA/Cardbus, and UART.

Encryption algorithms and hash functions usually encountered in network applications are implemented in hardware and can be enabled by any of the two processors. Examples of the hardware blocks are the AES unit, which supports the CCM/CTR/CBC modes, the TKIP for WPA support, and the IPSec unit with DES/3DES and MD5, SHA-1 capabilities. There is also a WEP unit integrated into the Hardware MAC block that implements the WEP algorithm of IEEE802.11 MAC standard.

The AT76C520 can also support a PCI Interface compliant with PCI v2.2. The chip can be configured as a master/ slave PCI device and can allow Host access to any memory location. It can also be configured as slave PCMCIA device.

The AT76C520 has internal 32-Kbytes SRAM attached to the COMBA bus which can be used by the processors for manipulating specific packet fields in order to avoid transactions with the external memory. The device also supports access, through the COMBA bus, to 256 Mbytes of external 32-bit SDRAM, 16 Mbytes of external SRAM, and 16 Mbytes of external Flash.

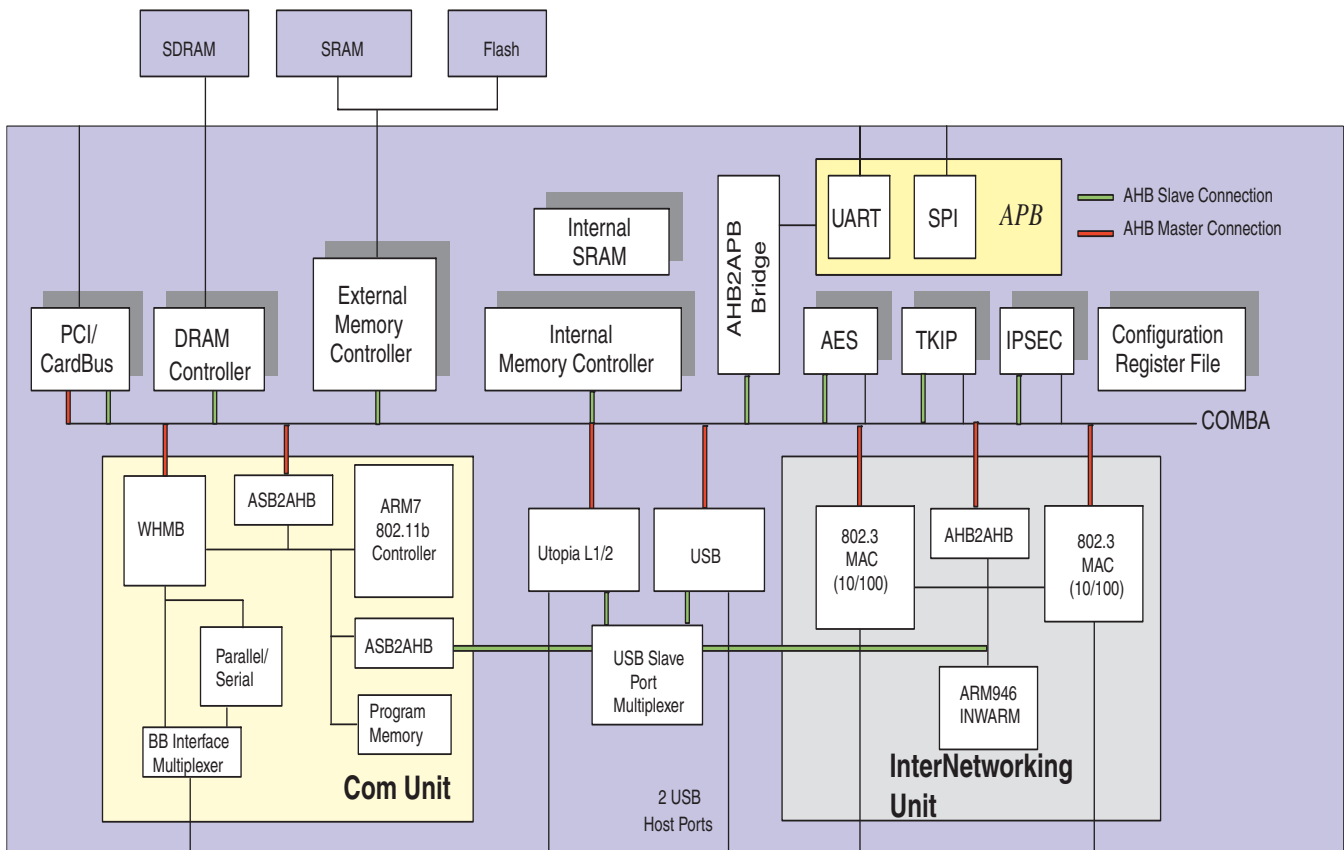
The ARM7 processor unit uses 32 Kbytes SRAM for both instruction and data. The interworking ARM9[®] processor, which is targeted for routing and bridging functions, uses 8 Kbyte-instruction Cache (ICache) and 8 Kbyte-Data Cache (DCache), as well as the external SDRAM for instruction or data fetching.

An efficient integration of fast communication peripherals such as UTOPIA and a USB Host allows either the ARM7 or the ARM9 to access them as slave devices, while they are able to transfer blocks of data to the common memory through the COMBA bus as

master devices. Support of AAL5 Segmentation and Reassembly is also provided by hardware blocks, as well as by the processors.

The device can also support a UART interface with a maximum baud rate 921 Kbaud with full modem control signals, as well as a Watchdog Timer. Finally, an SPI interface with two dedicated select signals is also available and can be configured as a slave one.

Functional Diagram





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5643AS-WLAN-12/04