

查询AT818供应商

捷多邦, 专业PCB打样工厂, 24小时加急出货

**ANSALDO**

**Ansaldo Trasporti s.p.a.**  
**Unita' Semiconduttori**

Via N. Lorenzi 8 - I 16152 GENOVA - ITALY  
Tel. int. +39/(0)10 6556549 - (0)10 6556488  
Fax Int. +39/(0)10 6442510  
Tx 270318 ANSUSE I -

**PHASE CONTROL THYRISTOR**

**AT818**

Repetitive voltage up to **4000 v**  
Mean on-state current **580 A**  
Surge current **5.9 kA**

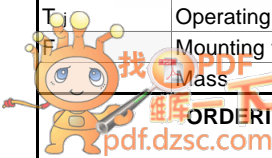
**FINAL SPECIFICATION**

feb 97 - ISSUE : 04

Symbol	Characteristic	Conditions	T <sub>j</sub> [°C]	Value	Unit
<b>BLOCKING</b>					
V <sub>RRM</sub>	Repetitive peak reverse voltage		125	4000	V
V <sub>RSM</sub>	Non-repetitive peak reverse voltage		125	4100	V
V <sub>DRM</sub>	Repetitive peak off-state voltage		125	4000	V
I <sub>RRM</sub>	Repetitive peak reverse current	V=VRRM	125	50	mA
I <sub>DRM</sub>	Repetitive peak off-state current	V=VDRM	125	50	mA
<b>CONDUCTING</b>					
I <sub>T(AV)</sub>	Mean on-state current	180° sin, 50 Hz, Th=55°C, double side cooled		580	A
I <sub>T(AV)</sub>	Mean on-state current	180° sin, 50 Hz, Tc=85°C, double side cooled		465	A
I <sub>TSM</sub>	Surge on-state current	sine wave, 10 ms	125	5.9	kA
I <sup>2</sup> t	I <sup>2</sup> t	without reverse voltage		174 x1E3	A <sup>2</sup> s
V <sub>T</sub>	On-state voltage	On-state current = 1600 A	25	3.38	V
V <sub>T(TO)</sub>	Threshold voltage		125	1.35	V
r <sub>T</sub>	On-state slope resistance		125	1.335	mohm
<b>SWITCHING</b>					
di/dt	Critical rate of rise of on-state current, min.	From 75% VDRM up to 620 A, gate 10V 5ohm	125	200	A/μs
dv/dt	Critical rate of rise of off-state voltage, min.	Linear ramp up to 70% of VDRM	125	500	V/μs
td	Gate controlled delay time, typical	VD=100V, gate source 25V, 10 ohm, tr=.5 μs	25	1.6	μs
tq	Circuit commutated turn-off time, typical	dV/dt = 20 V/μs linear up to 75% VDRM		320	μs
Q <sub>rr</sub>	Reverse recovery charge	di/dt=-20 A/μs, I= 410 A	125		μC
I <sub>rr</sub>	Peak reverse recovery current	VR= 50 V			A
I <sub>H</sub>	Holding current, typical	VD=5V, gate open circuit	25	300	mA
I <sub>L</sub>	Latching current, typical	VD=5V, tp=30μs	25	700	mA
<b>GATE</b>					
V <sub>GT</sub>	Gate trigger voltage	VD=5V	25	3.5	V
I <sub>GT</sub>	Gate trigger current	VD=5V	25	200	mA
V <sub>GD</sub>	Non-trigger gate voltage, min.	VD=VDRM	125	0.25	V
V <sub>FGM</sub>	Peak gate voltage (forward)			30	V
I <sub>FGM</sub>	Peak gate current			10	A
V <sub>RGM</sub>	Peak gate voltage (reverse)			5	V
P <sub>GM</sub>	Peak gate power dissipation	Pulse width 100 μs		150	W
P <sub>G</sub>	Average gate power dissipation			2	W
<b>MOUNTING</b>					
R <sub>th(j-h)</sub>	Thermal impedance, DC	Junction to heatsink, double side cooled		37	°C/kW
R <sub>th(c-h)</sub>	Thermal impedance	Case to heatsink, double side cooled		7	°C/kW
T <sub>j</sub>	Operating junction temperature			-30 / 125	°C
F <sub>Mass</sub>	Mounting force			11.8 / 13.2	kN
				300	g

ORDERING INFORMATION : AT818 S 40

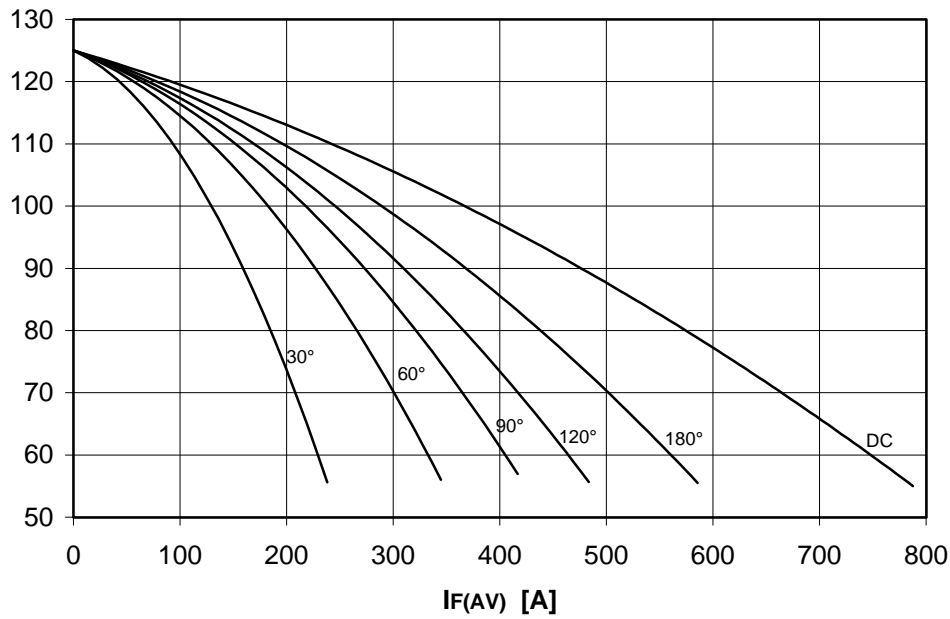
standard specification  VDRM&VRRM/100



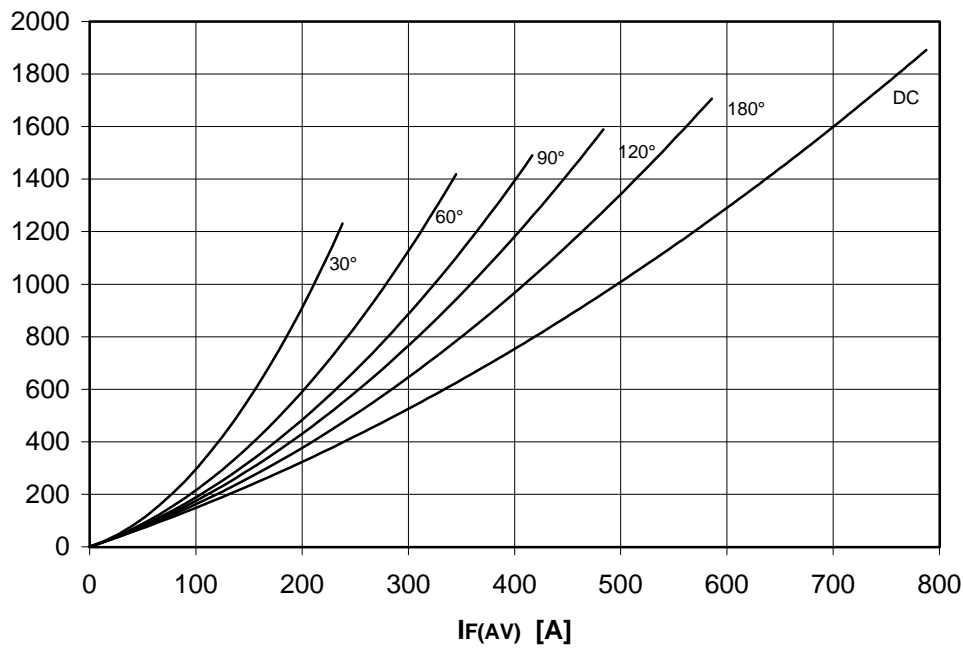
DISSIPATION CHARACTERISTICS

SQUARE WAVE

Th [°C]



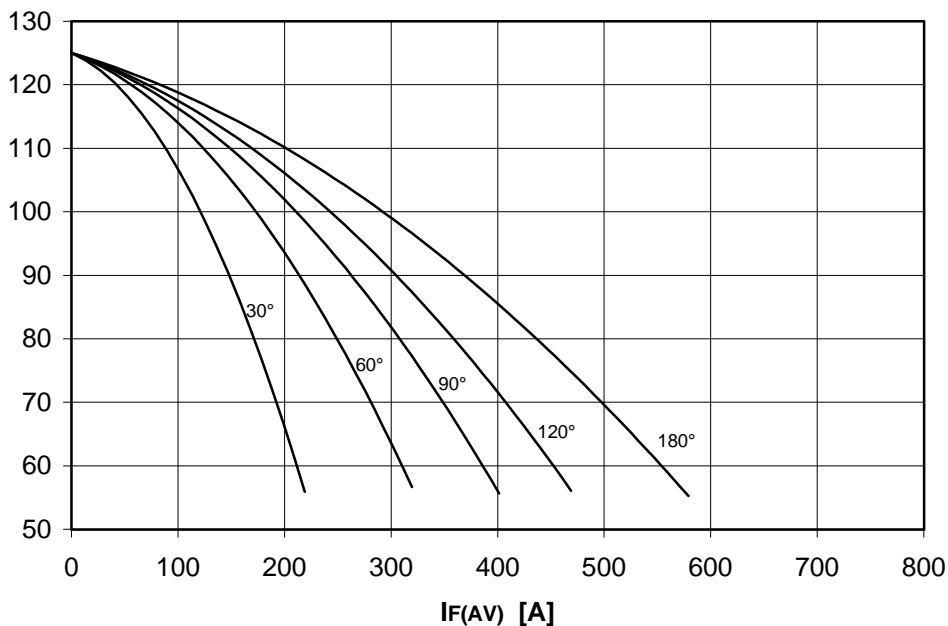
PF(AV) [W]



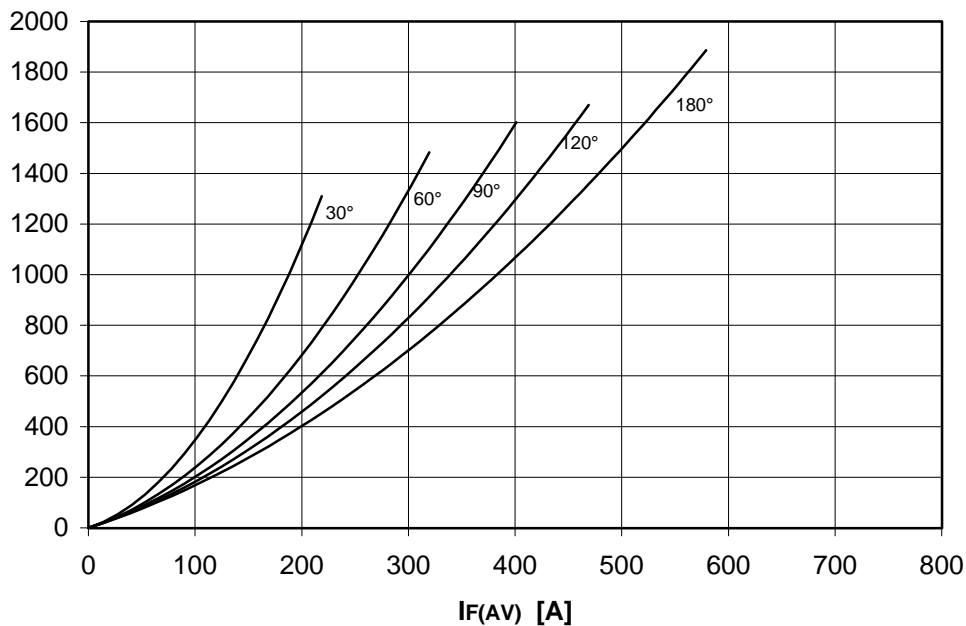
DISSIPATION CHARACTERISTICS

SINE WAVE

Th [°C]



PF(AV) [W]

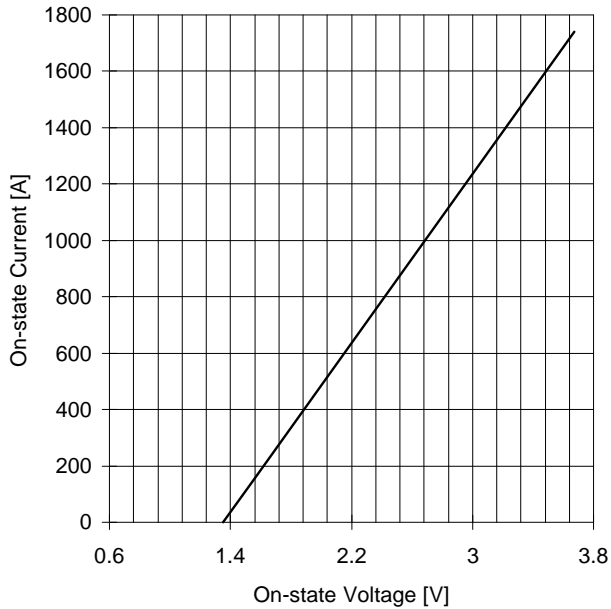


# AT818 PHASE CONTROL THYRISTOR

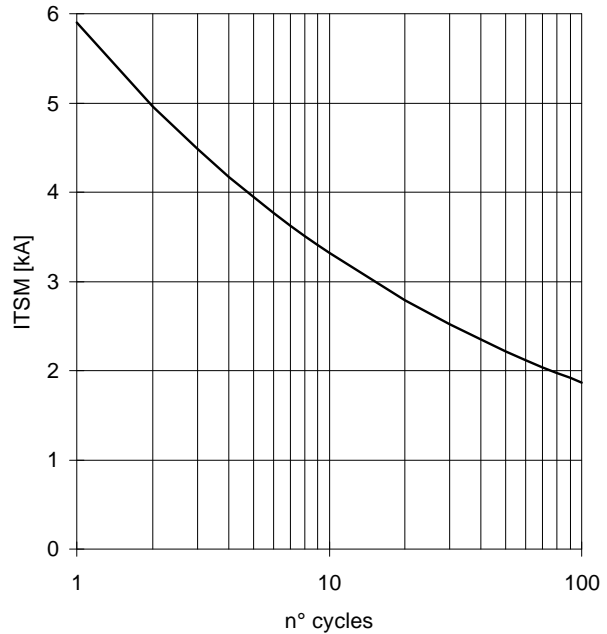
# ANSALDO

FINAL SPECIFICATION feb 97 - ISSUE : 04

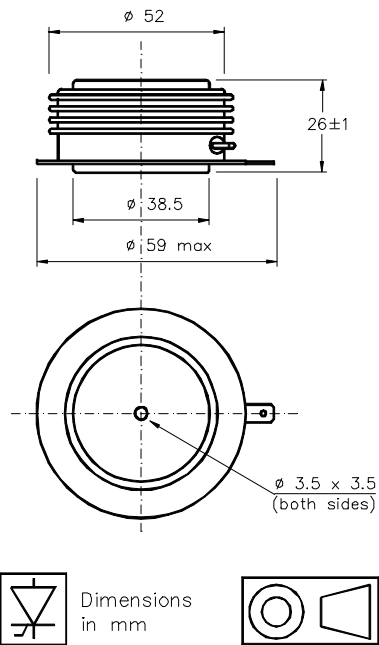
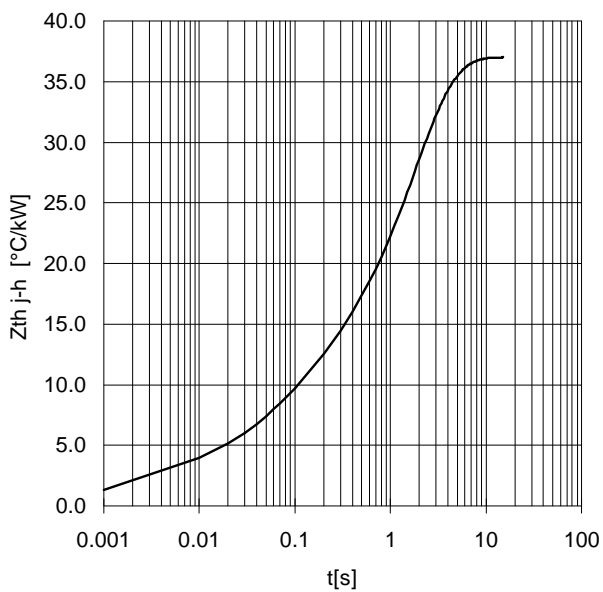
ON-STATE CHARACTERISTIC  
T<sub>j</sub> = 125 °C



SURGE CHARACTERISTIC  
T<sub>j</sub> = 125 °C



TRANSIENT THERMAL IMPEDANCE  
DOUBLE SIDE COOLED



Cathode terminal type DIN 46244 - A 4.8 - 0.8

Gate terminal type AMP 60598 - 1

All the characteristics given in this data sheet are guaranteed only with uniform clamping force, cleaned and lubricated heatsink, surfaces with flatness < .03 mm and roughness < 2 μm.

In the interest of product improvement ANSALDO reserves the right to change any data given in this data sheet at any time without previous notice.

If not stated otherwise the maximum value of ratings (symbols over shaded background) and characteristics is reported.

Distributed by

