AT86RF401 Reference Design

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It seems that many systems are requiring a radio frequency (RF) wireless link. We don't like standing on a chair to adjust the ceiling fan speed, we don't like climbing out of our car to open the garage door, and we certainly don't like walking outside on an early winter morning to see just how cold it is. Whether we're driven by cost, convenience, or performance, low cost RF wireless designs are here to stay. So, if you're not an expert in manipulating Maxwell's equations… is there an easy way to add RF to your design?

Fortunately, the answer is an emphatic YES. Atmel made your work much easier by recently introducing the AT86RF401, an RF wireless data micro-transmitter. By developing a chip that integrates the mysterious part of the RF transmitter design (normally reserved for an RF expert) and throwing in an AVR® microcontroller, your life just got a little bit simpler.

The heart of this chip is an AVR® microcontroller that's been given supervisory responsibility over a narrowband Phase-Locked-Loop (PLL) RF transmitter. What sets this device apart from many on the market today is that the solution is a true System On a Chip (SOC). It isn't a multi-chip package where each chip was designed by different teams having different priorities. Rather, it is a SINGLE chip resulting from the cooperative efforts of a cross-functional design team where the RF and control logic were designed to work together… from the beginning. With access to key RF control parameters such as output power attenuation, voltage controlled oscillator tuning, RF modulation and PLL lock/unlock criteria, the AVR core takes much of the headache out of getting your RF link's performance up to where you'd like it.

The AT86RF401 (see Figues A; page 40) is designed to operate down to 2.0V. C1, C7, and C8 provide an attenuation path to ground for unwanted high frequency transients. J2 provides an interface to the software development tools and allows you to flash the AVR®'s memory while it's still soldered onto the PCB. Switches, S1 – S4, along with the current limiting resistors, R1 – R4, trigger an event that awakens the device from a very low current sleep mode (typically less than 100 nA) and initiates the RF transmission.

The rest of the parts on the PCB support the RF transmitter. While X1 provides a clock source for the AVR®, it also is used as the reference frequency for the PLL. The PLL contains an internal divider fixed to 24 so the RF carrier will always be 24 times the frequency of X1 (24*13.125MHz = 315MHz). The VCO requires L2 to put its output in a controllable range enabling the PLL to closely track the reference frequency X1. All that's left to finish the design is to attach a tuned antenna to the chip and your hardware is ready. The complete Parts List is shown in table 1 below.

To minimize cost (while not the most efficient way to radiate RF), a tuned loop PCB trace antenna can be used. A reasonable impedance match between the output of the AT86RF401 and the PCB trace antenna AND assurance of an Federal Communications Commission (FCC) compliant design can be obtained using the component placement and geometry of the traces as shown in Figure 1a (top side PCB artwork including antenna) and Figure 1b (bottom side PCB artwork). Complete PCB design and fabrication documentation is available upon request. See contact information at the conclusion of this article.

In this design, peak resonance of the tuned loop antenna occurs with a non-standard capacitance value. So, three capacitors, C2-C4, are required to be connected in series to achieve this equivalent capacitance. This isn't necessarily a bad thing as a benefit to a series connection of three capacitors is a reduction in the overall variation of the equivalent capacitance.

ATMEL REMOTE KEYLESS ENTRY TRANSMITTER 315MHz version (REV B1 APRIL 15, 2003)

Item	Moose	Qty	Ref Designator	Description	Manufacturer	Part Number	Value	Tolerance	Rating	PCB Decal
1		2	C2 C4	0603 SIZE SMT CERAMIC CAPACITOR	Any		6p8F	+.25pF	50V NPO	603
2		1	C3	0603 SIZE SMT CERAMIC CAPACITOR	Any		33pF	5%	50V NPO	603
3		2	C1 C8	0603 SIZE SMT CERAMIC CAPACITOR	Any		100pF	5%	50V NPO	603
4		1	C7	0603 SIZE SMT CERAMIC CAPACITOR	Any		10nF	10%	50V X7R	603
5		1	J1	2032 COIN CELL HOLDER SMT	KEYSTONE	1061				KEYSTONE-1061
6		1	J2	3X2 PIN 0.1" RIGHT ANGLE HEADER	3M	929838-04-03				RTHEAD-2X3
7		1	L2	0603 SIZE CHIP INDUCTOR	COILCRAFT	0603CS-82NXJB	82nH	5%		603
8		4	R1 R2 R3 R4	0603 SURFACE MOUNT RESISTOR	Any		1k	5%	1/16 W	603
9		4	S1 S2 S3 S4	LIGHT TOUCH SWITCH	PANASONIC	EVQ-PPDA25				PANASONIC-EVQ-PP
10	X	1	U1	"SMARTRF" WIRELESS DATA	ATMEL	AT86RF401U				TSSOP20
11	X	1	X1	CSM-7 STYLE SMT CRYSTAL	CRYSTEK	16757	13.125MHz	+/-20ppm	CL 20pF	ECS-CSM-7
12		1	PCB 1	PRINTED CIRCUIT BOARD	JET	AT0308 rev B				

Table 1 - Parts list

Software development for this device can be done using AVRStudio. A recent upgrade, AVR Studio4, now includes drop down menus unique to the AT86RF401. When used with an AVR Starter Kit, STK500, a complete software development environment including editing, assembly, simulation, and serial flash programming can be realized.

But, if you're anxious to start playing with the hardware in the lab, try using the SPI Controller software (included with the AT86RF401U-EK1 Evaluation Kit). The SPI Controller gives you real time access to the key registers within the AT86RF401 that control the RF transmitter using a graphical user interface (GUI) as shown in Figure 2. By connecting the cable & dongle assembly (provided in AT86RF401U-EK1) between the parallel port of your PC and the programming header on the reference design, you'll be ready to go! Once you've connected your hardware and initialized the software, you can toggle the

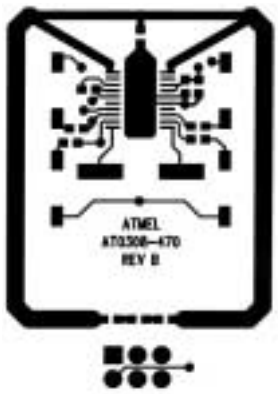

Figure 1a

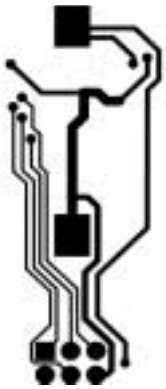

Figure 1b

appropriate bits in various registers to do things like change the output power of the RF signal (PWR_ATTEN[5:0) or activate the RF power amplifier (TX_CNTL[6:4,2]. Be sure to check out some of the canned routines located under the tool button labeled "PRESET FUNCTIONS" as shown in Figure 3. There are quite a few helpful programs that will allow you to evaluate many aspects of the RF transmitter without having to write any software.

Now that you've had a chance to try out the '401 in the lab using the SPI Controller tool, it's time to understand a sample software program that was developed to demonstrate the generation of a constant RF carrier whenever any of the switches S1 through S4 are pressed.

Using the AVRStudio4 and file CW Mode.asm as an example (see Figure 4), the essential elements of the software are:

Figure 2

Figure 3

- initialization of digital logic (e.g. AVR clock divide, stack pointer, I/O definition, etc.) and RF control registers (e.g. fine tuning the VCO, defining the PLL lock detector criteria, selecting output power, etc.)
- controlling the RF signal
- entering the sleep mode after RF transmission is complete

Upon power up, the program counter is reset to 0x0000 and execution begins at the "Reset" label. Initialization starts with establishing the AVR clock divider ratio and defining the stack pointer address. After these tasks are completed the "VCO" subroutine is called. This subroutine steps through an internal VCO tuning capacitor array to determine the optimal setting for the tuning capacitor array. This tuning process monitors both the PLL's ability to lock (TX_CNTL, Bit[2]) and the value of the VCO's control voltage window comparator (VCO-

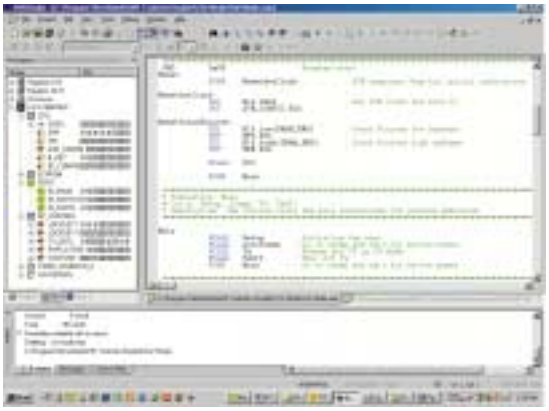

Figure 4

TUNE, Bits[7:6]). When both of these conditions are determined to be acceptable, the value of the tuning capacitor is retained in VCOTUNE, Bits[4:0].

It is important to note that optimal performance of the PLL lock detector has been determined empirically at the factory. Therefore, the constants programmed into registers LOCKDET1 and LOCKDET2 (0x07 and 0x85 respectively) do not require modification in most applications. The final steps of initialization involve the definition of the I/O registers corresponding to switches S1-S4. In this application, they are configured as inputs capable of generating a "button wake-up" (IO_ENAB, bits[5:0] and IO_DATOUT, bits[5:0]). This feature allows a switch depression to awaken the AT86RF401 from its low current sleep mode. Polling of the Button Detect Register (B_DET, bits[5:0]) provides an indication of which I/O was the source of wake up. Care must be taken to clear the bit(s) set in this register prior to entering the sleep mode.

After initialization is complete, generation of the RF carrier is straightforward. When, the appropriate bits in the Transmit Control Register, TX_CNTL, bits[5:4] are set, the RF carrier is routed to the antenna pins of the AT86RF401. This is controlled in the subroutine called "Tx". The RF continues as long as the Button Detect register indicates a switch was pressed (B_DET, bits[5:0]). Once the switch is released, the entire PLL controlling the RF carrier is powered off and the software resumes its sequence of control defined in the main loop of the program, "Main" and quickly enters the sleep mode.

This design was successfully tested for FCC compliance and yielded an output field strength of 85.8 dBuV/m. The FCC limit at 315MHz is 75.62dBuV/m but up to 20dB of relaxation on this limit is allowed if the RF is modulated. This raises the FCC limit to 95.62dBuV/m. This

means the design has a margin of 9.8dB. Results of FCC compliance testing for the fundamental and harmonics of interest are shown in Figures 5 and 6.

The formula to calculate the relaxation factor is:

$dB_{relaxation}$ = 20log(100mS/mS the RF is "on" time during 100mS)

Based on the margin of 9.8dB measured in the lab, we can calculate the maximum amount of RF is "on" during 100mS interval to determine the theoretical boundary of our modulation scheme. Using the equation above we can solve for RF "on" time as follows:

$$20dB \cdot 9.8dB = 20\log(100/t_{RF"on"})$$

$$t_{RF"on"} \leq 30.90mS$$

Based on this information, it would be possible to modulate the RF carrier using On-Off-Keying with a 50% duty cycle at a data rate of up to 10KHz (limited by the AT86RF401) for a duration of 61.8 mS and still meet the limits of the FCC requirements for intermittent operation as defined in FCC part 15.231, "Periodic operation above 70 MHz". Under these conditions, 618 bits of data could be sent at a data rate of 10Kb/S and the transmitter would still be FCC compliant!

As you can see, the AT86RF401 can make adding an RF link to your system easy and economical priced at only $1.36 in quantities of 100K. To get your design to market faster, try ordering an evaluation kit that contains the hardware and software described in this article. Your local Atmel distributor can provide this for $199. Use the order number AT86RF401U-EK1 for a 315MHz design or AT86RF401E-EK1 for a 433.92MHz. Both are available in stock today!

continued on page 40

For more information on this product or for additional design documentation, you may contact the author by phone: 719-540-6873 or email: jgoings@atmel.com. ❑

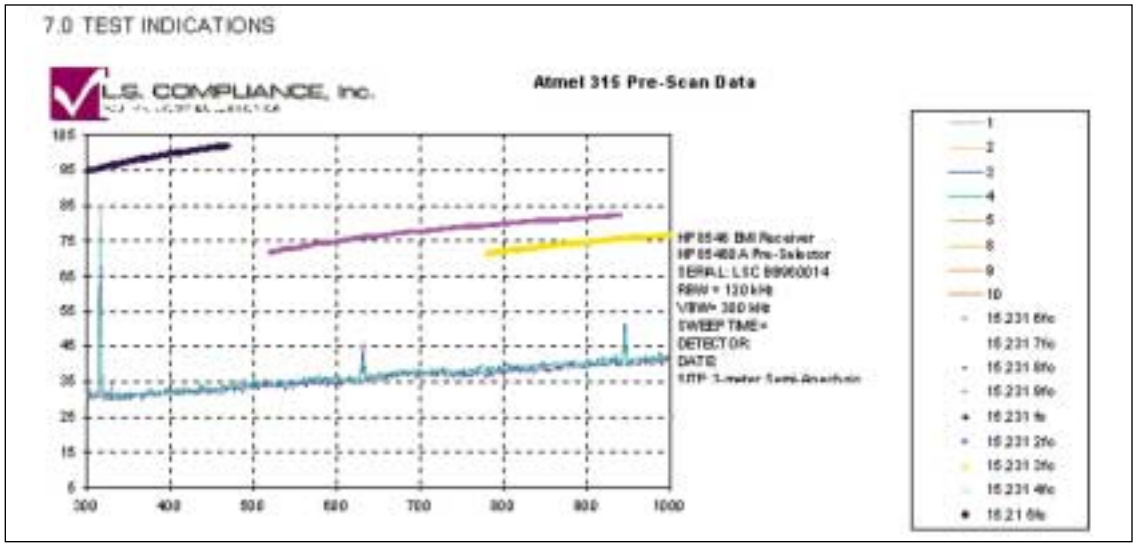

Figure 5

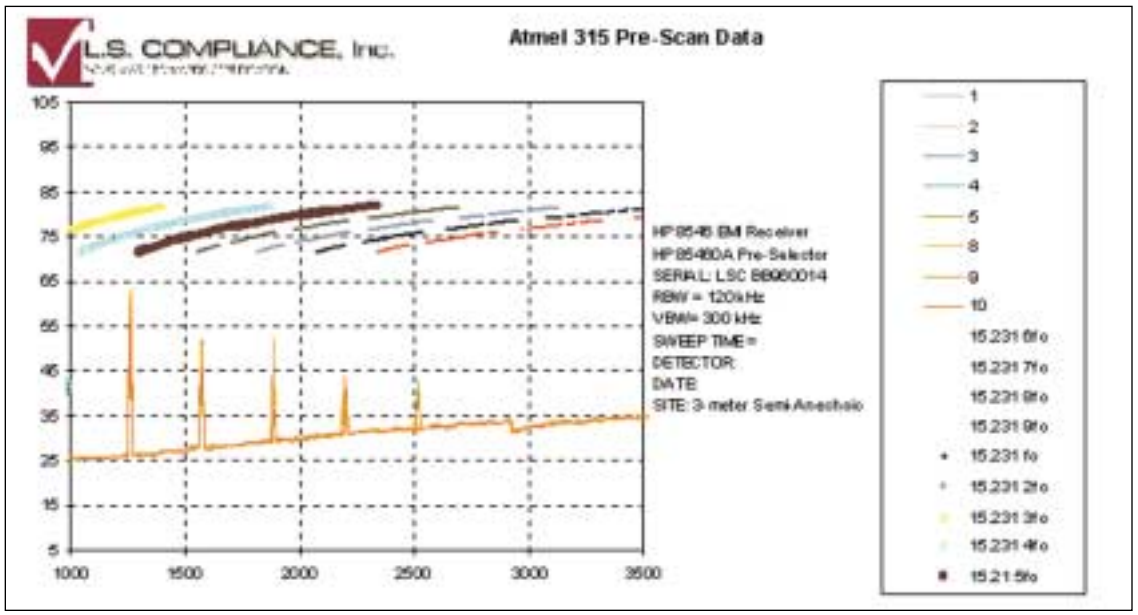

Figure 6