Features

- Watchdog Adjustable
- Over- and Undervoltage Detection of V_{cc} = 5 V
- Standby Modes On/Off via Ignition Pin VKL15
- Internal Time Delay for Output Signal
- Push-pull Output Driver
- Interference and Damage Protection According to ISO/CD 7637
- ESD Protection

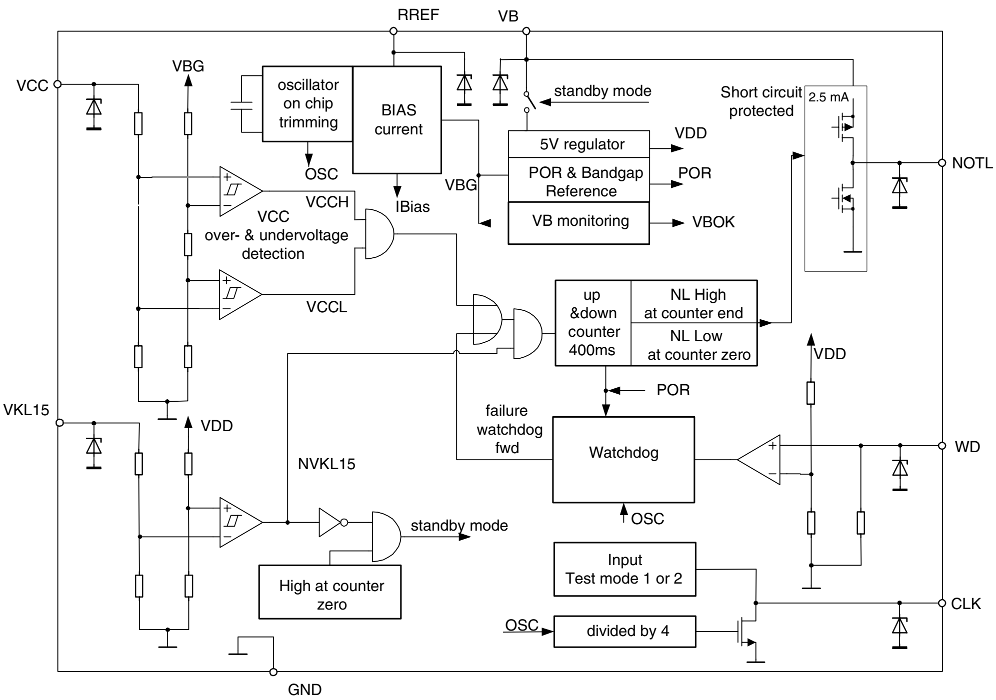
Watchdog IC

ATA6025

Description

The ATA6025 is a monolithic circuit based on Atmel's smart power BCD60-III technology. It is a universal IC for monitoring basic functions of an automotive application. It is possible to monitor the battery voltage (VKL15) and an external 5 V voltage regulator. With the independent watchdog the correct function of a microcontroller can be observed. If a failure occurs, the output NOTL switches to high after a time delay. During standby mode the current consumption is reduced to a minimum.

Figure 1. Block Diagram



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Pin Configuration

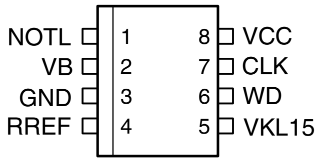


Figure 2. Pinning SO8

Pin Description

Pin	Symbol	Function
1	NOTL	Push-pull output driver
2	VB	Voltage supply
3	GND	Ground
4	RREF	Reference voltage to adjust oscillator frequency via resistor Rset
5	VKL15	Input for standby modes on/of via ignition KL15
6	WD	Input for watchdog signal from microcontroller
7	CLK	Clock output signal, open drain
8	VCC	Input for monitoring 5V power supply

Functional Description

Voltage Supply

The IC can be supplied directly from $V_{battery}$. If the voltage at the VB pin is lower than the threshold of V_{VBlo} = 5.76 V, the internal signal V_{BOK} is set to low. If V_{BOK} is low, the monitor function of the IC is completely disabled and the output NOTL is swiched off in all cases (see Figure 5).

If the voltage at pin VKL15 is low, the IC is in standby mode and reduces the current consumption at pin VB < 100 µA.

Oscillator

The frequency f_{CLK} of the internal oscillator is defined by the external resistor RSET and the internal capacitor. Thus, it is possible to vary the oscillator frequency between 4 kHz and 24 kHz.

VKL15 Monitoring

This input is used to monitor the battery voltage at ignition pin VKL15. If the voltage V_{KL15lo} < 1.8 V, the internal signal NVKL15 is set to high (see Figure 5). The IC switches to standby mode. During standby mode the monitor function is disabled and the output NOTL is switched off after the time delay t_{Delay}.

If the output NOTL is switched on and the voltage at VKL15 switches suddenly to low, the internal timer starts and switches the NOTL off after a time delay of t_{Delay} = 400 ms.

VCC Over-/Undervoltage

Via the VCC input an external 5 V voltage regulator is continuously monitored. If the voltage at pin VCC exceeds the voltage of VCC_{hon} > 6.3 V, the failure bit VCCH is set high. If the voltage at pin VCC decreases to a value below VCC_{lon} < 4 V, the internal failure bit VCCL will be set to high (see Figure 3).

This failure bit starts the internal counter and switches the output NOTL on after the time delay of typically t_{Delay}= 400 ms.

If the VCC voltage is inside the tolerance $VCC_{loff} < V_{VCC} < VCC_{hoff}$ the failure signal will be reset and the internal counter counts back to zero. After a time delay of typically t_{Delay} = 400 ms, the output NOTL is switched off again.

Watchdog

A microcontroller can be monitored by a digital window watchdog which accepts an incoming trigger signal T_{WD} of a constant frequency at pin WD for correct operation. If the pulse width T_{WD} between two alternate edges exceeds the time window of To_{WD} > 8.9 ms or if there is no watchdog signal, the failure signal fwd (failure watchdog) is set. In case the pulse width T_{WD} between two alternate edges falls below the time window of Tu_{WD} < 2.6 ms, the failure signal fwd (failure watchdog) is also set. With this fwd signal the internal up counter is activated and after a time delay of t_{Delay} = 400 ms, the output NOTL is switched to high.

If NOTL is high, 16 successive correct watchdog signals T_{WD} within the pulse width of $Tu_{WD} < T_{WD} < To_{WD}$ are needed to create the internal signal nfwd (no failure watchdog) to start the down counter. After a time delay of t_{Delay}= 400 ms, the output NOTL is switched to low (see Figure 4).

Time Delay

The internal time delay is generated by an up/down counter. The clock for the counter is disabled if the voltage at the supply pin VB < 5.76 V. In this case, the internal signal VBOK will be set to low and the output NOTL is directly switched to low.

The direction of counting is set by the watchdog or VCC over- and undervoltage detection. If the VCC monitoring detects an undervoltage condition, the failure signal VCCL (VCC low voltage) is set and starts the up counter. If the VCC monitoring detects an overvoltage condition, the failure signal VCCH (VCC high voltage) is set and starts the up counter.

A failure at the watchdog sets the internal fwd signal (failure watchdog) to high and starts the up counter. If the counter's final value is reached, a Flip Flop is set and switches the output NOTL to high. If no failure signal is set and the window watchdog has counted successive 16 alternate WDI edges then the down counter is started. If the counter reaches the zero value the Flip Flop receives a reset command and switches the output NOTL off.
The down counter is also started if the voltage at input VKL15 is low and switches the output NOTL after t_{Delay} = 400 ms to low (see Figure 5).

Output NOTL

If the voltage at VKL15 is high and if a failure signal is set, the output NOTL switches to high after the internal time delay.

The output is short circuit protected with a current limitation of ISC_{NOTL} = 15 mA.
The maximum output voltage is limited to VC_{NOTL} = 22 V (see Figure 6).

Test Mode

The pin CLK is normaly open or connected to GND. If the internal clock frequency is to be checked, the CLK pin has to be connected with an external resistor Rex = 5 kΩ to a 5 V supply. The measured value is the clock frequency divided by four.

Truth Table

V_{VB}	V_{VCC}	WDI	VKL15	Mode
V_{VB} < 5.76 V	Do not care	Do not care	Low	Standby, NOTL low
			High	NOTL low
7.26 < V_{VB} < 17.5 V	V_{VCC} < 4 V	Do not care	Low	Standby, NOTL low
			High	NOTL high
	4.8 V < V_{VCC} < 5.2 V	Do not care	Low	Standby, NOTL low
		No watchdog failure	High	NOTL low
		Watchdog failure	High	NOTL high
	V_{VCC} > 6.3 V	Do not care	Low	Standby, NOTL low
	V_{VCC} > 6.3 V		High	NOTL high
22 V< V_{VB} < 40 V	V_{VCC} < 4 V	Do not care	Low	Standby, NOTL low
			High	NOTL high (maximum 22 V)
	4.8 V < V_{VCC} < 5.2 V	Do not care	Low	Standby, NOTL low
		No watchdog failure	High	NOTL low
		Watchdog failure	High	NOTL high (maximum 22 V)
	V_{VCC} > 6.3 V	Do not care	Low	Standby, NOTL low
	V_{VCC} > 6.3 V		High	NOTL high

Absolute Maximum Ratings

Parameters	Symbol	Min.	Max.	Unit
Supply voltage	V_{VB}	-0.3	+40	V
Voltage at pins VCC, WD	V_{VCC}, V_{WDI}	-0.3	+30	V
Voltage at pins RREF, CLK	V_{RREF}, V_{CLK}	-0.5	+6	V
Voltage at pin NOTL	V_{NOTL}	-0.3	+22	V
Voltage at pin KL15 (in series with external resistor of 50 kΩ 1%)	V_{KL15}	-0.1	+40	V
Maximum current at pin VCC	I_{VCC}	-100	+0.1	mA
Maximum current at pin VB	I_{VB}	-10	+10	mA
Maximum current in pins CLK, RREF, VKL15, NOTL		-100	+100	mA
Maximum current at pin WD	I_{WD}	-1	+1	mA
ESD classification HBM ESD S.5.1	all pins	2000		V
ESD classification MM JEDEC A115A	all pins	200		V
Power dissipation	P_V		300	mW
Chip temperature	T_J	-40	+150	°C
Operating ambient temperature	T_{amb}	-40	+125	°C
Storage temperature	T_{Stg}	-55	+150	°C

Thermal Resistance

Parameters	Symbol	Value	Unit
Thermal resistance from junction to ambient	R_{thJA}	160	K/W

Electrical Characteristics

V_{VB} = 7.2 to 17.5 V, RKL15 = 50 kΩ 1%, RSET = 22 kΩ 1%, T_{amb} = -40 to 125°C, unless otherwise specified

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
0	**Current Consumption and ESD Clamping**								
0.1	Current consumption in normal mode	V_{VKL15} > 4.5 V V_{VB} =17.5 V NOTL = high I_{NOTL} = -2.5 mA	2	I_{VB}			10	mA	A
0.2	Current consumption in standby mode	Standby: V_{VKL15} < 1.8 V V_{VB} = 17.5 V NOTL = low	2	I_{VBstby}			100	µA	A
0.3	Negative ESD clamping pin VB	to GND, I_{VB} = -10 mA	2	VN_{VB}	-1.4		-0.3	V	A
0.4	Positive ESD clamping pin RREF	to GND, I_{RREF} = 5 mA	4	VP_{RREF}	4		8	V	A
0.5	Positve ESD clamping pin CLK	to GND, I_{CLK} = 20 mA	7	VP_{CLK}	6		10	V	A
0.6	Positve ESD clamping pin VB	to GND, I_{VB} = 5 mA	2	VP_{VB}	41		65	V	A
0.7	Positve ESD clamping pin VKL15	to GND, I_{VKL15} = 1.6 mA	5	VP_{VKL15}	41		65	V	A
0.8	Positve ESD clamping pin NOTL	to GND, I_{NOTL} = 20 mA	1	VP_{NOTL}	31		55	V	A
0.9	Positve ESD clamping pin WD	to GND, I_{WD} = 0.7 mA	6	VP_{WD}	35		55	V	A
0.10	Positve ESD clamping pin VCC	to GND, I_{VCC} = 0.5 mA	8	VP_{VCC}	35		55	V	A
1	**Reference Voltage**								
1.1	Voltage at RREF		4	V_{RREF}	1.14	1.22	1.3	V	A
1.2	Possible values of resistor RREF		4	R_{RREF}	10	22	50	kΩ	A
2	**Oscillator**								
2.1	Oscillator frequency	RSET = 22 kW ±1% at pin CLK with pull-up-resistor to +5 V	7	f_{CLK}	9	10	11	kHz	A
2.2	Oscillator frequency is variable in a range	RSE = 10 kΩ to 50 kΩ ±1%	7	f_{CLK}	3.96		24.2	kHz	A
4	**VB Monitoring**								
4.1	High level threshold		2	V_{VBhi}	5.94		7.26	V	A
4.2	Low level threshold		2	V_{VBlo}	5.76		7.04	V	A
4.3	Hysteresis		2	V_{VBhys}	0.2			V	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Electrical Characteristics (Continued)

V_{VB} = 7.2 to 17.5 V, RKL15 = 50 kΩ 1%, RSET = 22 kΩ 1%, T_{amb} = -40 to 125°C, unless otherwise specified

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
5	**VKL15 Monitoring**								
5.1	Input resistor at VKL15		5	Ri_{KL15}	18		70	kΩ	A
5.2	Low voltage threshold	RKL15 = 50 kΩ ±1%	5	$VKL15_{lo}$	1.8			V	A
5.3	High voltage threshold	RKL15 = 50 kΩ ±1%	5	$VKL15_{hi}$			4.5	V	A
5.4	Hysteresis		5	$VKL15_{hys}$	0.2		1	V	A
6	**VCC Monitoring**								
6.1	Pull-down resistor to GND at pin VCC	V_{VB} = 17.5 V V_{VKL15} = 0 V or $V_{VKL15} = V_{VB}$ V_{VCC} = 5 V	8	Rpd_{VCC}	50		350	kΩ	A
6.2	Undervoltage detection low level		8	$VCCl_{on}$	4			V	A
6.3	Undervoltage detection high level		8	$VCCl_{off}$			4.8	V	A
6.4	Overvoltage detection high level		8	$VCCl_{off}$			6.3	V	A
6.5	Overvoltage detection low level		8	$VCCh_{off}$	5.2			V	A
6.6	Hysteresis of under- and overvoltage detection		8	VCC_{hys}	0.2			V	A
9	**Oscillator Test**								
9.1	Pull-down-resistor	CLK = high, V_{CLK} = 0 to 4.5 V	7	Rpd_{CLK}	6		15	kΩ	A
9.2	Saturation voltage	I_{CLK} = 1.6 mA, CLK = low	7	Vs_{CLK}			0.4	V	A
9.3	Short current	V_{CLK} = 5 V, CLK = low	7	Isc_{CLK}			10	mA	A
10	**Push-pull Output NOTL**								
10.1	Saturation voltage NOTL switched off	I_{NOTL} = 1.8 mA NOTL off	1	$Vsat_{NOTLoff}$			1	V	A
10.2	Short current NOTL if switched off	$V_{NOTL} = V_{VB}$ NOTL off	1	$Isc_{NOTLoff}$			15	mA	A
10.3	Maximum output voltage NOTL	17.5 V < V_{VB} < 30 V I_{NOTL} = -2.5 mA NOTL on	1	$V_{NOTLmax}$	17.5		22	V	A
10.4	Saturation voltage NOTL switched on; guaranteed down to VB low level threshold	$Vsat_{NOTLon}$ = $V_{VB} - V_{NOTL}$ $V_{VKL15} = V_{VB}$ I_{NOTL} = -2.5 mA NOTL on	1	$Vsat_{NOTLon}$			0.25	V	A
10.5	Short current NOTL if switched onf	V_{NOTL} = 0 V NOTL = on	1	Isc_{NOTLon}	-50			mA	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Electrical Characteristics (Continued)

V_{VB} = 7.2 to 17.5 V, RKL15 = 50 kΩ 1%, RSET = 22 kΩ 1%, T_{amb} = -40 to 125°C, unless otherwise specified

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
10.7	Time delay of internal up and down counter		1	t_{Delay}	360	400	450	ms	A
10.8	Rise time at pin NOTL switch on	C_{NOTL} ≤ 200 pF V_{NOTL} from low = 10% to high = 90% V_{VB}	1	tr_{NOTL}			5	µs	A
10.9	Fall time at pin NOTL switch off	C_{NOTL} ≤ 200 pF V_{NOTL} from high = 90% to low = 10% V(VB)	1	tf_{NOTL}			5	µs	A
11	**Watchdog**								
11.1	Pull-down-resistor	V_{VB} = V_{KL15} = 17.5 V	6	Rpd_{WD}	30		200	kΩ	A
11.2	Voltage threshold low		6	$Vlow_{WD}$	1			V	A
11.3	Voltage threshold high		6	$Vhigh_{WD}$			3.5	V	A
11.4	Hysteresis	$Vhys_{WD}$ = $Vhigh_{WD}$ - $Vlow_{WD}$	6	$Vhys_{WD}$	0.5			V	A
11.5	Acceptable low WD pulse width for failure	pulse = high or low RSET = 22 kΩ ±1%	6	Tu_{WD}	2.6	3	3.3	ms	A
11.6	Acceptable high WD pulse width for failure	pulse = high or low RSET = 22 kΩ ±1%	6	To_{WD}	7.1	8	8.9	ms	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Diagrams

Figure 3. VCC Monitoring Diagram

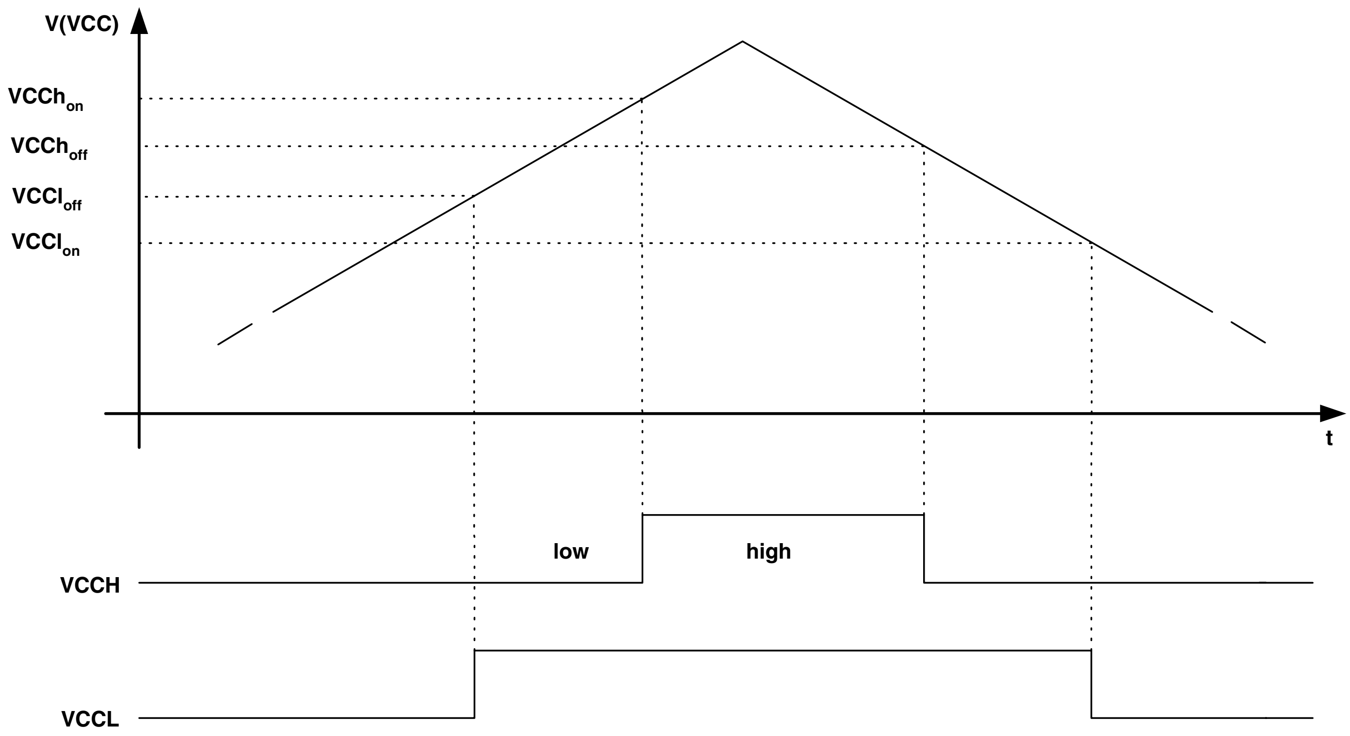


Figure 4. Watchdog Timing Diagram

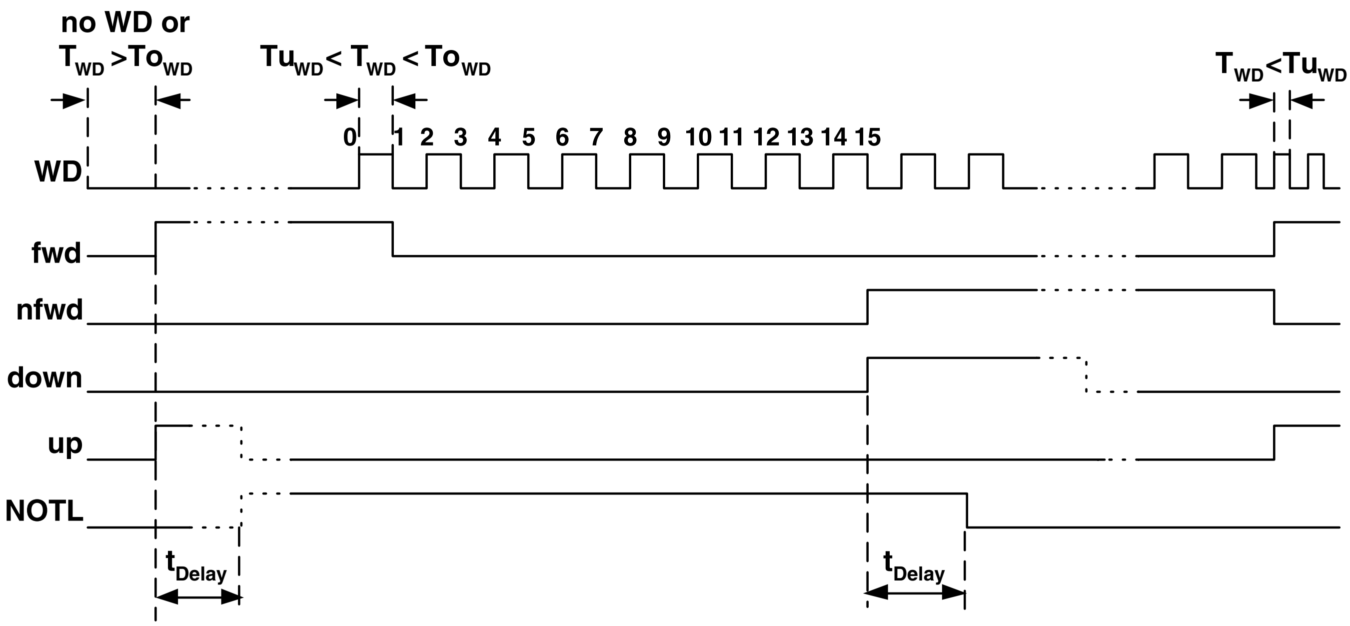


Figure 5. Time Delay Diagram

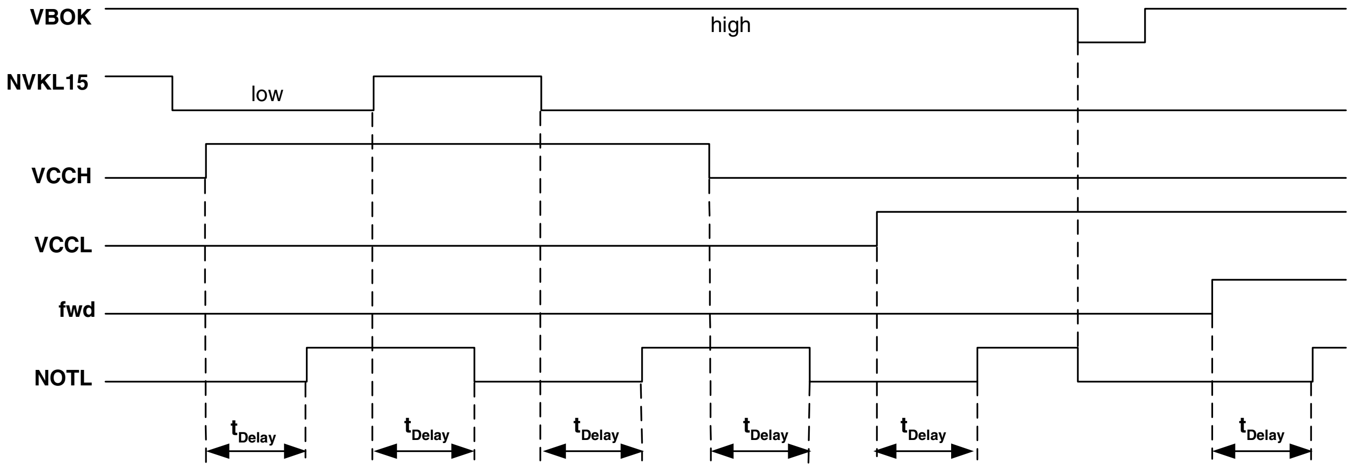


Figure 6. Push-pull Output NOTL

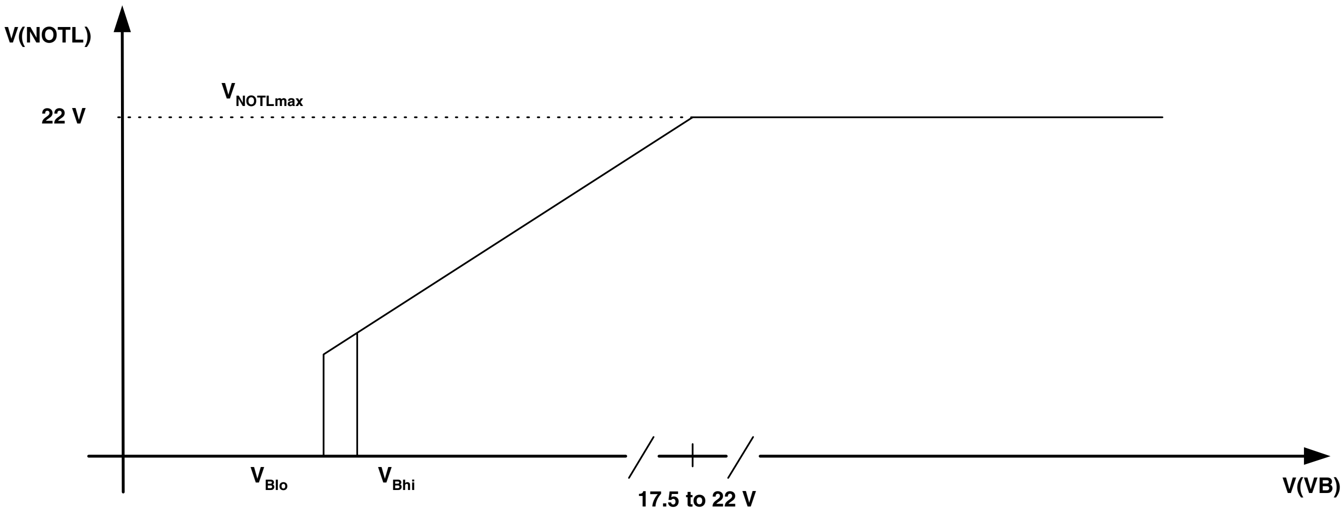
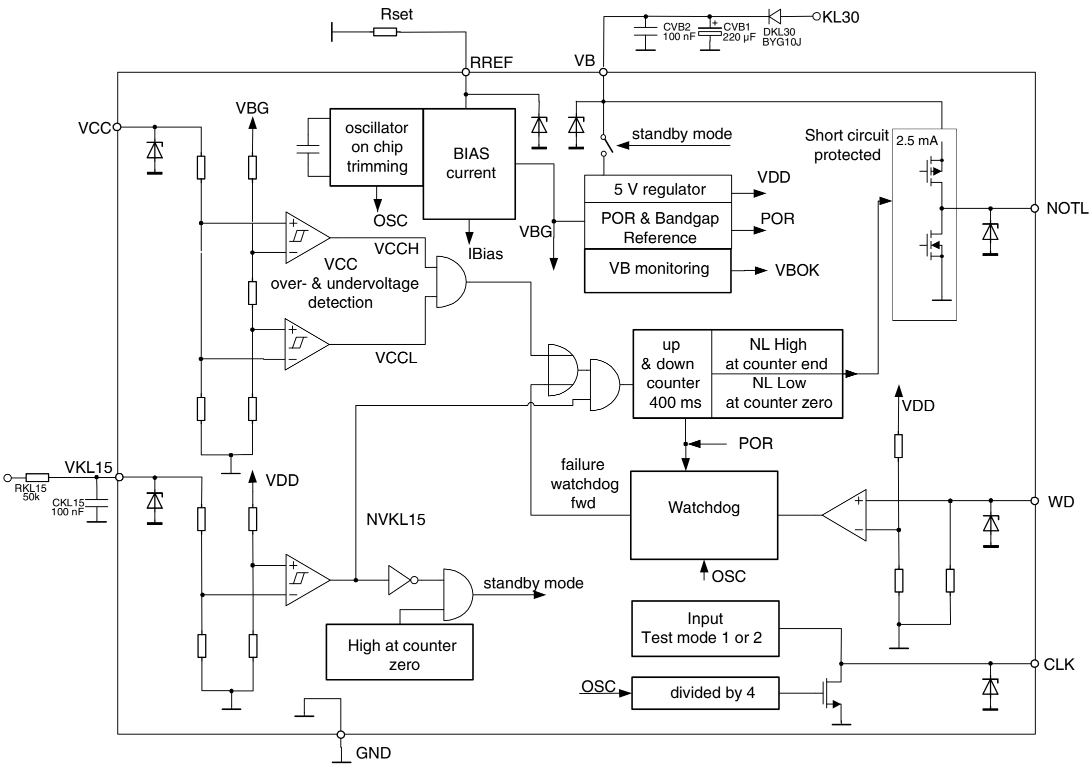


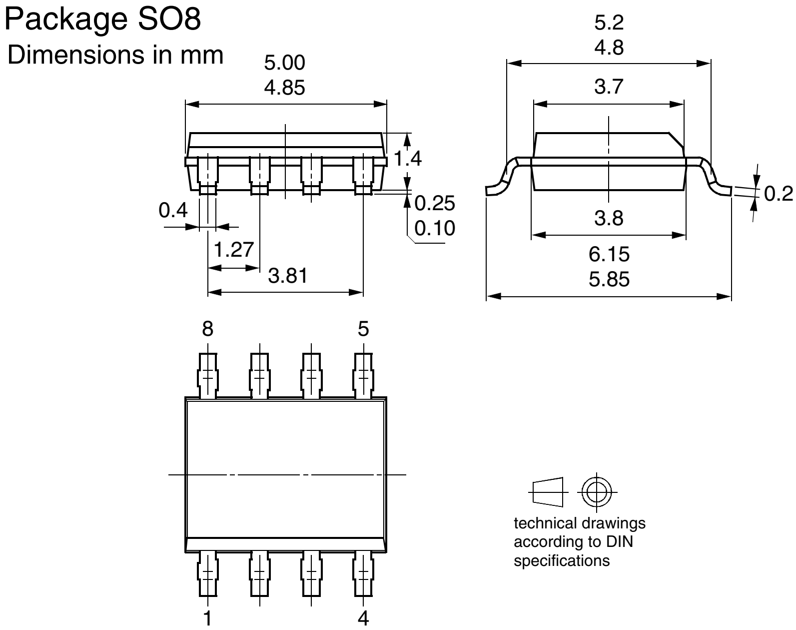
Figure 7. Application Circuit



Ordering Information

Extended Type Number	Package	Remarks
ATA6025	SO8	

Package Information



Atmel Corporation

2325 Orchard Parkway
San Jose, CA 95131
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

Regional Headquarters

Europe
Atmel Sarl
Route des Arsenaux 41
Case Postale 80
CH-1705 Fribourg
Switzerland
Tel: (41) 26-426-5555
Fax: (41) 26-426-5500

Asia
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimshatsui
East Kowloon
Hong Kong
Tel: (852) 2721-9778
Fax: (852) 2722-1369

Japan
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

Atmel Operations

Memory
2325 Orchard Parkway
San Jose, CA 95131
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

Microcontrollers
2325 Orchard Parkway
San Jose, CA 95131
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

La Chantrerie
BP 70602
44306 Nantes Cedex 3, France
Tel: (33) 2-40-18-18-18
Fax: (33) 2-40-18-19-60

ASIC/ASSP/Smart Cards
Zone Industrielle
13106 Rousset Cedex, France
Tel: (33) 4-42-53-60-00
Fax: (33) 4-42-53-60-01

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Scottish Enterprise Technology Park
Maxwell Building
East Kilbride G75 0QR, Scotland
Tel: (44) 1355-803-000
Fax: (44) 1355-242-743

RF/Automotive
Theresienstrasse 2
Postfach 3535
74025 Heilbronn, Germany
Tel: (49) 71-31-67-0
Fax: (49) 71-31-67-2340

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Biometrics/Imaging/Hi-Rel MPU/
High Speed Converters/RF Datacom
Avenue de Rochepleine
BP 123
38521 Saint-Egreve Cedex, France
Tel: (33) 4-76-58-30-00
Fax: (33) 4-76-58-34-80

e-mail
literature@atmel.com

Web Site
http://www.atmel.com

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