Features

- PLL Transmitter IC with Single-ended Output
- High Output Power (6 dBm) at 8.1 mA (315 MHz) and 8.5 mA (433 MHz) Typical Values
- Divide by 24 (ATA5756) and 32 (ATA5757) Blocks for 13 MHz Crystal Frequencies and for Low XTO Start-up Times
- Modulation Scheme ASK/FSK with Internal FSK Switch
- Up to 20 kBaud Manchester Coding, Up to 40 kBaud NRZ Coding
- Power-down Idle and Power-up Modes to Adjust Corresponding Current Consumption through ASK/FSK/Enable Input Pins
- ENABLE Input for Parallel Usage of Controlling Pins in a 3-wire Bus System
- CLK Output Switches ON if the Crystal Current Amplitude has Reached 35% to 80% of its Final Value
- Crystal Oscillator Time Until CLK Output is Activated, Typically 0.6 ms
- Supply Voltage 2.0 V to 3.6 V in Operation Temperature Range of -40° C to +125° C
- ESD Protection at all Pins (4 kV HBM)
- Small Package TSSOP10

Lead Free

Benefits

- Low Parasitic FSK Switch Integrated
- Very Short and Reproducible Time to Transmit Typically < 0.85 ms
- 13.125 MHz/13.56 MHz Crystals Give Opportunity for Small Package Sizes

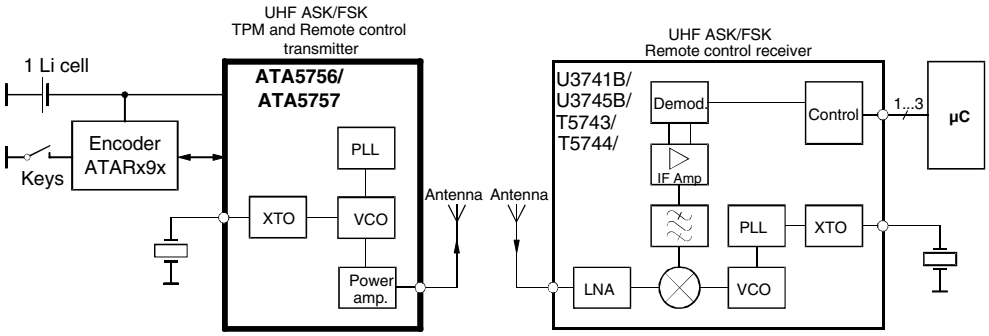
UHF ASK/FSK Transmitter

ATA5756
ATA5757

1. Description

The ATA5756/ATA5757 is a PLL transmitter IC which has been developed for the demands of RF low-cost transmission systems at data rates up to 20 kBaud Manchester coding and 40 kBaud NRZ coding. The transmitting frequency range is 313 MHz to 317 MHz (ATA5756) and 432 MHz to 448 MHz (ATA5757), respectively. It can be used in both FSK and ASK systems. Due to its shorten crystal oscillator settling time it is well suited for Tire Pressure Monitoring (TPM) and for Passive Entry Go applications.

Figure 1-1. System Block Diagram



Rev. 4702I–RKE–11/05

2. Pin Configuration

Figure 2-1. Pinning TSSOP10

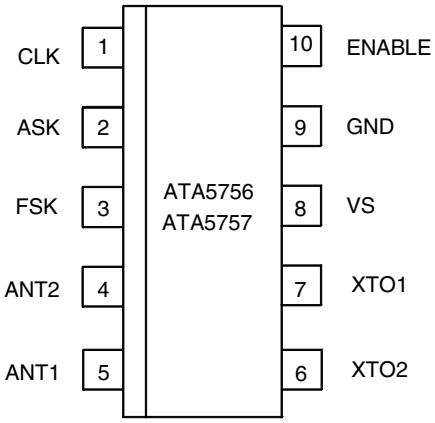


Table 2-1. Pin Description

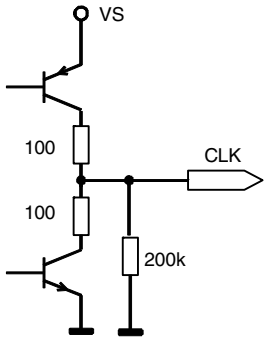
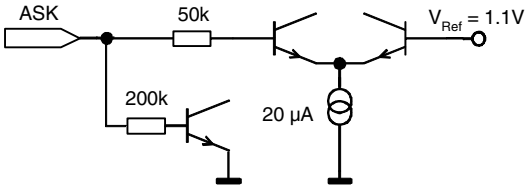
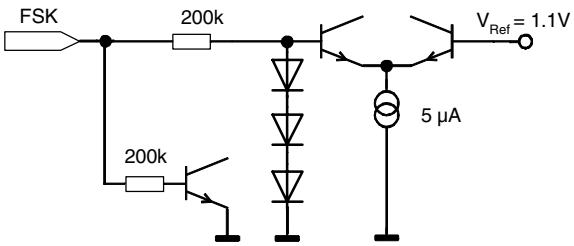
Pin	Symbol	Function	Configuration
1	CLK	Clock output signal for the microcontroller. The clock output frequency is set by the crystal to $f_{XTAL}/8$. The CLK output stays Low in power-down mode and after enabling of the PLL. The CLK output switches on if the oscillation amplitude of the crystal has reached a certain level.	
2	ASK	Switches on the power amplifier for ASK modulation and enables the PLL and XTO if the ENABLE pin is open	
3	FSK	Switches off the FSK switch (switch has high Z if signal at pin FSK is High) and enables the PLL and the XTO if the ENABLE pin is open	

Table 2-1. Pin Description (Continued)

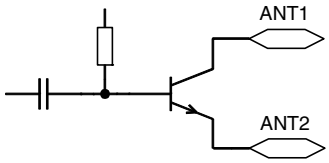
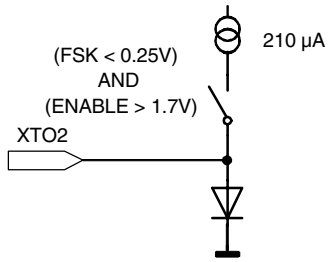
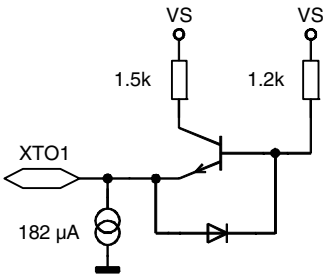
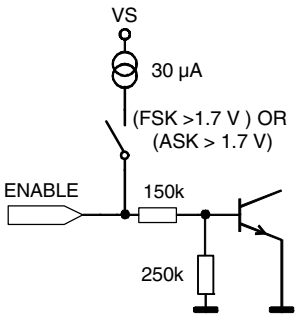
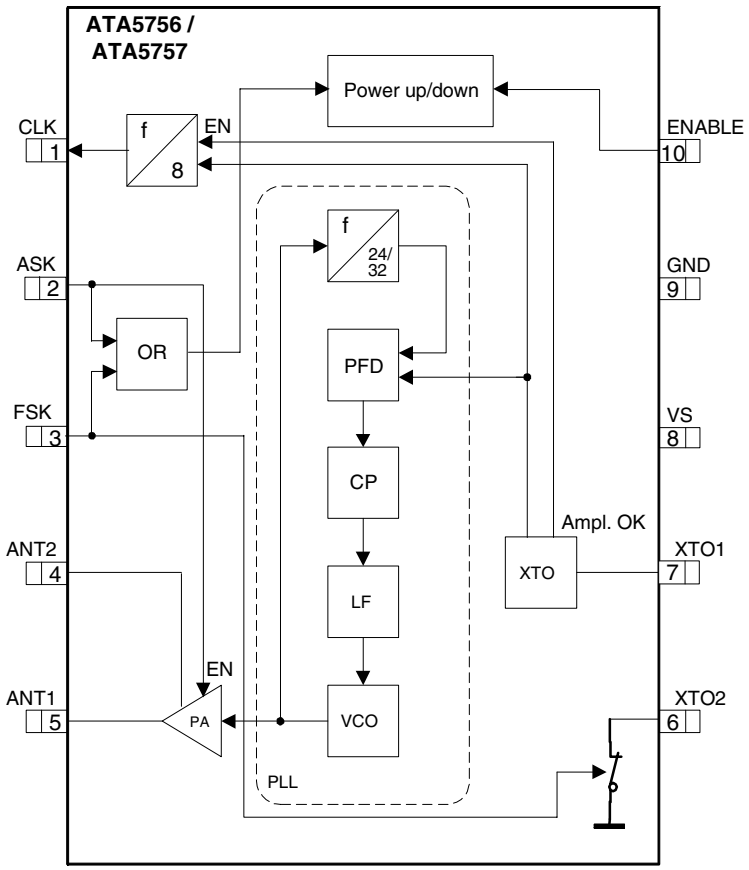
Pin	Symbol	Function	Configuration
4	ANT2	Emitter of antenna output stage	
5	ANT1	Open collector antenna output	
6	XTO2	Diode switch, used for FSK modulation	
7	XTO1	Connection for crystal	
8	VS	Supply voltage	See ESD protection circuitry (see Figure 4-9 on page 14)
9	GND	Ground	See ESD protection circuitry (see Figure 4-9 on page 14)
10	ENABLE	ENABLE input If ENABLE is connected to GND and the ASK or FSK pin is High, the device stays in idle mode. In normal operation ENABLE is left open and ASK or FSK is used to enable the device.	

Figure 2-2. Block Diagram



3. General Description

This fully integrated PLL transmitter allows the design of simple, low-cost RF miniature transmitters for TPM and RKE applications. The VCO is locked to $24 \times f_{XTAL}/32 \times f_{XTAL}$ for ATA5756/ATA5757. Thus, a 13.125 MHz/13.56 MHz crystal is needed for a 315 MHz/433.92 MHz transmitter. All other PLL and VCO peripheral elements are integrated.

The XTO is a series resonance (current mode) oscillator. Only one capacitor and a crystal connected in series to GND are needed as external elements in an ASK system. The internal FSK switch, together with a second capacitor, can be used for FSK modulation. The crystal oscillator needs typically 0.6 ms until the CLK output is activated if a crystal as defined in the electrical characteristics is used (e.g., TPM crystal). For most crystals used in RKE systems, a shorter time will result.

The CLK output is switched on if the amplitude of the current flowing through the crystal has reached 35% to 80% of its final value. This is synchronized with the 1.64/1.69 MHz CLK output. As a result, the first period of the CLK output is always a full period. The PLL is then locked <250 µs after CLK output activation. This means an additional wait time of ≥250 µs is necessary before the PA can be switched on and the data transmission can start. This results in a significantly lower time of about 0.85 ms between enabling the ATA5756/ATA5757 and the beginning of the data transmission which saves battery power especially in tire pressure monitoring systems.

The power amplifier is an open-collector output delivering a current pulse which is nearly independent from the load impedance and can therefore be controlled via the connected load impedance.

This output configuration enables a simple matching to any kind of antenna or to 50 Ω. A high power efficiency for the power amplifier results if an optimized load impedance of $Z_{Load, opt}$ = 380 Ω + j340 Ω (ATA5756) at 315 MHz and $Z_{Load, opt}$ = 280 Ω + j310 Ω (ATA5757) at 433.92 MHz is used at the 3-V supply voltage.

4. Functional Description

If ASK = Low, FSK = Low and ENABLE = open or Low, the circuit is in power-down mode consuming only a very small amount of current so that a lithium cell used as power supply can work for many years.

If the ENABLE pin is left open, ENABLE is the logical OR operation of the ASK and FSK input pins. This means, the IC can be switched on by either the FSK of the ASK input.

If the ENABLE pin is Low and ASK or FSK are High, the IC is in idle mode where the PLL, XTO and power amplifier are off and the microcontroller ports controlling the ASK and FSK inputs can be used to control other devices. This can help to save ports on the microcontroller in systems where other devices with 3-wire interface are used.

With FSK = High and ASK = Low and ENABLE = open or High, the PLL and the XTO are switched on and the power amplifier is off. When the amplitude of the current through the crystal has reached 35% to 80% of its final amplitude, the CLK driver is automatically activated. The CLK output stays Low until the CLK driver has been activated. The driver is activated synchronously with the CLK output frequency, hence, the first pulse on the CLK output is a complete period. The PLL is then locked within <250 µs after the CLK driver has been activated, and the transmitter is then ready for data transmission.

With ASK = High the power amplifier is switched on. This is used to perform the ASK modulation. During ASK modulation the IC is enabled with the FSK or the ENABLE pin.

With FSK = Low the switch at pin XTO2 is closed, with FSK = High the switch is open. To achieve a faster start-up of the crystal oscillator, the FSK pin should be High during start-up of the XTO because the series resistance of the resonator seen from pin XTO1 is lower if the switch is off.

The different modes of the ATA5756/ATA5757 are listed in Table 4-1, the corresponding current consumption values can be found in the table “Electrical Characteristics” on page 15.

Table 4-1. ATA5756/ATA5757 Modes

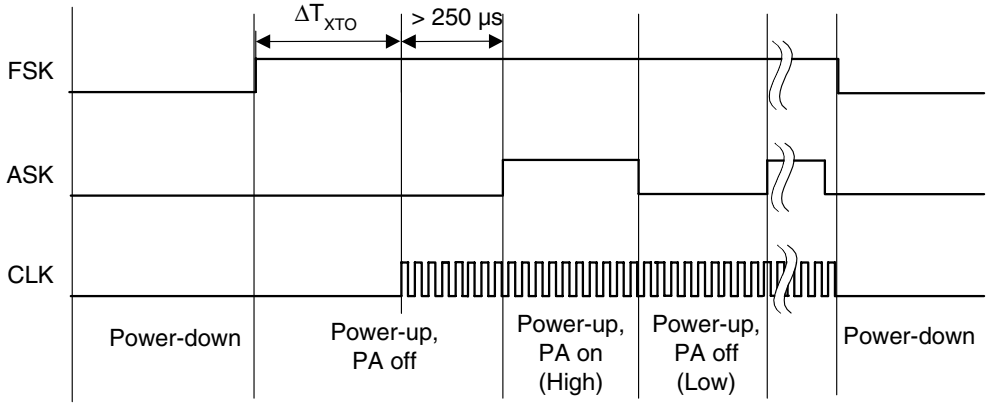
ASK Pin	FSK Pin	ENABLE Pin	Mode
Low	Low	Low/open	Power-down mode, FSK switch High Z
Low	Low	High	Power-up, PA off, FSK switch Low Z
Low	High	High/open	Power-up, PA off, FSK switch High Z
High	Low	High/open	Power-up, PA on, FSK switch Low Z
High	High	High/open	Power-up, PA on, FSK switch High Z
Low/High	High	Low	Idle mode, FSK switch High Z
High	Low/High	Low	Idle mode, FSK switch High Z

4.1 Transmission with ENABLE = open

4.1.1 ASK Mode

The ATA5756/ATA5757 is activated by ENABLE = open, FSK = High, ASK = Low. The microcontroller is then switched to external clocking. After typically 0.6 ms, the CLK driver is activated automatically (i.e., the microcontroller waits until the XTO and CLK are ready). After another time period of ≥250 µs, the PLL is locked and ready to transmit. The output power can then be modulated by means of pin ASK. After transmission, ASK is switched to Low and the microcontroller returns back to internal clocking. Then, the ATA5756/ATA5757 is switched to power-down mode with FSK = Low.

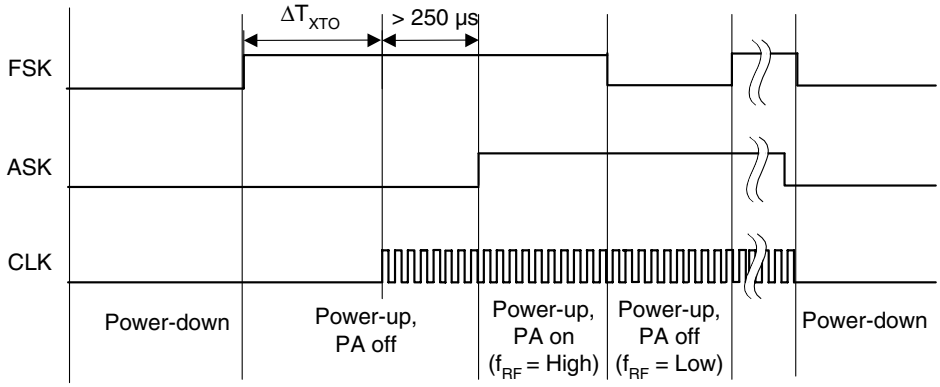
Figure 4-1. Timing ASK Mode with ENABLE not Connected to the Microcontroller



4.1.2 FSK Mode

The ATA5756/ATA5757 is activated by FSK = High, ASK = Low. The microcontroller is then switched to external clocking. After typically 0.6 ms, the CLK driver is activated automatically (i.e., the microcontroller waits until the XTO and CLK are ready. After another time period of ≥250 µs, the PLL is locked and ready to transmit. The power amplifier is switched on with ASK = H. The ATA5756/ATA5757 is then ready for FSK modulation. The microcontroller starts to switch on and off the capacitor between the crystal load capacitor and GND by means of pin FSK, thus, changing the reference frequency of the PLL. IF FSK = L the output frequency is lower, if FSK = H output frequency is higher. After transmission, FSK stays High and ASK is switched to Low and the microcontroller returns back to internal clocking. Then, the ATA5756/ATA5757 is switched to power-down mode with FSK = Low.

Figure 4-2. Timing FSK Mode with ENABLE not Connected to the Microcontroller

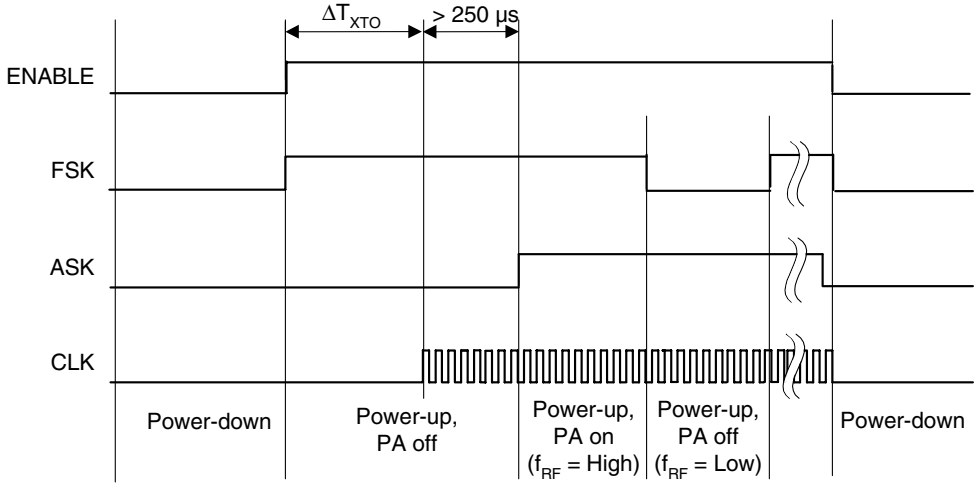


4.2 Transmission with ENABLE = High

4.2.1 FSK Mode

The ATA5756/ATA5757 is activated by ENABLE = High, FSK = High and ASK = Low. The microcontroller is then switched to external clocking. After typically 0.6 ms, the CLK driver is activated automatically (i.e., the microcontroller waits until the XTO and CLK are ready). After another time period of ≥250 µs, the PLL is locked and ready to transmit. The power amplifier is switched on with ASK = H. The ATA5756/ATA5757 is then ready for FSK modulation. The microcontroller starts to switch on and off the capacitor between the crystal load capacitor and GND by means of pin FSK, thus, changing the reference frequency of the PLL. IF FSK = L the output frequency is lower, if FSK = H output frequency is higher. After transmission, ASK is switched to Low and the microcontroller returns back to internal clocking. Then, the ATA5756/ATA5757 is switched to power-down mode with ENABLE = Low and FSK = Low.

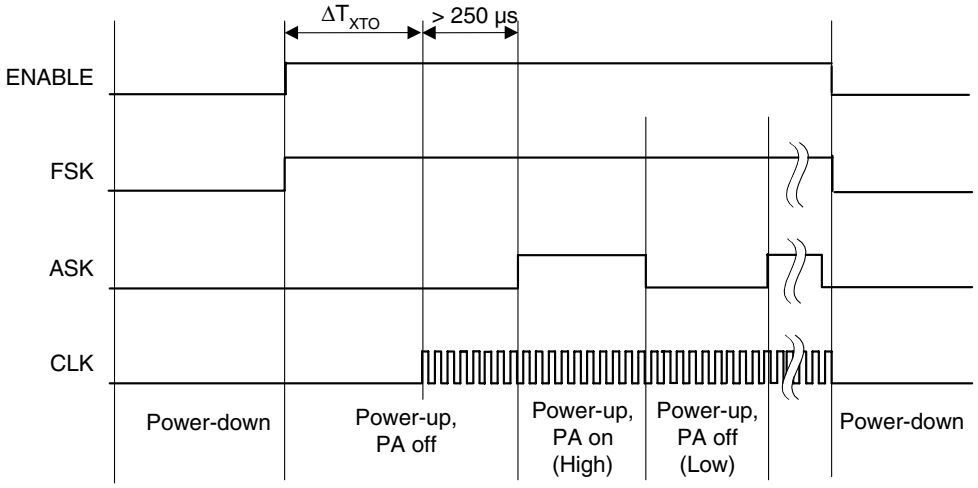
Figure 4-3. Timing FSK Mode with ENABLE Connected to the Microcontroller



4.2.2 ASK Mode

The ATA5756/ATA5757 is activated by ENABLE = High, FSK = High and ASK = Low. After activation the microcontroller is switched to external clocking. After typically 0.6 ms, the CLK driver is activated automatically (the microcontroller waits until the XTO and CLK are ready). After another time period of ≥250 µs, the PLL is locked and ready to transmit. The output power can then be modulated by means of pin ASK. After transmission, ASK is switched to Low and the microcontroller returns back to internal clocking. Then, the ATA5756/ATA5757 is switched to power-down mode with ENABLE = Low and FSK = Low.

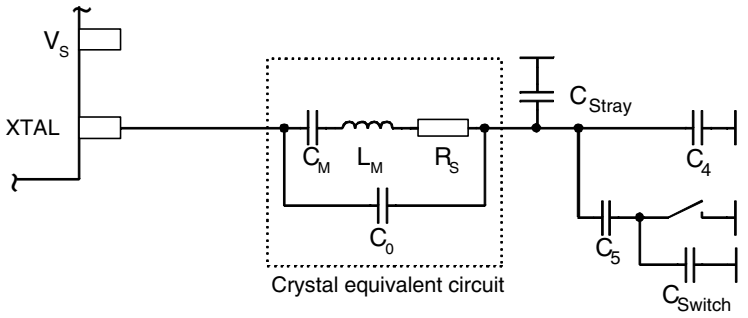
Figure 4-4. Timing ASK Mode with ENABLE Connected to the Microcontroller



4.3 Accuracy of Frequency Deviation

The accuracy of the frequency deviation using the XTAL pulling method is about ±20% if the following tolerances are considered. One important aspect is that the values of C_0 and C_M of typical crystals are strongly correlated which reduces the tolerance of the frequency deviation.

Figure 4-5. Tolerances of Frequency Modulation



Using a crystal with a motional capacitance of C_M = 4.37 fF ±15%, a nominal load capacitance of C_{LNOM} = 18 pF and a parallel capacitance of C_0 = 1.30 pF correlated with C_M results in $C_0 = 297 \times C_M$ (the correlation has a tolerance of 10%, so C_0 = 267 to 326 × C_M). If using the internal FSK switch with C_{Switch} = 0.9 pF ±20% and estimated parasites of C_{Stray} = 0.7 pF ±10%, the resulting C_4 and C_5 values are C_4 = 10 pF ±1% and C_5 = 15 pF ±1% for a nominal frequency deviation of ±19.3 kHz with worst case tolerances of ±15.8 kHz to ±23.2 kHz.

4.4 Accuracy of the Center Frequency

The imaginary part of the impedance in large signal steady state oscillation IM_{XTO}, seen into the pin 7 (XTO1), causes some additional frequency tolerances, due to pulling of the XTO oscillation frequency. These tolerances have to be added to the tolerances of the crystal itself (adjustment tolerance, temperature stability and ageing) and the influence to the center frequency due to tolerances of C_4, C_5, C_{Switch} and C_{Stray}. The nominal value of IM_{XTO} = 110 Ω, C_{Switch} and C_{Stray} should be absorbed into the C_4 and C_5 values by using a crystal with known frequency and choosing C_4 and C_5, so that the XTO center frequency equals the crystal frequency, and the frequency deviation is as expected. Then, from the nominal value, the IM_{XTO} has ±90 Ω tolerances, using the pulling formula $P = -IM_{XTO} \times C_M \times \pi \times f_{XTO}$ with f_{XTO} = 13.56 MHz and C_M = 4.4 fF an additional frequency tolerance of P = ±16.86 ppm results. If using crystals with other C_M the additional frequency tolerance can be calculated in the same way. For example, a lower C_M = 3.1 fF will reduce the frequency tolerance to 11.87 ppm, where a higher C_M = 5.5 fF increases the tolerance to 21.07 ppm.

4.5 CLK Output

An output CLK signal of 1.64 MHz (ATA5756 operating at 315 MHz) and 1.69 MHz (ATA5757 operating at 433.92 MHz) is provided for a connected microcontroller. The delivered signal is CMOS-compatible with a High and Low time of >125 ns if the load capacitance is lower than 20 pF. The CLK output is Low in power-down mode due to an internal pull-down resistor. After enabling the PLL and XTO the signal stays Low until the amplitude of the crystal oscillator has reached 35% to 80% of its amplitude. Then, the CLK output is activated synchronously with its output signal so that the first period of the CLK output signal is a full period.

4.5.1 Clock Pulse Take-over by Microcontroller

The clock of the crystal oscillator can be used for clocking the microcontroller. Atmel's ATARx9x microcontroller family provides the special feature of starting with an integrated RC oscillator to switch on the ATA5756/ATA5757's external clocking and to wait automatically until the CLK output of the ATA5756/ATA5757 is activated. After a time period of 250 µs the message can be sent with crystal accuracy.

4.5.2 Output Matching and Power Setting

The output power is set by the load impedance of the antenna. The maximum output power is achieved with a load impedance of $Z_{Load, opt}$ = 380 Ω + j340 Ω (ATA5756) at 315 MHz and $Z_{Load, opt}$ = 280 Ω + j310 Ω (ATA5757) at 433.92 MHz. A low resistive path to V_S is required to deliver the DC current (see Figure 4-6 on page 10).

The power amplifier delivers a current pulse and the maximum output power is delivered to a resistive load if the 0.66 pF output capacitance of the power amplifier is compensated by the load impedance.

At the ANT1 pin, the RF output amplitude is about V_S - 0.5 V.

The load impedance is defined as the impedance seen from the ATA5756's ANT1, ANT2 into the matching network. Do not mix up this large-signal load impedance with a small-signal input impedance delivered as an input characteristic of RF amplifiers.

The latter is measured from the application into the IC instead of from the IC into the application for a power amplifier.

The 0.66 pF output capacitance absorbed into the load impedance a real impedance of 684 Ω (ATA5756) at 315 MHz and 623 Ω (ATA5757) at 433.92 MHz should be measured with a network analyses at pin 5 (ANT1) with the ATA5756/ATA5757 soldered, an optimized antenna connected and the power amplifier switched off.

Less output power is achieved by lowering the real parallel part where the parallel imaginary part should be kept constant. Lowering the real part of the load impedance also reduces the supply voltage dependency of the output power.

Output power measurement can be done with the circuit as shown in Figure 4-6. Please note that the component values must be changed to compensate the individual board parasitics until the ATA5756/ATA5757 has the right load impedance. Also, the damping of the cable used to measure the output power must be calibrated.

Figure 4-6. Output Power Measurement ATA5756/ATA5757

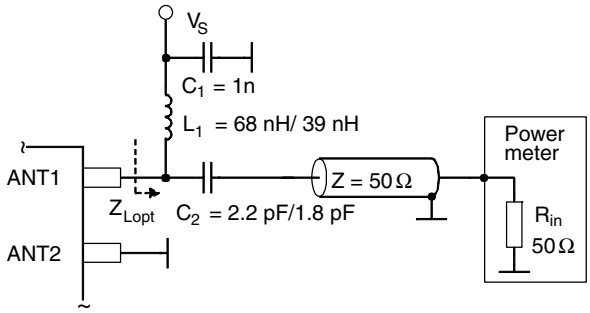


Table 4-2 and Table 4-3 show the output power and the supply current versus temperature and supply voltage.

Table 4-2. Output Power and Supply Current versus Temperature and Supply Voltage for the ATA5756 with Z_{Load} = 380 Ω + j340 Ω (Correlation Tested)

Ambient Temperature	V_S = 2.0 V (dBm/mA)	V_S = 3.0 V (dBm/mA)	V_S = 3.6 V (dBm/mA)
T_{amb} = -40°C	3.1 ±1.5 / 7.2	6.1 +2/-3 / 7.7	7.1 +2/-3 / 7.9
T_{amb} = +25°C	3.0 ±1.5 / 7.5	6.0 ±2 / 8.1	7.4 ±2 / 8.3
T_{amb} = +85°C	3.0 ±1.5 / 7.5	5.8 +2/-3 / 8.2	7.2 +2/-3 / 8.5
T_{amb} = +125°C	2.5 ±1.5 / 7.6	5.5 +2/-3 / 8.2	6.5 +2/-3 / 8.5

Table 4-3. Output Power and Supply Current versus Temperature and Supply Voltage for the ATA5757 with Z_{Load} = 280 Ω + j310 Ω (Correlation Tested)

Ambient Temperature	V_S = 2.0 V (dBm/mA)	V_S = 3.0 V (dBm/mA)	V_S = 3.6 V (dBm/mA)
T_{amb} = -40°C	3.3 ±1.5 / 7.6	6.2 +2/-3 / 8.1	7.1 +2/-3 / 8.4
T_{amb} = +25°C	3.0 ±1.5 / 8.0	6.0 ±2 / 8.5	7.5 ±2 / 8.8
T_{amb} = +85°C	2.8 ±1.5 / 8.0	5.7 +2/-3 / 8.6	6.8 +2/-3 / 8.8
T_{amb} = +125°C	2.7 ±1.5 / 8.1	5.5 +2/-3 / 8.7	6.6 +2/-3 / 8.9

4.6 Application Circuits

For the supply voltage blocking capacitor C_3, a value of 68 nF/X7R is recommended (see Figure 4-7 on page 12 and Figure 4-8 on page 13). C_1 and C_2 are used to match the loop antenna to the power amplifier. For C_2, two capacitors in series should be used to achieve a better tolerance value and to enable it to realize $Z_{Load,opt}$ by using capacitors with standard values.

Together with the pins of ATA5756 and the PCB board wires, $C_{1\ forms}$ a series resonance loop that suppresses the 1st harmonic, hence the position of C_1 on the PCB is important. Normally, the best suppression is achieved when C_1 is placed as close as possible to the pins ANT1 and ANT2.

The loop antenna should not exceed a width of 1.5 mm, otherwise the Q-factor of the loop antenna is too high.

L_1 (50 nH to 100 nH) can be printed on the PCB. C_4 should be selected so that the XTO runs on the load resonance frequency of the crystal. Normally, a value of 10 pF results in a 12 pF load-capacitance crystal due to the board parasitic capacitances and the inductive impedance of the XTO1 pin.

Figure 4-7. ASK Application Circuit

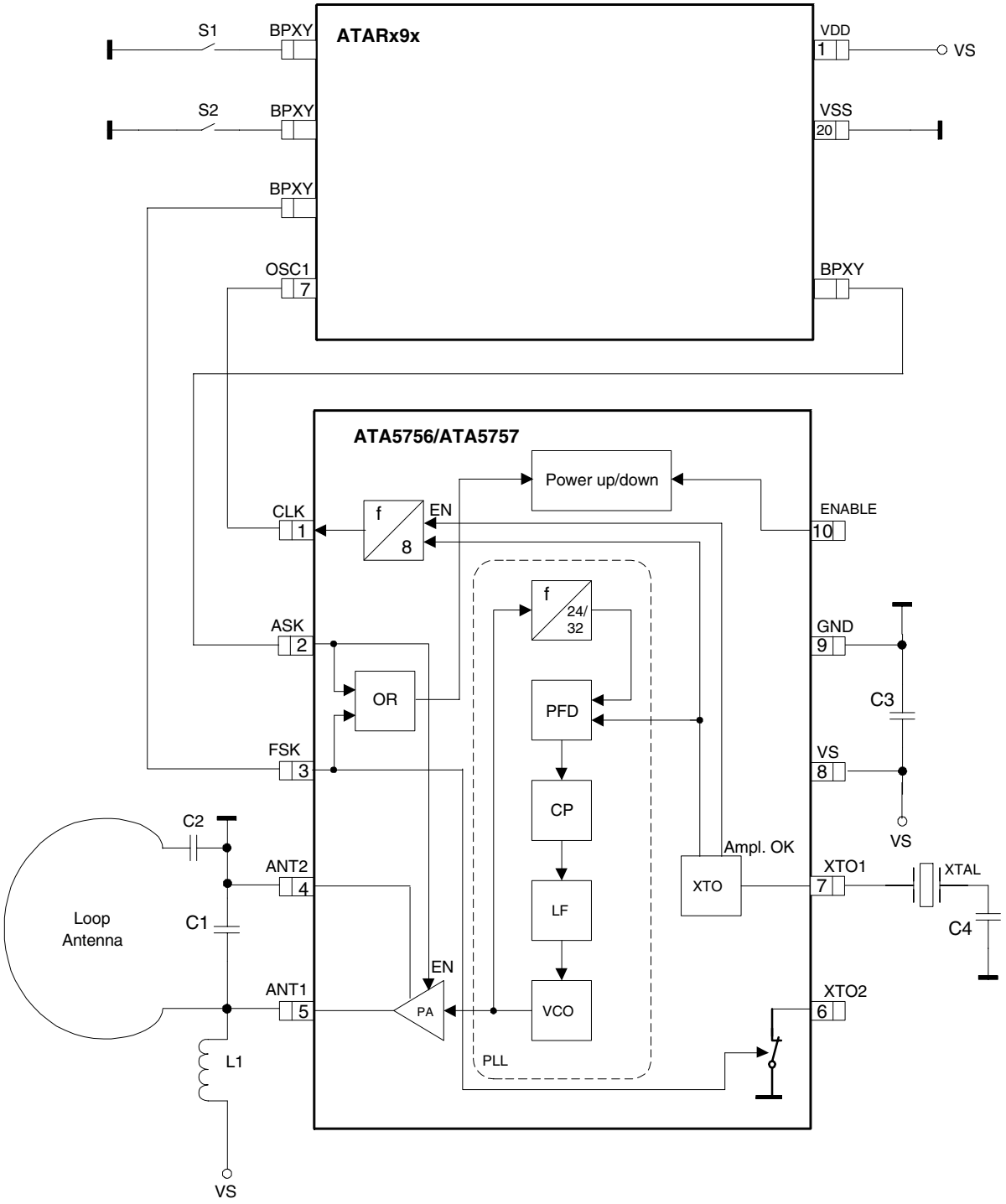


Figure 4-8. FSK Application Circuit

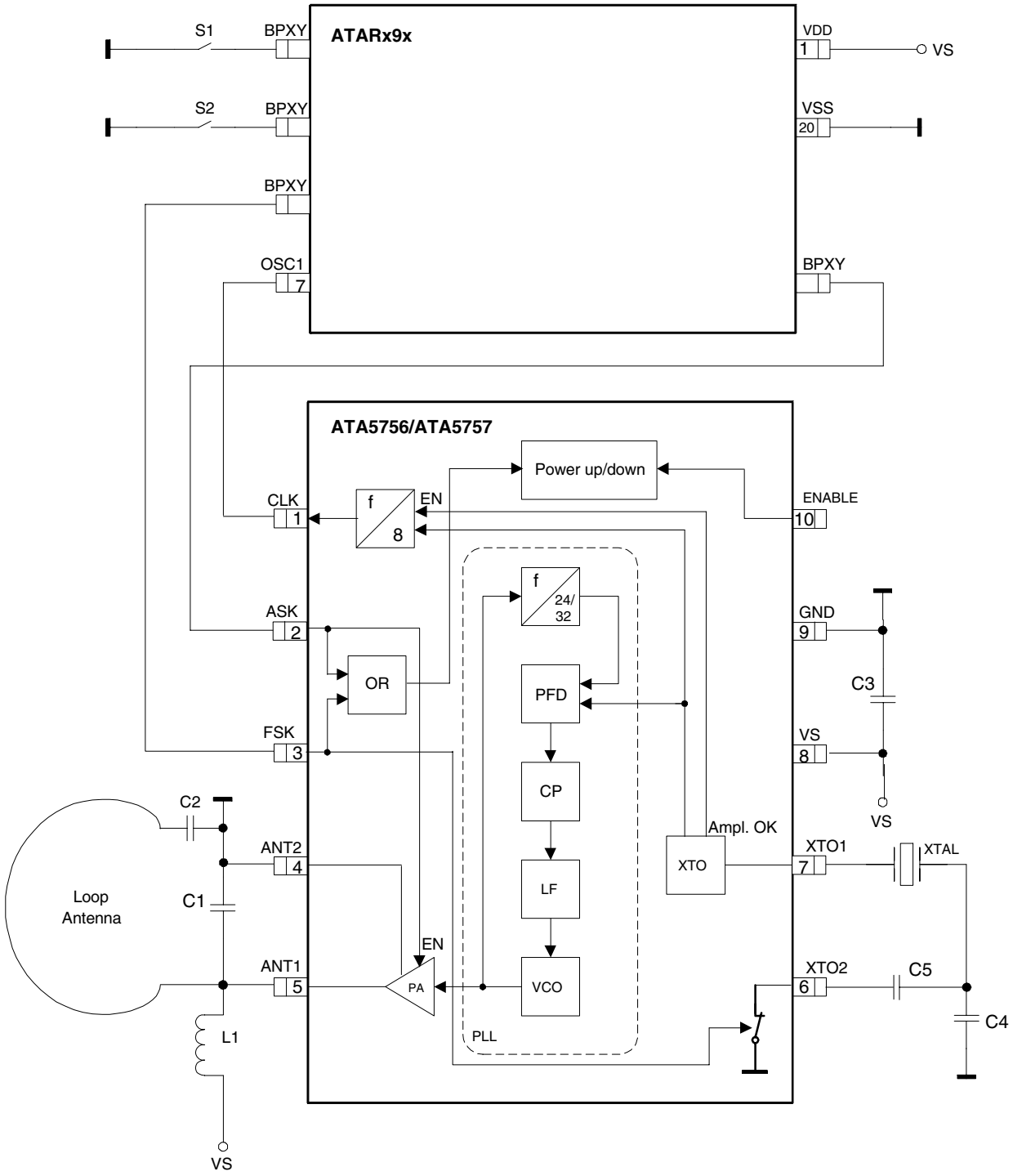
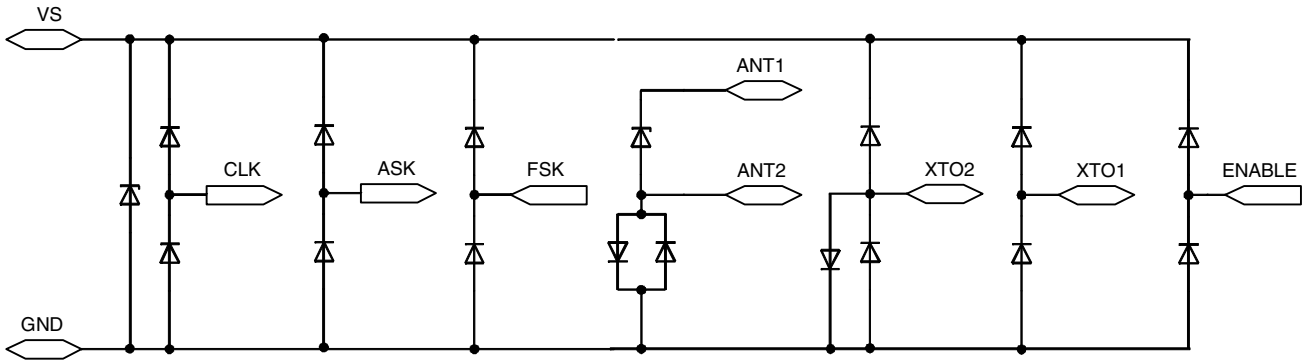


Figure 4-9. ESD Protection Circuit



5. Absolute Maximum Ratings

Parameters	Symbol	Minimum	Maximum	Unit
Supply voltage	V_S		5	V
Power dissipation	P_{tot}		100	mW
Junction temperature	T_j		150	°C
Storage temperature	T_{stg}	-55	125	°C
Ambient temperature	T_{amb1}	-55	125	°C
Ambient temperature in power-down mode for 15 minutes without damage with $V_S \leq 3.2$ V $V_{ENABLE} < 0.25$ V or ENABLE is open, $V_{ASK} < 0.25$ V, $V_{FSK} < 0.25$ V	T_{amb2}		175	°C
Input voltage	V_{maxASK}	-0.3	$(V_S + 0.3)^{(1)}$	V

Note: 1. If $V_S + 0.3$ is higher than 3.7 V, the maximum voltage will be reduced to 3.7 V.

6. Thermal Resistance

Parameters	Symbol	Value	Unit
Junction ambient	R_{thJA}	170	K/W

7. Electrical Characteristics

V_S = 2.0 V to 3.6 V, T_{amb} = -40°C to 125°C unless otherwise specified.
Typical values are given at V_S = 3.0 V and T_{amb} = 25°C. All parameters are referred to GND (Pin 9).

C_M = 4.37 fF, C_0 = 1.3 pF, C_{LNOM} = 18 pF, C_4 = 10 pF, C_5 = 15 pF and $R_S \leq 60\ \Omega$

Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
Supply current, power-down mode	V_{ENABLE} < 0.25 V or ENABLE is open, V_{ASK} < 0.25 V, V_{FSK} < 0.25 V T_{amb} = 25° C T_{amb} = -40° C to +85° C T_{amb} = -40° C to +125° C	I_{S_Off}		1	100 350 7,000	nA nA nA
Supply current, idle mode	V_{ENABLE} < 0.25 V, $V_S \leq$3.2 V ASK,FSK can be Low or High	I_{S_IDLE}			100	µA
Supply current, power-up, PA off, FSK switch High Z	$V_S \leq$3.2 V, V_{FSK} > 1.7 V, V_{ASK} < 0.25 V ENABLE is open	I_S		3.6	4.6	mA
Supply current, power-up, PA on, FSK switch High Z	$V_S \leq$3.2 V, $C_{CLK} \leq$10 pF V_{FSK} > 1.7 V, V_{ASK} > 1.7 V ENABLE is open ATA5756 ATA5757	$I_{S\_Transmit1}$		 8.1 8.5	 9.8 10.5	 mA mA
Supply current, power-up, PA on, FSK Low Z	$V_S \leq$3.2 V, $C_{CLK} \leq$10 pF V_{FSK}< 0.25 V, V_{ASK} > 1.7 V ENABLE is open ATA5756 ATA5757	$I_{S\_Transmit2}$		 8.4 8.8	 10.2 11.0	 mA mA
Output power	V_S = 3.0 V, T_{amb} = 25° C, f = 315 MHz for ATA5756, $Z_{Load,\ opt}$ = (380 + j340) Ω f = 433.92 MHz for ATA5757, $Z_{Load,\ opt}$ = (280 + j310) Ω	P_{Out}	4	6	8	dBm
Output power for the full temperature and supply voltage range	T_{amb} = -40°C to +125° C, V_S = 2.0 V to 3.2 V	P_{Out}	1		8.2	dBm
Spurious emission	$f_{CLK} = f_{XT0}/8$ Load capacitance at pin CLK ≤20 pF $f_0 \pm f_{CLK}$ $f_0 \pm f_{XT0}$ other spurious are lower	Spour		 -42 -60		dBc
Harmonics	With 50 Ωmatching network according to Figure 4-6 on page 10 2nd 3rd			 -16 -15		 dBc dBc
Oscillator frequency XTO (= phase comparator frequency)	$f_{XTO} = f_0/24$ ATA5756 $f_{XTO} = f_0/32$ ATA5757 f_{XTAL} = resonant frequency of the XTAL, C_M = 4.37 fF, load capacitance selected accordingly T_{amb} = -40°C to +85°C T_{amb} = -40°C to +125°C	Δf_{XTO}	 -14.0 -17.5	 f_{XTAL} f_{XTAL}	 +14.0 +17.5	 ppm ppm

7. Electrical Characteristics (Continued)

V_S = 2.0 V to 3.6 V, T_{amb} = -40°C to 125°C unless otherwise specified.
Typical values are given at V_S = 3.0 V and T_{amb} = 25°C. All parameters are referred to GND (Pin 9).

C_M = 4.37 fF, C_0 = 1.3 pF, C_{LNOM} = 18 pF, C_4 = 10 pF, C_5 = 15 pF and $R_S \leq 60\ \Omega$

Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
Imaginary part of XTO1 Impedance in steady state oscillation	Since pulling P is $P = -IM_{XTO} \times C_M \times \pi \times f_{XTO}$ Δf_{XTO} can be calculated out of IM_{XTO} with C_M = 4.37 fF	IM_{XTO}	j20	j110	j200	Ω
Real part of XTO1 impedance in small signal oscillation	This value is important for crystal oscillator start-up	RE_{XTO}	-650	-1100		Ω
Crystal oscillator start-up time	Time between ENABLE of the IC with FSK = H and activation of the CLK output. The CLK is activated synchronously to the output frequency if the current through the XTAL has reached 35% to 80% of its maximum amplitude. Crystal parameters: C_M = 4.37 fF, C_0 = 1.3 pF, C_{LNOM} = 18 pF, C_4 = 10 pF, C_5 = 15 pF, $R_S \leq 60\ \Omega$	ΔT_{XTO}		0.6	1.4	ms
XTO drive current	Current flowing through the crystal in steady state oscillation (peak-to-peak value)	I_{DXTO}		300		µApp
Locking time of the PLL	Time between the activation of CLK and when the PLL is locked (transmitter ready for data transmission)	ΔT_{PLL}			250	µs
PLL loop bandwidth		f_{Loop_PLL}		250		kHz
In loop phase noise PLL	25 kHz distance to carrier	L_{PLL}		-85	-76	dBc/Hz
Phase noise VCO	at 1 MHz at 36 MHz	L_{at1M} L_{at36M}		-90 -121	-84 -115	dBc/Hz dBc/Hz
Frequency range of VCO	ATA5756 ATA5757	f_{VCO}	310 432		317 448	MHz MHz
Clock output frequency (CMOS microcontroller compatible)	ATA5756 ATA5757	f_{CLK}		$f_0/192$ $f_0/256$		MHz
Clock output minimum High and Low time	$C_{Load} \leq 20$ pF, High = 0.8 × Vs, Low = 0.2 × V_S, f_{CLK} < 1.7 MHz	T_{CLKLH}	125			ns
Series resonance resistance of the resonator seen from pin XTO1	For proper detection of the XTO amplitude	R_{s_max}			150	Ω
Capacitive load at Pin XTO1		C_{L_max}			5	pF
FSK modulation frequency rate	This corresponds to 20 kBaud in Manchester coding and 40 kBaud in NRZ coding	f_{MOD_FSK}	0		20	kHz
FSK switch OFF resistance	High Z	R_{SWIT_OFF}	50			kΩ
FSK switch OFF capacitance	High Z capacitance	C_{SWIT_OFF}	0.75	0.9	1.1	pF
FSK switch ON resistance	Low Z	R_{SWIT_ON}		130	175	Ω
ASK modulation frequency rate	Duty cycle of the modulation signal = 50%, this corresponds to 20 kBaud in Manchester coding and 40 kBaud in NRZ coding	f_{MOD_ASK}	0		20	kHz

7. Electrical Characteristics (Continued)

V_S = 2.0 V to 3.6 V, T_{amb} = -40°C to 125°C unless otherwise specified.
Typical values are given at V_S = 3.0 V and T_{amb} = 25°C. All parameters are referred to GND (Pin 9).

C_M = 4.37 fF, C_0 = 1.3 pF, C_{LNOM} = 18 pF, C_4 = 10 pF, C_5 = 15 pF and $R_S \leq 60\ \Omega$

Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
ASK input	Low level input voltage	V_{Il}			0.25	V
	High level input voltage	V_{Ih}	1.7		V_S	V
	Input current high	I_{In}			30	µA
FSK input	Low level input voltage	V_{Il}			0.25	V
	High level input voltage	V_{Ih}	1.7		V_S	V
	Input current high	I_{In}			30	µA
ENABLE input	Low level input voltage	V_{Il}			0.25	V
	High level input voltage	V_{Ih}	1.7		V_S	V
	Input current high	I_{Inh}	-40		40	µA
	Input current Low	I_{Inl}	-40		40	µA

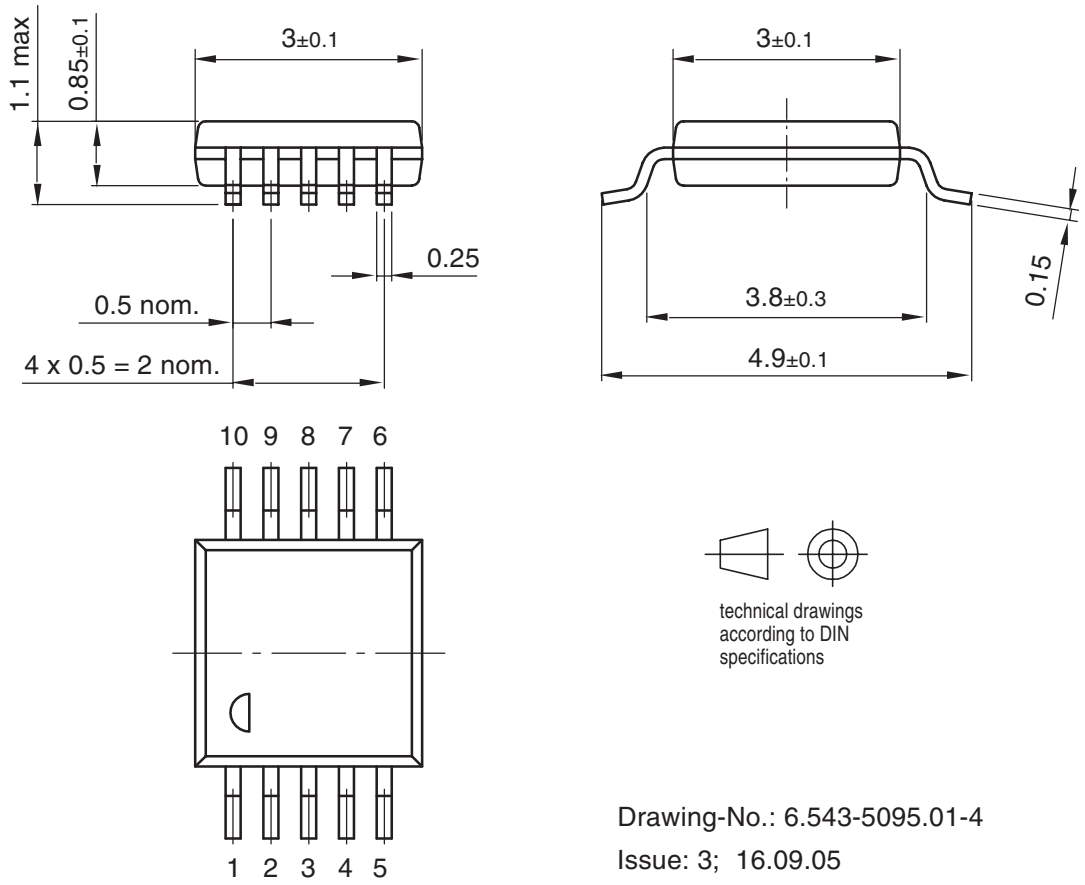
8. Ordering Information

Extended Type Number	Package	Remarks
ATA5756-6DQY ATA5756-6DPJ	TSSOP10	Pb-free
ATA5757-6DQJ	TSSOP10	Pb-free

9. Package Information TSSOP10

Package: TSSOP 10
(acc. to JEDEC Standard MO-187)

Dimensions in mm
Not indicated tolerances ± 0.05



Drawing-No.: 6.543-5095.01-4
Issue: 3; 16.09.05

10. Revision History

Please note that the following page numbers referred to in this section refer to the specific revision mentioned, not to this document.

Revision No.	History
4702I-RKE-11/05	• Put datasheet in a new template • First page: Pb-free logo added • Page 18: Ordering Information and package drawing changed
4702H-RKE-09/04	• Electrical Characteristics table, page 15, row “Output power for the full...”. -> maximum value changed
4702G-RKE-08/04	• Electrical Characteristics table, page 15, row “Output power variation...”. -> the word “variation” deleted
4702F-RKE-08/04	• Preliminary deleted
4702E-RKE-07/04	• Abs. Max. Ratings table (page 14): row “Input voltage” added • Abs. Max. Ratings table (page 14): table note 1 added • El. Char. table (page 17): rows “ASK input”, “FSK input“, “ENABLE input” maximum values changed

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