



# CY74FCT2646T

SCCS043 - September 1994 - Revised March 2000

## 8-Bit Registered Transceiver

### Features

- Function and pinout compatible with FCT and F logic
- FCT-C speed at 5.4 ns max.  
FCT-A speed at 6.3 ns max.
- Reduced  $V_{OH}$  (typically = 3.3V) versions of equivalent FCT functions
- 25Ω output series resistors to reduce transmission line reflection noise
- Reduced  $V_{OH}$  (typically=3.3V) versions of equivalent FCT functions
- Edge-rate control circuitry for significantly improved noise characteristics
- Power-off disable feature permits live insertion
- Matched rise and fall times
- ESD > 2000V
- Fully compatible with TTL input and output logic levels
- Sink current 12 mA  
Source current 15 mA
- Independent register for A and B buses
- Extended commercial temp. range of -40°C to +85°C
- Three-state output

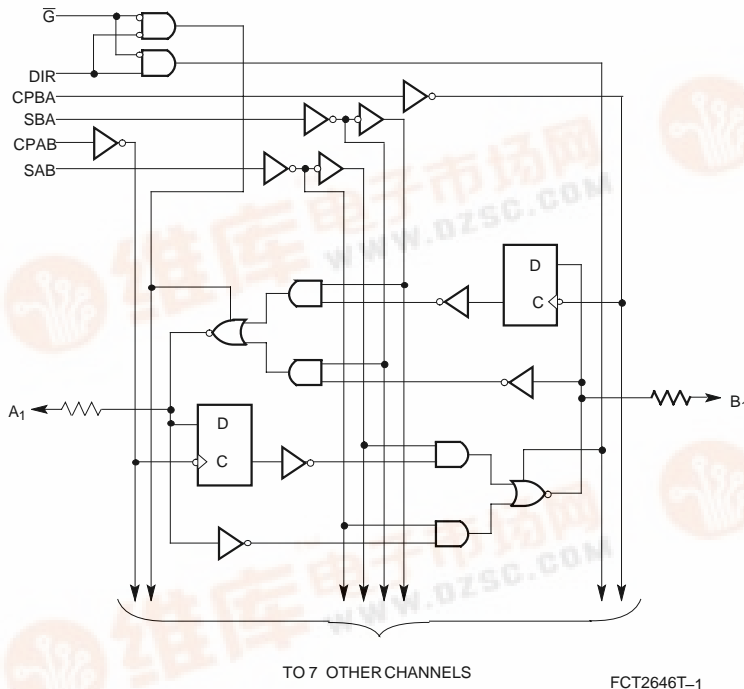
### Functional Description

The FCT2646T consists of a bus transceiver circuit with three-state, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to a HIGH logic level. Enable Control  $\bar{G}$  and direction pins are provided to control the transceiver function. On-chip termination resistors have been added to the outputs to reduce system noise caused by reflections so that the FCT2646T can be used to replace the FCT646T in an existing design.

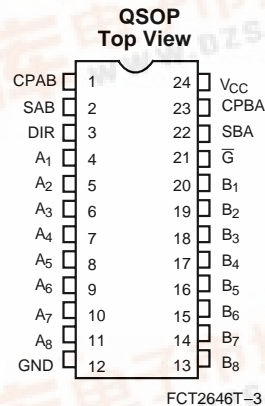
In the transceiver mode, data present at the high impedance port may be stored in either the A or B register, or in both. Select controls can multiplex stored and real-time (transparent mode) data. The direction control determines which bus will receive data when the enable control  $\bar{G}$  is Active LOW. In the isolation mode (enable control  $\bar{G}$  HIGH), A data may be stored in the B register and/or B data may be stored in the A register.

The outputs are designed with a power-off disable feature to allow for live insertion of boards.

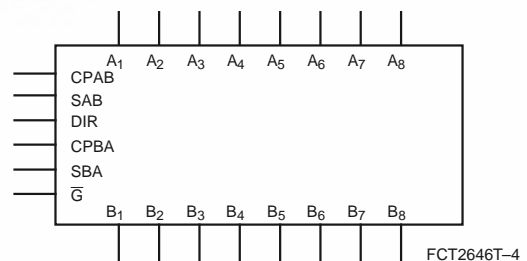
### Functional Block Diagram



### Pin Configurations

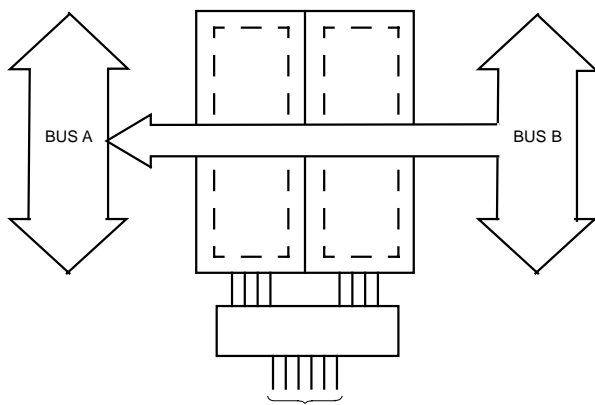


### Logic Block Diagram



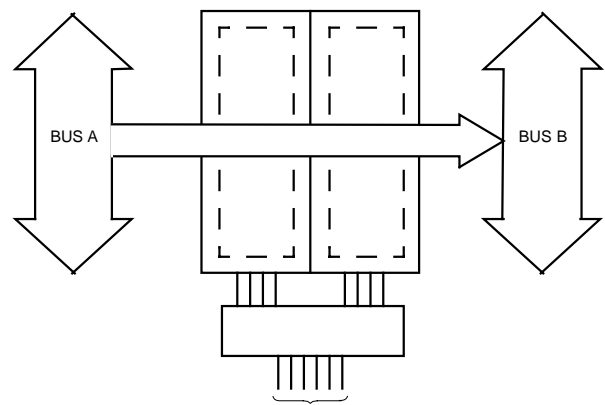
**Pin Description**

| Name           | Description                                     |
|----------------|---|
| A              | Data Register A Inputs, Data Register B Outputs |
| B              | Data Register B Inputs, Data Register A Outputs |
| CPAB, CPBA     | Clock Pulse Inputs                              |
| SAB, SBA       | Output Data Source Select Inputs                |
| DIR, $\bar{G}$ | Output Enable Inputs                            |



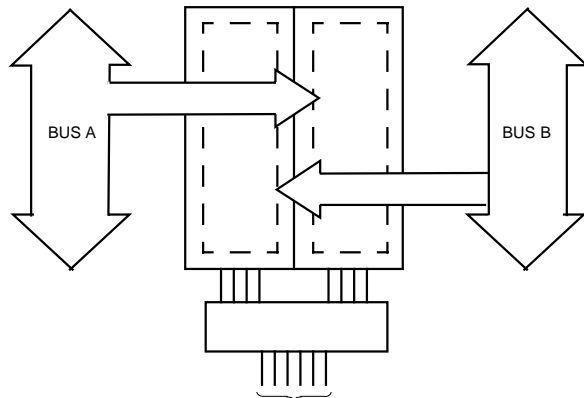
DIR L     $\bar{G}$  L    CPAB X    CPBA X    SAB X    SBA X

Real-Time Transfer  
Bus B to Bus A



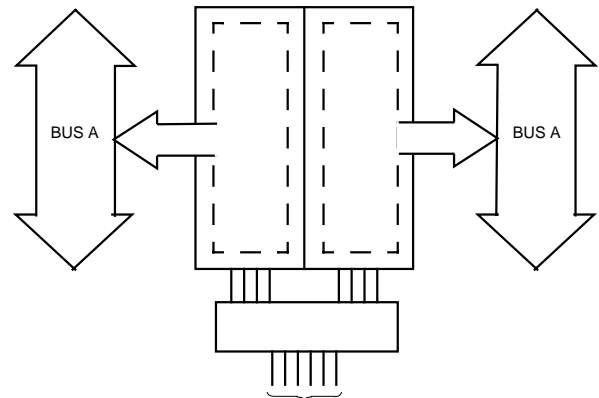
DIR H     $\bar{G}$  L    CPAB X    CPBA X    SAB L    SBA X

Real-Time Transfer  
Bus A to Bus B



DIR H L X     $\bar{G}$  L L H    CPAB J X J    CPBA X J J    SAB X X X    SBA X X X

Storage from  
A and/or B



DIR<sup>[1]</sup> L H     $\bar{G}$  L L    CPAB X H or L    CPBA H or L X    SAB X H    SBA H X

Transfer Stored Data  
to A and/or B

**Note:**

1. Cannot transfer data to A bus and B bus simultaneously.

**Function Table<sup>[2]</sup>**

| Inputs    |        |             |             |        |        | Data I/O <sup>[3]</sup>            |                                    | Operation or Function                               |
|-----------|--------|-------------|-------------|--------|--------|------------------------------------|------------------------------------|---|
| $\bar{G}$ | DIR    | CPAB        | CPBA        | SAB    | SBA    | A <sub>1</sub> thru A <sub>8</sub> | B <sub>1</sub> thru B <sub>8</sub> | FCT2646T  |
| H<br>H    | X<br>X | H or L<br>┐ | H or L<br>┐ | X<br>X | X<br>X | Input                              | Input                              | Isolation<br>Store A and B Data                     |
| L<br>L    | L<br>L | X<br>X      | X<br>H or L | X<br>X | L<br>H | Output                             | Input                              | Real Time B Data to A Bus<br>Stored B Data to A Bus |
| L<br>L    | H<br>H | X<br>H or L | X<br>X      | L<br>H | X<br>X | Input                              | Output                             | Real Time A Data to B Bus<br>Stored A Data to B Bus |

**Maximum Ratings<sup>[4, 5]</sup>**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C

Ambient Temperature with  
Power Applied ..... -65°C to +135°C

Supply Voltage to Ground Potential ..... -0.5V to +7.0V

DC Input Voltage ..... -0.5V to +7.0V

DC Output Voltage ..... -0.5V to +7.0V

DC Output Current (Maximum Sink Current/Pin) ..... 120 mA

Power Dissipation ..... 0.5W

Static Discharge Voltage..... >2001V  
(per MIL-STD-883, Method 3015)

**Operating Range**

| Range      | Ambient Temperature | V <sub>CC</sub> |
|------------|---------------------|-----------------|
| Commercial | -40°C to +85°C      | 5V ± 5%         |

**Electrical Characteristics** Over the Operating Range

| Parameter        | Description                                 | Test Conditions   | Min. | Typ <sup>[6]</sup> | Max. | Unit |
|------------------|---|---|------|--------------------|------|------|
| V <sub>OH</sub>  | Output HIGH Voltage                         | V <sub>CC</sub> =Min., I <sub>OH</sub> =-15 mA          | 2.4  | 3.3                |      | V    |
| V <sub>OL</sub>  | Output LOW Voltage                          | V <sub>CC</sub> =Min., I <sub>OL</sub> =12 mA           |      | 0.3                | 0.55 | V    |
| R <sub>OUT</sub> | Output Resistance                           | V <sub>CC</sub> =Min., I <sub>OL</sub> =12 mA           | 20   | 25                 | 40   | Ω    |
| V <sub>IH</sub>  | Input HIGH Voltage                          |   | 2.0  |                    |      | V    |
| V <sub>IL</sub>  | Input LOW Voltage                           |   |      |                    | 0.8  | V    |
| V <sub>H</sub>   | Hysteresis <sup>[7]</sup>                   | All inputs  |      | 0.2                |      | V    |
| V <sub>IK</sub>  | Input Clamp Diode Voltage                   | V <sub>CC</sub> =Min., I <sub>IN</sub> =-18 mA          |      | -0.7               | -1.2 | V    |
| I <sub>IH</sub>  | Input HIGH Current                          | V <sub>CC</sub> =Max., V <sub>IN</sub> =V <sub>CC</sub> |      |                    | 5    | μA   |
| I <sub>IH</sub>  | Input HIGH Current                          | V <sub>CC</sub> =Max., V <sub>IN</sub> =2.7V            |      |                    | ±1   | μA   |
| I <sub>IL</sub>  | Input LOW Current                           | V <sub>CC</sub> =Max., V <sub>IN</sub> =0.5V            |      |                    | ±1   | μA   |
| I <sub>OS</sub>  | Output Short Circuit Current <sup>[8]</sup> | V <sub>CC</sub> =Max., V <sub>OUT</sub> =0.0V           | -60  | -120               | -225 | mA   |
| I <sub>OFF</sub> | Power-Off Disable                           | V <sub>CC</sub> =0V, V <sub>OUT</sub> =4.5V             |      |                    | ±1   | μA   |

**Notes:**

- H = HIGH Voltage Level. L = LOW Voltage Level. X = Don't Care.
- The data output functions may be enabled or disabled by various signals at the G or DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every LOW-to-HIGH transition of the clock inputs.
- Unless otherwise noted, these limits are over the operating free-air temperature range.
- Unused inputs must always be connected to an appropriate logic voltage level, preferably either V<sub>CC</sub> or ground.
- Typical values are at V<sub>CC</sub>=5.0V, T<sub>A</sub>=+25°C ambient.
- This parameter is specified but not tested.
- Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I<sub>OS</sub> tests should be performed last.

**Capacitance<sup>[7]</sup>**

| Parameter        | Description        | Typ. <sup>[6]</sup> | Max. | Unit |
|------------------|--------------------|---------------------|------|------|
| C <sub>IN</sub>  | Input Capacitance  | 6                   | 10   | pF   |
| C <sub>OUT</sub> | Output Capacitance | 8                   | 12   | pF   |

**Power Supply Characteristics**

| Parameter        | Description                                      | Test Conditions  | Typ. <sup>[6]</sup> | Max.                 | Unit       |
|------------------|--|--|---------------------|----------------------|------------|
| I <sub>CC</sub>  | Quiescent Power Supply Current                   | V <sub>CC</sub> =Max., V <sub>IN</sub> ≤0.2V,<br>V <sub>IN</sub> ≥V <sub>CC</sub> -0.2V  | 0.1                 | 0.2                  | mA         |
| ΔI <sub>CC</sub> | Quiescent Power Supply Current (TTL inputs HIGH) | V <sub>CC</sub> =Max., V <sub>IN</sub> =3.4V, <sup>[9]</sup><br>f <sub>1</sub> =0, Outputs Open  | 0.5                 | 2.0                  | mA         |
| I <sub>CCD</sub> | Dynamic Power Supply Current <sup>[10]</sup>     | V <sub>CC</sub> =Max., One Input Toggling,<br>50% Duty Cycle, Outputs Open,<br>G=DIR=GND, GAB=GBA=GND,<br>V <sub>IN</sub> ≤0.2V or V <sub>IN</sub> ≥V <sub>CC</sub> -0.2V  | 0.06                | 0.12                 | mA/<br>MHz |
| I <sub>C</sub>   | Total Power Supply Current <sup>[11]</sup>       | V <sub>CC</sub> =Max., f <sub>0</sub> =10 MHz,<br>50% Duty Cycle, Outputs Open,<br>One Bit Toggling at f <sub>1</sub> =5 MHz,<br>G=DIR=GND, GAB=GBA=GND,<br>V <sub>IN</sub> ≤0.2V or V <sub>IN</sub> ≥V <sub>CC</sub> -0.2V    | 0.7                 | 1.4                  | mA         |
|                  |  | V <sub>CC</sub> =Max., f <sub>0</sub> =10 MHz,<br>50% Duty Cycle, Outputs Open,<br>One Bit Toggling at f <sub>1</sub> =5 MHz,<br>G=DIR=GND, GAB=GBA=GND,<br>V <sub>IN</sub> =3.4V or V <sub>IN</sub> =GND                      | 1.2                 | 3.4                  | mA         |
|                  |  | V <sub>CC</sub> =Max., f <sub>0</sub> =10 MHz,<br>50% Duty Cycle, Outputs Open,<br>Eight Bits Toggling at f <sub>1</sub> =5 MHz,<br>G=DIR=GND, GAB=GBA=GND,<br>V <sub>IN</sub> ≤0.2V or V <sub>IN</sub> ≥V <sub>CC</sub> -0.2V | 2.8                 | 5.6 <sup>[12]</sup>  | mA         |
|                  |  | V <sub>CC</sub> =Max., f <sub>0</sub> =10 MHz,<br>50% Duty Cycle, Outputs Open,<br>Eight Bits Toggling at f <sub>1</sub> =5 MHz,<br>G=DIR=GND, GAB=GBA=GND,<br>V <sub>IN</sub> =3.4V or V <sub>IN</sub> =GND                   | 5.1                 | 14.6 <sup>[12]</sup> | mA         |

**Notes:**

9. Per TTL driven input (V<sub>IN</sub>=3.4V); all other inputs at V<sub>CC</sub> or GND.
10. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
11. I<sub>C</sub> = I<sub>QUIESCENT</sub> + I<sub>INPUTS</sub> + I<sub>DYNAMIC</sub>  
I<sub>C</sub> = I<sub>CC</sub> + ΔI<sub>CC</sub>D<sub>H</sub>N<sub>T</sub> + I<sub>CCD</sub>(f<sub>0</sub>/2 + f<sub>1</sub>N<sub>1</sub>)  
I<sub>CC</sub> = Quiescent Current with CMOS input levels  
ΔI<sub>CC</sub> = Power Supply Current for a TTL HIGH input (V<sub>IN</sub>=3.4V)  
D<sub>H</sub> = Duty Cycle for TTL inputs HIGH  
N<sub>T</sub> = Number of TTL inputs at D<sub>H</sub>  
I<sub>CCD</sub> = Dynamic Current caused by an input transition pair (HLH or LHL)  
f<sub>0</sub> = Clock frequency for registered devices, otherwise zero  
f<sub>1</sub> = Input signal frequency  
N<sub>1</sub> = Number of inputs changing at f<sub>1</sub>  
All currents are in milliamps and all frequencies are in megahertz.
12. Values for these conditions are examples of the I<sub>CC</sub> formula. These limits are specified but not tested.

**Switching Characteristics** Over the Operating Range<sup>[13]</sup>

| Parameter                            | Description  | CY74FCT2646AT |      | CY74FCT2646CT |      | Unit | Fig. No. <sup>[14]</sup> |
|--------------------------------------|--|---------------|------|---------------|------|------|--------------------------|
|                                      |  | Min.          | Max. | Min.          | Max. |      |                          |
| t <sub>PLH</sub><br>t <sub>PHL</sub> | Propagation Delay Bus to Bus   | 1.5           | 6.3  | 1.5           | 5.4  | ns   | 1, 3                     |
| t <sub>PZH</sub><br>t <sub>PZL</sub> | Output Enable Time Enable to Bus and DIR to A <sub>n</sub> or B <sub>n</sub> | 1.5           | 9.8  | 1.5           | 7.8  | ns   | 1, 7, 8                  |
| t <sub>PHZ</sub><br>t <sub>PLZ</sub> | Output Disable Time $\bar{G}$ to Bus and DIR to Bus                          | 1.5           | 6.3  | 1.5           | 6.3  | ns   | 1, 7, 8                  |
| t <sub>PLH</sub><br>t <sub>PHL</sub> | Propagation Delay Clock to Bus   | 1.5           | 6.3  | 1.5           | 5.7  | ns   | 1, 5                     |
| t <sub>PLH</sub><br>t <sub>PHL</sub> | Propagation Delay SBA or SAB to A or B                                       | 1.5           | 7.7  | 1.5           | 6.2  | ns   | 1, 5                     |
| t <sub>S</sub>                       | Set-Up Time HIGH or LOW, Bus to Clock  | 2.0           |      | 2.0           |      | ns   | 4                        |
| t <sub>H</sub>                       | Hold Time HIGH or LOW, Bus to Clock  | 1.5           |      | 1.5           |      | ns   | 4                        |
| t <sub>W</sub>                       | Pulse Width, <sup>[7]</sup> HIGH or LOW                                      | 5.0           |      | 5.0           |      | ns   | 5                        |

**Notes:**

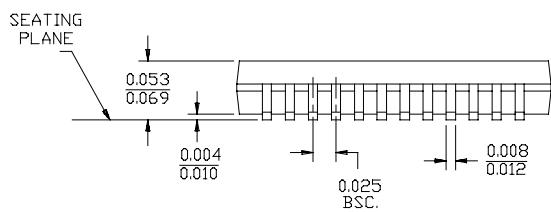
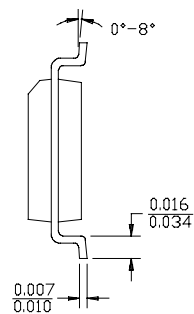
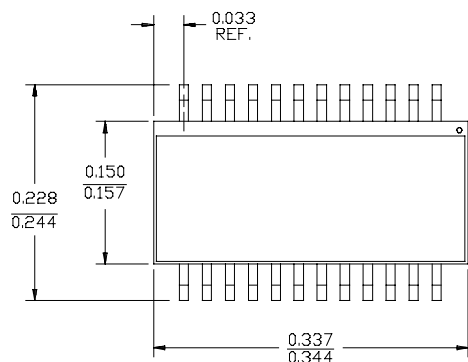
13. Minimum limits are specified but not tested on Propagation Delays.  
 14. See "Parameter Measurement Information" in the General Information section.

**Ordering Information**

| Speed (ns) | Ordering Code    | Package Name | Package Type           | Operating Range |
|------------|------------------|--------------|------------------------|-----------------|
| 5.4        | CY74FCT2646CTQCT | Q13          | 24-Lead (150-Mil) QSOP | Commercial      |
| 6.3        | CY74FCT2646ATQCT | Q13          | 24-Lead (150-Mil) QSOP | Commercial      |

Package Diagrams

24-Lead Quarter Size Outline Q13



DIMENSIONS IN INCHES MIN.  
MAX.  
LEAD COPLANARITY 0.004 MAX.

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