Features

- **Very Low Power Design (≈ 50 mW)**
- **Single IF Concept**
- **2-bit ADC on Chip**
- **Small QFN Package (28 Pins)**
- **Highly Integrated, Few External Components**
- **UHF6 Technology**

Electrostatic sensitive device.
Observe precautions for handling.

GPS Front-end IC

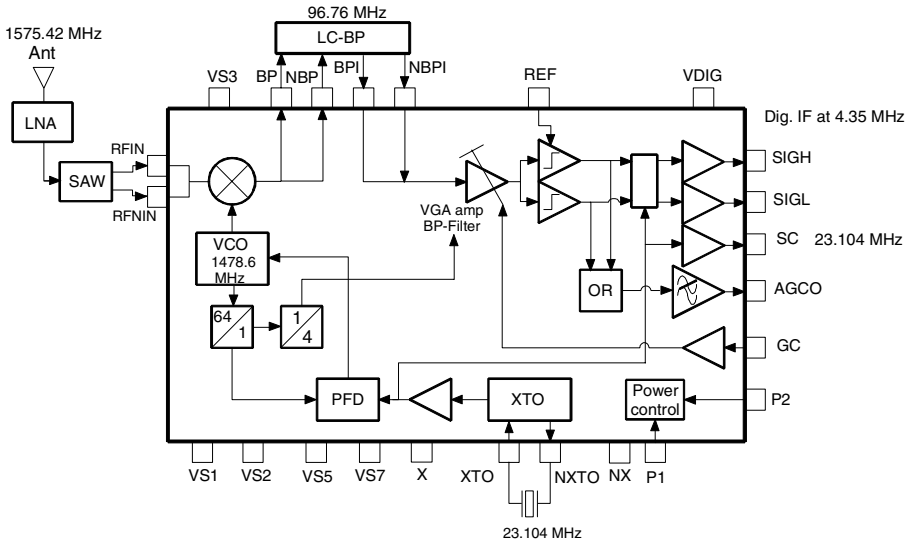
ATR0600

Preliminary

Description

With the growing importance of mobile communication, location awareness is a key feature for more and more products and services. Due to its small size and minimal power consumption, the GPS front-end IC ATR0600 is an ideal solution for mobile applications and navigation systems.

Figure 1. Block Diagram



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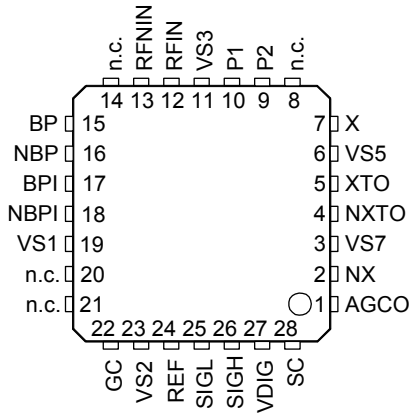
Pin Configuration

Figure 2. Pinning QFN28



Pin Description

Pin	Symbol	Type	Function	Protection Level
1	AGCO	O	Signal level output	ESD3
2	NX	OB	Complementary to X	ESD3
3	VS7	P	ECL - blocks supply	ESD2
4	NXTO	IB	Complementary to XTO	ESD3
5	XTO	IB	Quartz input	ESD3
6	VS5	P	XTO supply	ESD2
7	X	OB	Quartz intermediate output	ESD3
8	n.c.	–	Not connected	–
9	P2	I	Power-up quartz oscillator	ESD3
10	P1	I	Power-up RF part	ESD3
11	VS3	P	Reference supply	ESD2
12	RFIN	IB	RF input 1.575 GHz	ESD3
13	RFNIN	IB	Complementary to RFIN	ESD3
14	n.c.	–	Not connected	–
15	BP	IB	Open-collector output of mixer	ESD3
16	NBP	IB	Complementary to BP	ESD3
17	BPI	IB	IF - filter input	ESD3
18	NBPI	IB	Complementary to BPI	ESD3
19	VS1	P	VCO + mixer + VGA supply	ESD2
20	n.c.	–	Not connected	–
21	n.c.	–	Not connected	–
22	GC	I	Gain control input	ESD3
23	VS2	P	Subsampling unit supply	ESD2
24	REF	O	Defining low threshold voltage	ESD3
25	SIGL	O	Digital interface subsampled output high threshold voltage refered to REF1	ESD3
26	SIGH	O	Digital interface subsampled output low threshold voltage refered to REF2	ESD3
27	VDIG	P	Digital interface supply voltage 1.8 V	ESD2
28	SC	O	Digital interface clock output	ESD3

Functional Description

The specification of GPS receivers for personal mobile applications strongly differs from stand-alone GPS receiver specifications. One reason is the presence of strong blocking signals from mobile transmitters which might cause unacceptable levels of degradation in the carrier-to-noise ratio of a GPS system if not sufficiently suppressed. The other reason is the requirements for very low power consumption.

The ATR0600 GPS receiver IC has been especially designed for GPS applications in mobile phones. From this system point of view, it incorporates highest isolation between GPS and cellular antennas, as well as low power consumption. The ATR0600 contains a low-power single IF design and integrates a complete frequency synthesizer. It is fully functional over a supply-voltage range of 2.7 V to 3.3 V and is housed in a 28-pin QLN package.

The GPS receiver's input signal is a Direct Sequence Spread Spectrum (DSSS) signal at 1575.42 MHz with a 1.023 Mbps Bi-Phase-Shift-Keying (BPSK) modulated spreading code. As the input signal power at the antenna is approximately -140 dBm, the desired signal is below the thermal noise floor.

LNA/Mixer Stage

The ATR0600 receives the L1 GPS signal via an external LNA. The LNA bandwidth should be as narrow as possible to avoid interferences from out-of-band signals (especially from those of the 1800 GSM band).

Combined with the antenna the LNA provides a first filtering of the GPS signal. The LNA in addition should have a power shutdown feature. The shutdown signal will be generated inside the digital section of the GPS receiver. The output of the LNA drives an external SAW filter, which provides the image rejection for the mixer and the isolation of the 1800-MHz GSM band. The output of the SAW filter drives a highly linear mixer which down-converts the GPS signal to an IF of 97.76 MHz.

IF Stage

The mixer directly drives an external LC-bandpath filter. In order to provide the ultimate selectivity of the GPS frequency before the A/D conversion of the receiver part, the signal path of the ATR0600 combines an external filter and a second integrated filter. We recommend to design the external filter as a 2-pole filter with quality factor Q > 25.

VGA Amplifier Stage

The output of the LC-filter drives an on-chip Variable Gain-Controlled amplifier (VGA) which is combined with an integrated IF-bandpath filter to perform additional filtering of GSM jamming signals. The AGC stage provides the additional gain needed to optimally load the signal range of the following analog/digital converter. The AGC control loop can be selected either on-chip close loop or open loop mode. Connecting the AGC_OUT output directly to the AGC_CNTRL input activates the internal control loop.

In that case, the VGA control signal is passed to the VGA via an integrated buffer stage including all necessary filtering (low-pass filter). The external control loop is closed by the baseband IC ATR0620.

A/D Converter Stage

The output of the VGA drives the integrated 1.5-bit analog-to-digital converter stage, which comprises two comparators and two output drivers in order to provide sign and magnitude output bits to the baseband IC ATR0620. The comparator LOW- and HIGH-thresholds (in Figure 1 on page 1 for SIGH and SIGL) are adjustable via external resistor. The OR gate closes the internal AGC control loop.

Power Save Setting Stage

The integrated power-control stage is controlled by the baseband IC ATR0620 via P1 and P2. The input signals control the shutdown of the reference crystal oscillator (P2) or the shutdown of the whole RF section (P1).

Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameters	Symbol	Value	Unit
Supply voltage	V_S	3.7	V
Input voltage	V_{in}	3.7	V
Junction temperature	T_j	125	°C
Storage temperature range	T_{stg}	-40 to +125	°C

Thermal Resistance

Parameters	Symbol	Value	Unit
Junction ambient	R_{thJA}	125	K/W

Recommended Operating Conditions

Parameters	Symbol	Value	Unit
Supply voltage	V_S	2.7 to 3.3	V
Temperature range	Temp	-40 to +85	°C
Input frequency	$f_{in,\ mixer}$	1575.42	MHz
Reference frequency	f_{ref}	23.104	MHz
External IF filter (see Figure 13 on page 9)			
Supply voltage digital interface, pin 27	V_{DD}	1.65 to 2.0	V

Electrical Characteristics

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
1	**Common**								
1.1	Supply current	P1 = P2 = VPU_{on}	3, 6, 11, 19, 23	I_S		18		mA	A
1.2	Supply current XTO	P1 = VPU_{off} P2 = VPU_{on}	6	I_{XTO}		2		mA	A
1.3	Supply current digital interface	P1 = P2 = VPU_{on}	27	I_{DD}		250		µA	A
1.4	Supply current (power down)	P1 = P2 = VPU_{OFF}	3, 6, 11, 19, 23, 27	$I_{S,\ pd}$			20	µA	A
1.5	Total gain	RFIN, RNIN matched, to 50 Ω, V_{GC} = 2.2 V	1	G		95		dB	B
1.6	Noise figure			N_F			6.9	dB	C

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Electrical Characteristics (Continued)

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
2	**Mixer and 1st IF-filter**								
2.1	Output frequency	f_{ref} = 23.104 MHz	15, 16	f_{IF}		96.76		MHz	B
2.2	Input impedance	f_{ref} = 1575 MHz	12, 13	$Z_{in, IF}$		13 - j80		Ω	C
3	**VGA and 2nd IF-filter**								
3.1	Bandpass center frequency	f_{ref} = 23.104 MHz		$f_{in, VGA}$		96.76		MHz	
3.2	Minimum gain	V_{GC} = 1.0 V		$G_{VGA, min}$		0		dB	D
3.3	Maximum gain	V_{GC} = 2.2 V		$G_{VGA, max}$		75		dB	D
3.4	Control-voltage sensitivity	V_{GC} = 2.2 V V_{GC} = 1.0 V		$N_{vga, min}$ $N_{vga, max}$		6.6 150		dB/V dB/V	D D
3.5	Gain-control output cut-off frequency	Without external load		F_{agc_out}		100		kHz	D
3.6	Gain-control output voltage	at 50 pF load	1	V_{agc_out}	1.0		2.2	V	B
4	**Reference Oscillator**								
4.1	XTO phase noise at 100 Hz		28	P_{n100}		-80		dBc/Hz	C
4.2	XTO phase noise at 1 kHz		28	P_{n1k}		-100		dBc/Hz	C
5	**Clock and Data Driver**								
5.1	Clock driver frequency		28	f_{clk}		23.104		MHz	A
5.2	Clock output level	C_{load} = 10 pF	28	$V_{clkhigh}$		0.8 × V_{DD}		V	B, C
5.3	Clock output level	C_{load} = 10 pF	28	V_{clklow}		0.2 × V_{DD}		V	C
5.4	Data output level	C_{load} = 10 pF	25, 26	$V_{datahigh}$		0.8 × V_{DD}		V	C
5.5	Data output level	C_{load} = 10 pF	25, 26	$V_{datalow}$		0.2 × V_{DD}		V	C
6	Power-up, Pins P1 and P2								
6.1	Power-on voltage level on		9, 10	VPU_{on}	0.9			V	C
6.2	Power-on voltage level off		9, 10	VPU_{off}			0.3	V	C
6.3	Power-on delay time		9, 10	$TPU_{on, off}$			6	µs	C

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Interface Description

Figure 3. Clock Interface

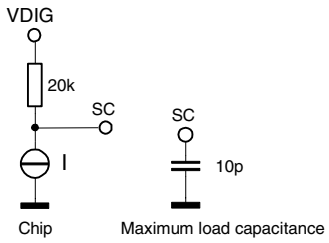


Figure 4. SIGH Interface

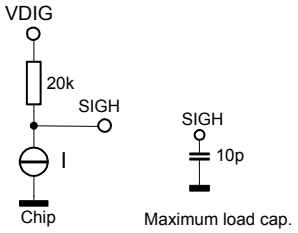


Figure 5. SIGL Interface

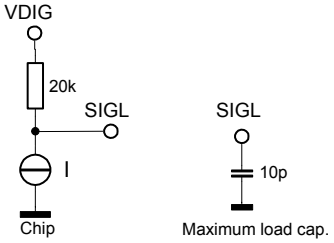


Figure 6. Supply VDIGI Interface

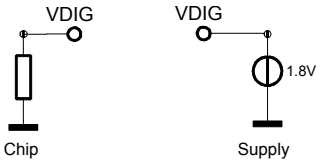


Figure 7. Power Control Interface P1

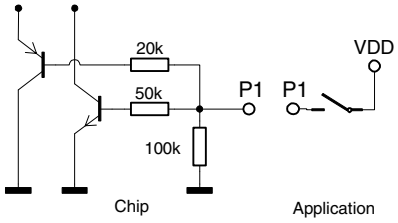


Figure 8. Power Control Interface P2

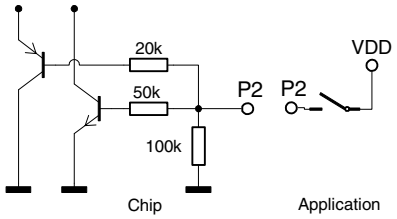


Figure 9. Automatic Gain-control Interface

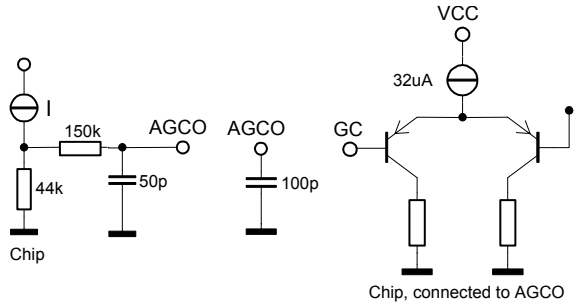


Figure 10. A/D Reference Level-control Interface Ref

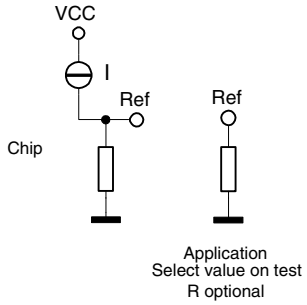


Figure 11. Mixer Input Interface

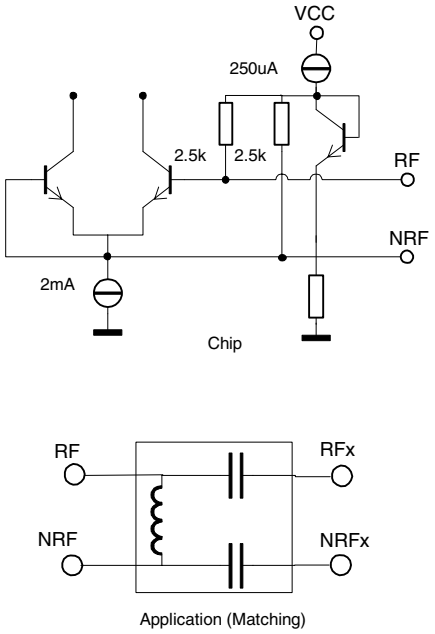


Figure 12. XTO Interface

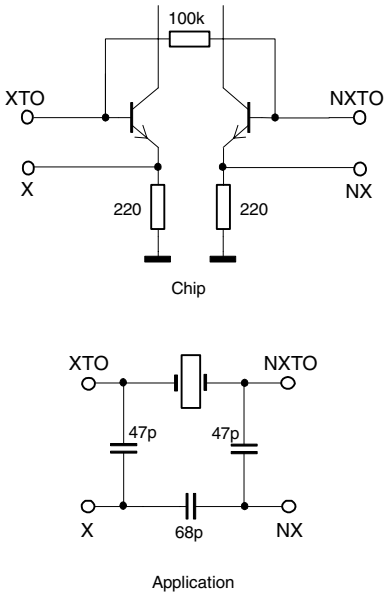


Figure 13. IF-filter Interface

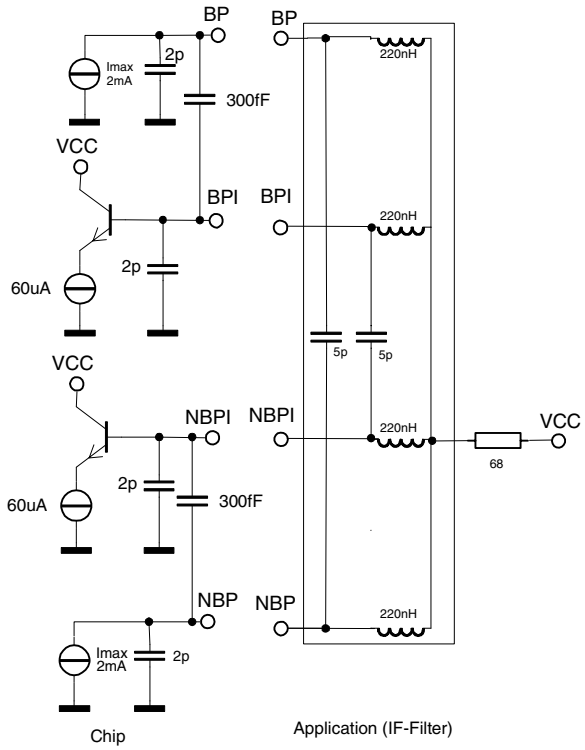
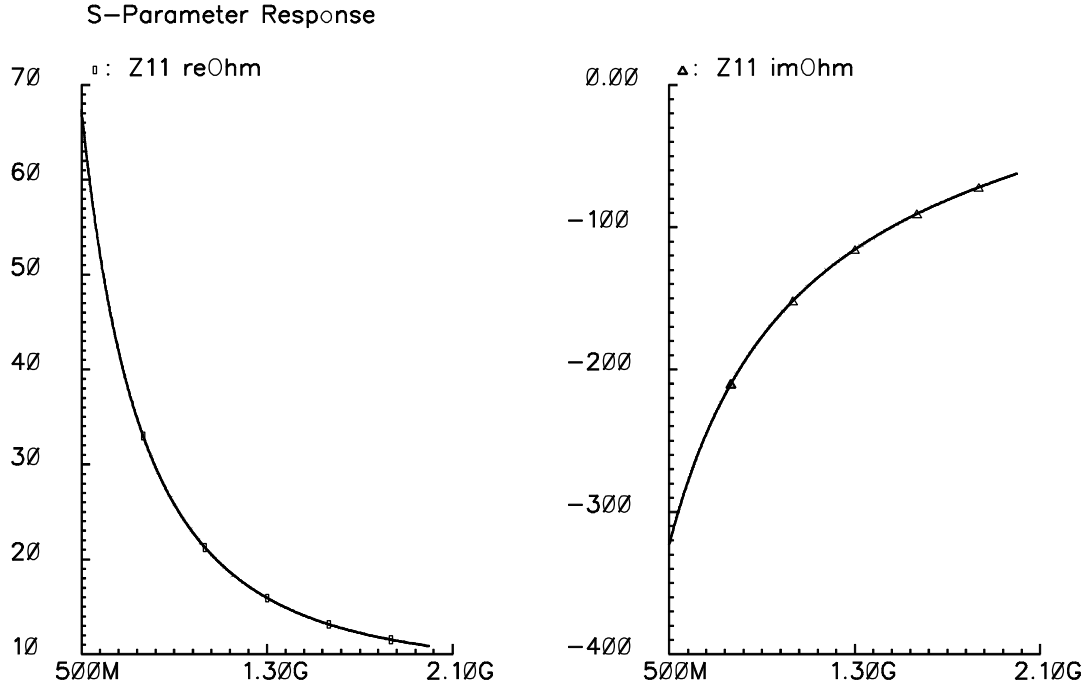


Figure 14. Mixer Input Impedance at RF-NRF



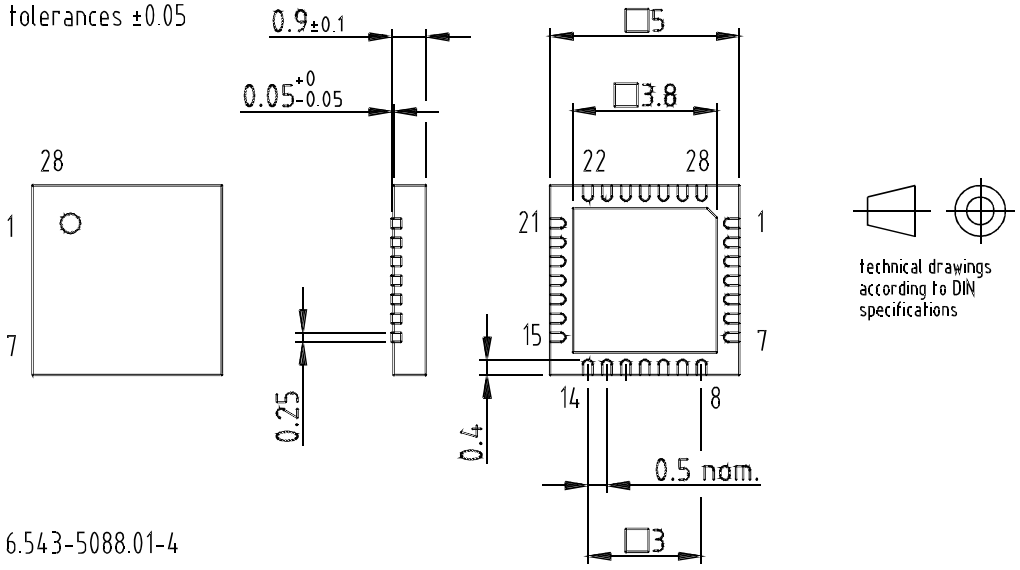
Ordering Information

Extended Type Number	Package	Remarks
ATR0600-PJQ	QFN28 - 5x5	Taped and reeled

Package Information

Package: QFN 28 - 5x5
Exposed pad 3.8x3.8
(acc. JEDEC OUTLINE No. MO-220)
Dimensions in mm

Not indicated tolerances ±0.05



Drawing-No.: 6.543-5088.01-4
Issue: 2; 24.01.03

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