

DATA SHEET

AU2901

Quad voltage comparator

Product data
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2001 Aug 03

Quad voltage comparator

AU2901

DESCRIPTION

The AU2901 consists of four independent precision voltage comparators, with an offset voltage specification as low as 2.0 mV max for each comparator, which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common-mode voltage range includes ground, even though they are operated from a single power supply voltage.

The AU2901 was designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, the AU2901 will directly interface with MOS logic where their low power drain is a distinct advantage over standard comparators.

FEATURES

- Wide single supply voltage range 2.0 V_{DC} to 36 V_{DC} or dual supplies ± 1.0 V_{DC} to ± 18 V_{DC}
- Very low supply current drain (0.8 mA) independent of supply voltage (1.0 mW/comparator at 5.0 V_{DC})
- Low input biasing current 25 nA
- Low input offset current ± 5 nA and offset voltage
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Low output 250 mV at 4 mA saturation voltage
- Output voltage compatible with TTL, DTL, ECL, MOS and CMOS logic systems

APPLICATIONS

- A/D converters
- Wide range VCO
- MOS clock generator
- High voltage logic gate
- Multivibrators

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
14-Pin Plastic Small Outline (SO) Package	-40 °C to +125 °C	AU2901D	SOT108-1
14-Pin Plastic Dual In-Line Package (DIP)	-40 °C to +125 °C	AU2901N	SOT27-1

PIN CONFIGURATION

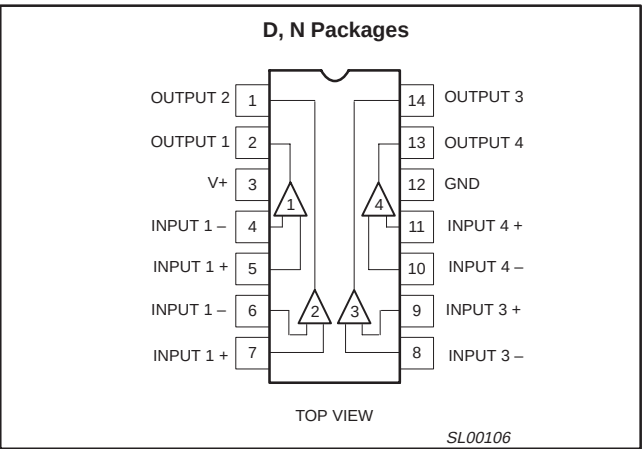


Figure 1. Pin Configuration

EQUIVALENT CIRCUIT

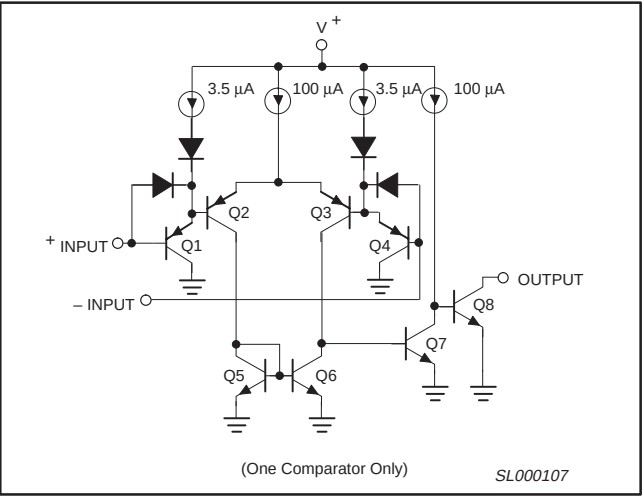


Figure 2. Equivalent Circuit

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ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	V_{CC} supply voltage	36 or ± 18	V_{DC}
V_{DIFF}	Differential input voltage	36	V_{DC}
V_{IN}	Input voltage	-0.3 to $+36$	V_{DC}
P_{DMAX}	Maximum power dissipation, $T_{amb} = 25\text{ }^{\circ}\text{C}$ (still-air) ¹		
	N package	1420	mW
	D package	1040	mW
	Output short-circuit to ground ²	Continuous	
I_{IN}	Input current ($V_{IN} < -0.3 V_{DC}$) ³	50	mA
T_{amb}	Operating temperature range	-40 to $+125$	$^{\circ}\text{C}$
T_{stg}	Storage temperature range	-65 to $+150$	$^{\circ}\text{C}$
T_{sld}	Lead soldering temperature (10 sec max)	230	$^{\circ}\text{C}$

NOTES:

- Derate above $25\text{ }^{\circ}\text{C}$, at the following rates:
N Package at $11.4\text{ mW}/^{\circ}\text{C}$
D Package at $8.3\text{ mW}/^{\circ}\text{C}$
- Short circuits from the output to $V+$ can cause excessive heating and eventual destruction. The maximum output current is approximately 20 mA independent of the magnitude of $V+$.
- This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the $V+$ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will reestablish when the input voltage, which was negative, again returns to a value greater than $-0.3 V_{DC}$.

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ELECTRICAL CHARACTERISTICS

V+ = 5 V_{DC}; -40 °C ≤ T_{amb} ≤ 125 °C, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	Limits			UNIT
			Min	Typ	Max	
V _{OS}	Input offset voltage ²	T _{amb} = 25 °C Over temp.		±2.0 ±2.5	±3 ±5	mV
V _{CM}	Input common-mode voltage range ³	T _{amb} = 25 °C Over temp.	0 0		V+ -1.5 V+ -2.0	V
V _{IDR}	Differential input voltage ¹	Keep all V _{IN} ^S ≥ 0V _{DC} (or V- if need)			V+	V
I _{BIAS}	Input bias current ⁴	I _{IN(+)} or I _{IN(-)} with output in linear range T _{amb} = 25 °C Over temp.		25 200	250 500	nA
I _{OS}	Input offset current	I _{IN(+)} - I _{IN(-)} T _{amb} = 25 °C Over temp.		±5 ±50	±50 ±200	nA nA
I _{OL}	Output sink current	V _{IN(-)} ≥ 1 V _{DC} ; V _{IN(+)} = 0; V _O ≤ 1.5 V _{DC} ; T _{amb} = 25 °C	6.0	16		mA
I _{OH}	Output leakage current	V _{IN(+)} ≥ 1 V _{DC} ; V _{IN(-)} = 0 V _O = 5 V _{DC} ; T _{amb} = 25 °C V _O = 30 V _{DC} ; Over temp.		0.1	1.0	nA μA
I _{CC}	Supply current	R _L = ∞ on comparators, T _{amb} = 25 °C V+ = 30 V		0.8 1.0	2.0 2.5	mA
A _V	Voltage gain	R _L ≥ 15 kΩ; V+ = 15 V _{DC}	25	100		V/mV
V _{OL}	Saturation voltage	V _{IN(-)} ≥ 1 V _{DC} ; V _{IN(+)} = 0; I _{SINK} ≤ 4 mA T _{amb} = 25 °C Over temp.		400	400 700	mV
t _{LSR}	Large-signal response time	V _{IN} = TTL logic swing; V _{REF} = 1.4V _{DC} ; V _{RL} = 5V _{DC} ; R _L = 5.1 kΩ; T _{amb} = 25 °C		300		ns
t _R	Response time ⁵	V _{RL} = 5 V _{DC} ; R _L = 5.1 kΩ; T _{amb} = 25 °C		1.3		μs

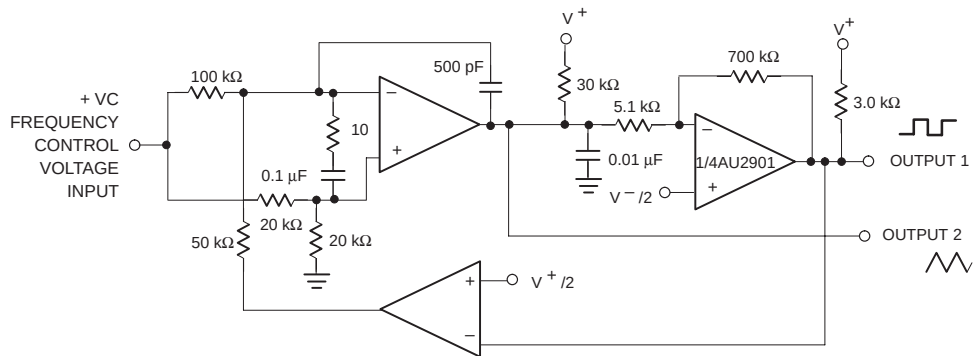
NOTES:

- Positive excursions of input voltage may exceed the power supply level by 17 V. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than -0.3 V_{DC} (or 0.3 V_{DC} below the magnitude of the negative power supply, if used).
- At output switch point, V_O ≈ 1.4 V_{DC}, R_S = 0 Ω with V+ from 5 V_{DC} to 30 V_{DC}; and over the full input common-mode range (0 V_{DC} to V+ - 1.5 V_{DC}).
- The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3 V. The upper end of the common-mode voltage range is V+ - 1.5 V, but either or both inputs can go to 30 V_{DC} without damage.
- The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.
- The response time specified is for a 100 mV input step with a 5 mV overdrive. For larger overdrive signals, 300 ns can be obtained (see Typical Performance Characteristics section).

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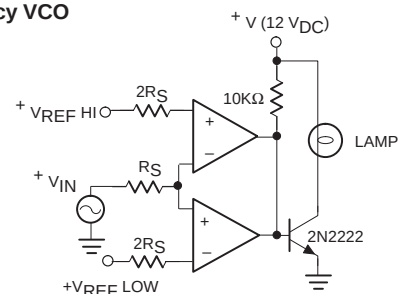
EQUIVALENT CIRCUIT



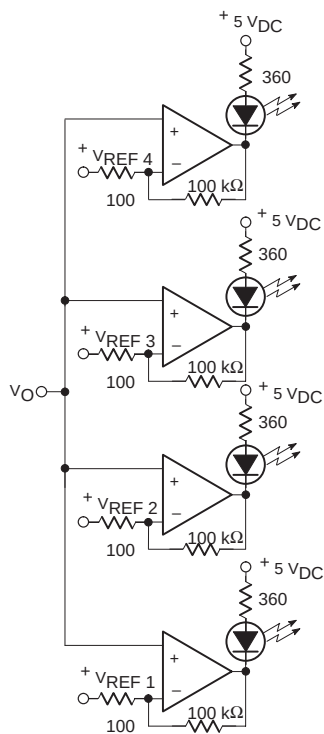
NOTES:

$$V_+ = 30 \text{ V}_{\text{DC}}$$
$$+ 250 \text{ mV}_{\text{DC}} \leq V_C \leq 50 \text{ V}_{\text{DC}}$$
$$700 \text{ Hz} \leq f_O = 100 \text{ kHz}$$

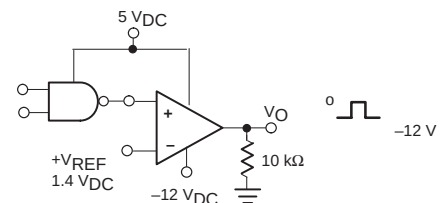
Two-Decade High-Frequency VCO



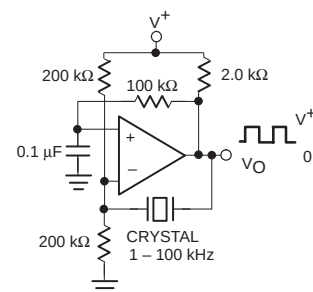
Limit Comparator



Visible Voltage Indicator



TTL-to-MOS Logic Converter



Crystal-Controlled Oscillator

NOTE:

NOTE:
Input of unused comparators should be grounded.

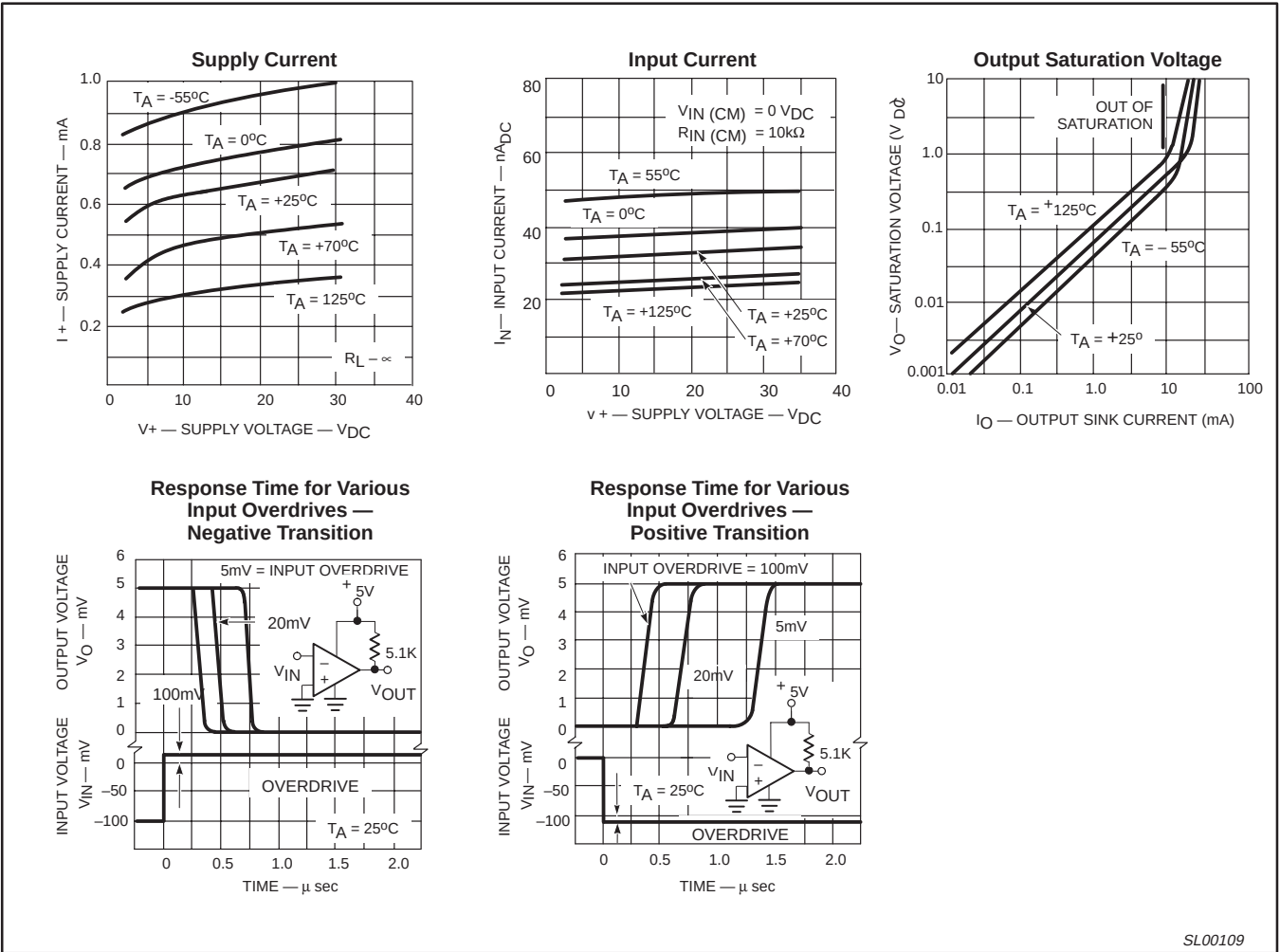
SL00108

Figure 3. Equivalent Circuit

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TYPICAL PERFORMANCE CHARACTERISTICS



SL00109

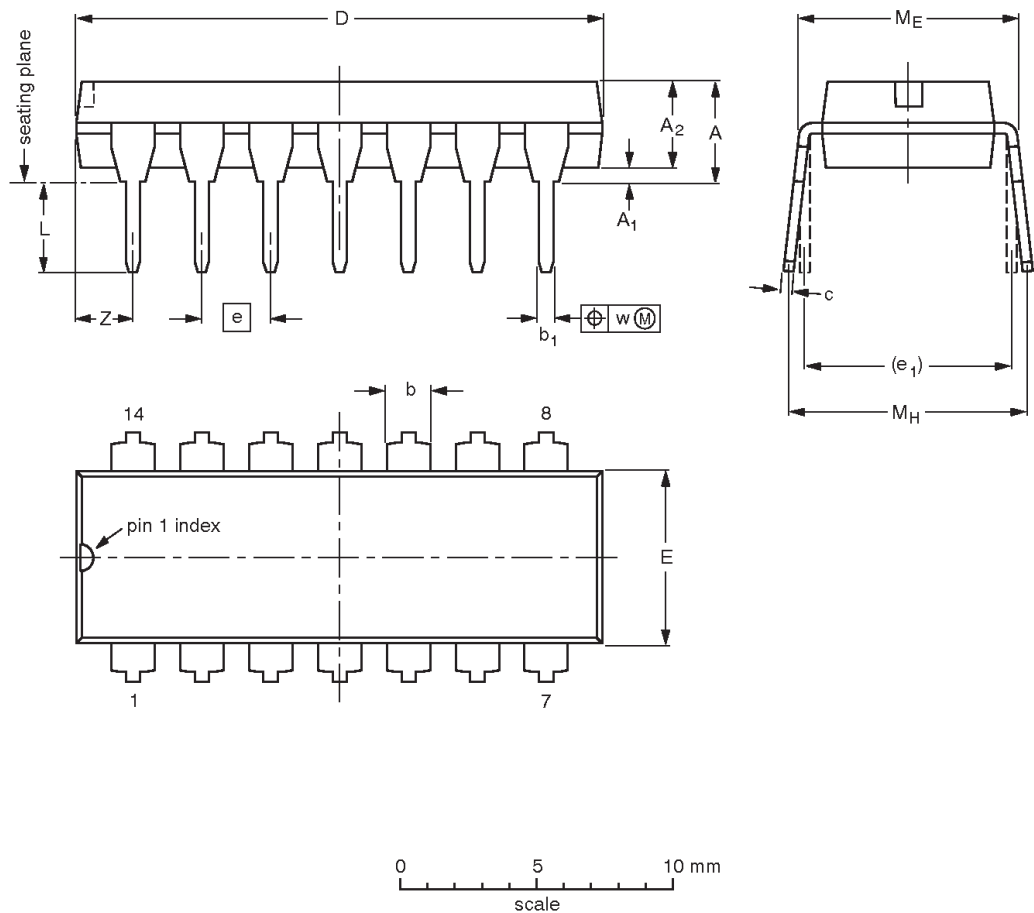
Figure 4. Typical Performance Characteristics

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DIP14: plastic dual in-line package; 14 leads (300 mil)

SOT27-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	c	D ⁽¹⁾	E ⁽¹⁾	e	e ₁	L	M _E	M _H	w	Z ⁽¹⁾ max.
mm	4.2	0.51	3.2	1.73 1.13	0.53 0.38	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.2
inches	0.17	0.020	0.13	0.068 0.044	0.021 0.015	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

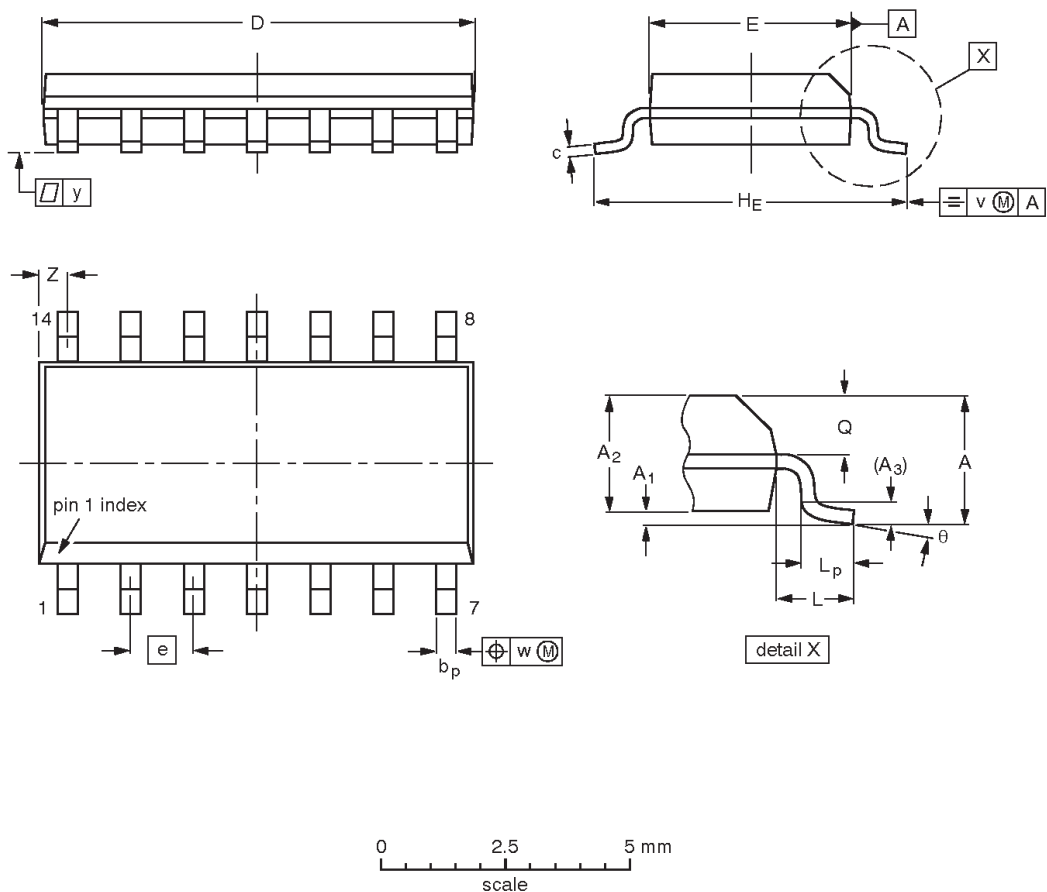
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT27-1	050G04	MO-001	SC-501-14			95-03-11 99-12-27

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SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT108-1	076E06	MS-012				97-05-22 99-12-27

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NOTES

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