AU9321
USB Compact Flash Card Reader
Technical Reference Manual

Revision 1.1

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1.0 Introduction

1.1 Description

The AU9321 is a single chip integrated USB Compact Flash (CF) card reader controller. It can be used as a removable storage disk in enormous data exchange applications between PC and PC or PC and various consumer electronic devices.

The AU9321 can read of CF card's contents created by handheld consumer electronic devices such as digital camera, MP3 player, PDA and mobile phone… etc. It provides a faster and convenient way of data transfer scheme to meet the emerging need of a data exchange center between PC and various consumer devices. With AU9320, users' experience will be further enhanced by the Plug-and-Play nature built into latest operation systems such as Windows 2000/XP and Mac OS X.

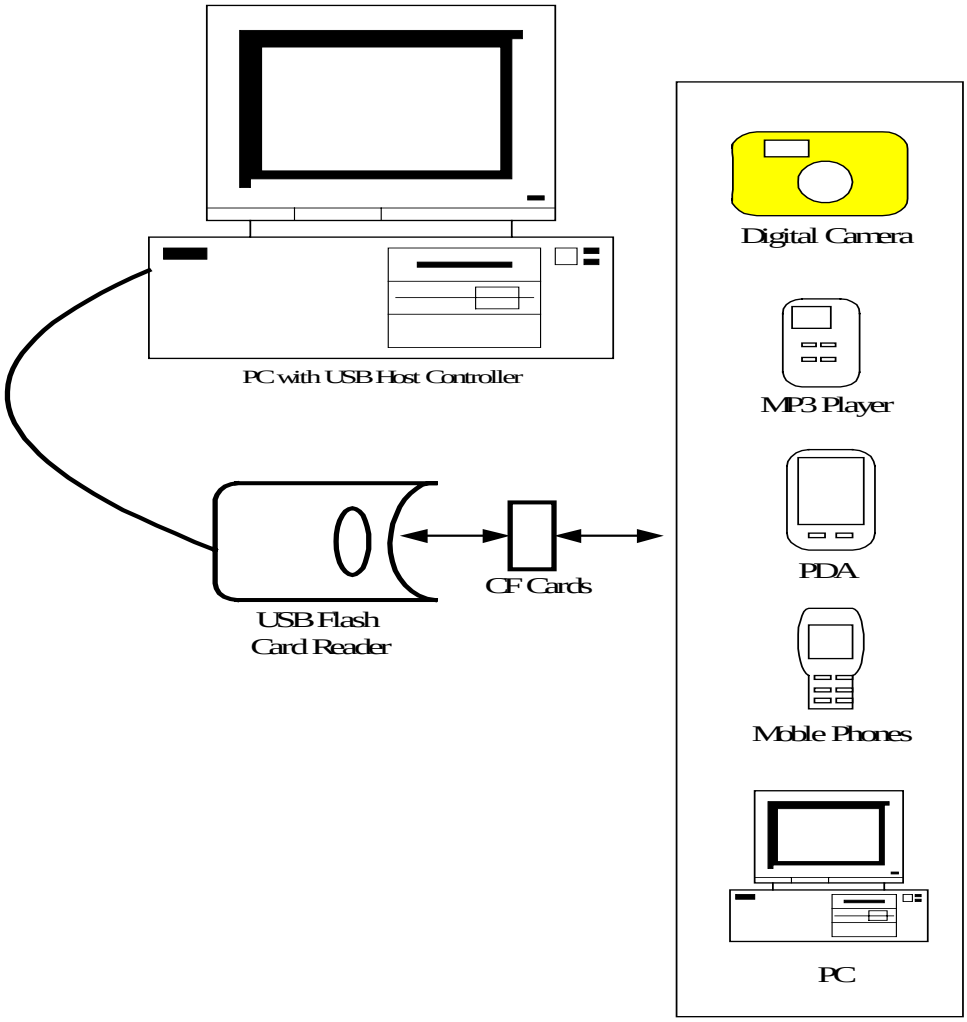
Because of the multiple sectors transfer up to 4G bytes and the single chip integration, AU9321 will be the most powerful and cost efficient CF card reader controller solution in the market.

1.2 Features

- Fully compliant with USB v1.1 specification and USB Device Class Definition for Mass Storage, Bulk-Transport v1.0
- Fully compliant with Compact Flash (CF) v1.4 Specification.
- Work with default driver from Windows ME, Windows 2000, Windows XP, Mac OS 9.1, and Mac OS X. Windows 98 is supported by vendor driver from Alcor.
- Ping-pong FIFO implementation for concurrent bus operation
- Support multiple sectors transfer up to 4G byte to optimize performance
- Support optional external EEPROM for USB VID, PID and string customization
- Capable of handling 8 sets of built-in PID, VID and strings to minimize inventory control and improve lead production lead time
- LED for bus activity monitoring
- Integrated power switch and power management circuit to meet USB 500uA power consumption during suspend with CF card in the slot.
- Runs at 12MHz, built-in 48 MHz PLL
- Built-in 3.3V regulator
- 48-pin LQFP package

2.0 Application Block Diagram

Following is the application diagram of a typical flash memory card reader using AU9321. By connecting the reader to a PC through USB bus, the AU9321 is acting as a bridge between the flash memory card from digital camera, MP3 player, PDA or mobile phone and PC.



3.0 Pin Assignment

The AU9321 is packed in 48-LQFP form factor. The following figure shows signal name for each pin and the table in the following page describes each pin in detail.

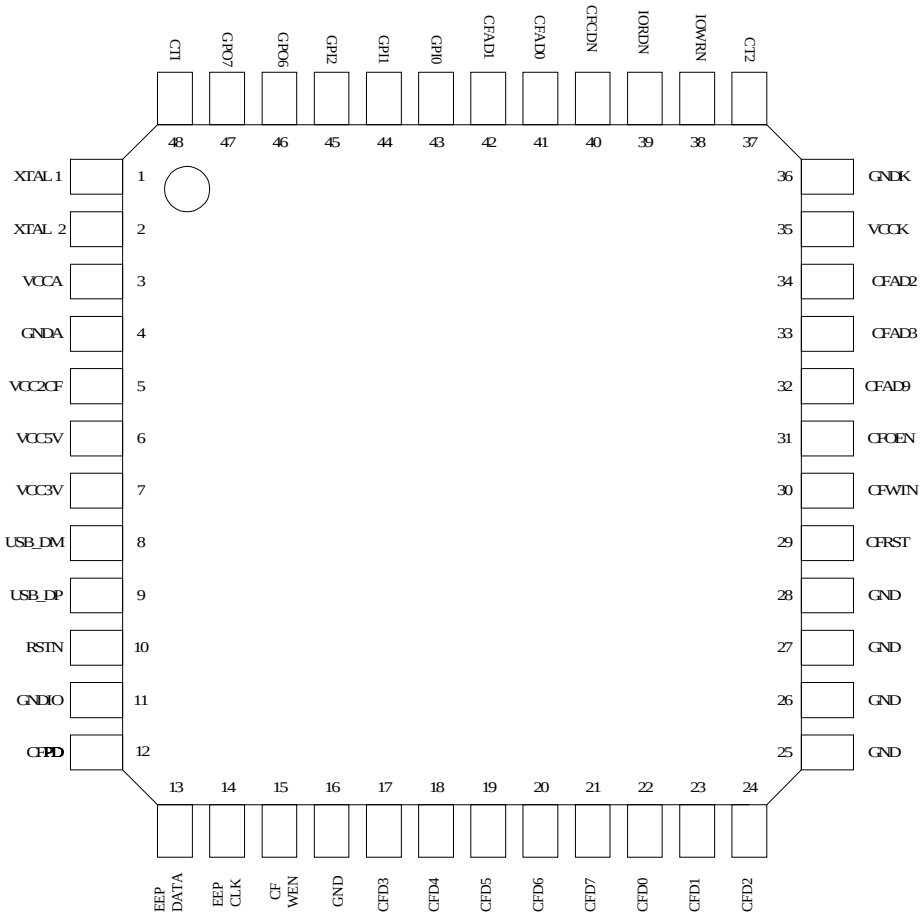


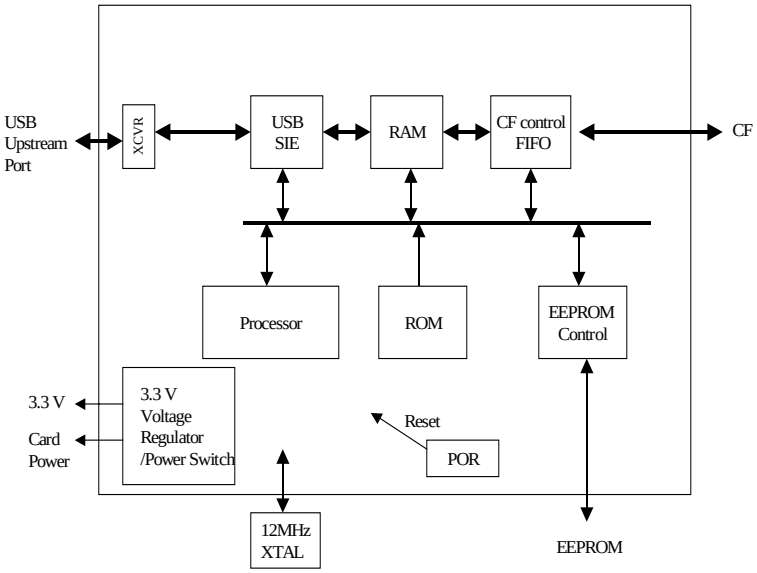
Table 3-1. Pin Descriptions

Pin	Name	IO Type	Description
1	XTAL1	Input	Crystal Oscillator Input (12MHz)
2	XTAL2	Output	Crystal Oscillator Output (12MHz)
3	VCCA	Power	Analog Vcc, Connected to 3.3V
4	GNDA	Ground	Connected to Ground
5	VCC2CF	Power	CF Power
6	VCC5V	Power	5V Power Supply
7	VCC3V	Output	Regulated 3.3V out
8	USB_DM	Input/Output	USB D-
9	USB_DP	Input/Output	USB D+
10	RSTN	Input	Hardware reset (Active Low)
11	GNDIO	Ground	Ground
12	CFPD	Power	Power Down
13	EEPDATA	Input/Output	EEPROM Data
14	EEPCLK	Output	EEPROM Clock
15	CFWEN	Output	Arribute write enable
16	GND	Ground	Ground
17	CFD3	Input/Output	Compact Flash Data 3
18	CFD4	Input/Output	Compact Flash Data 4
19	CFD5	Input/Output	Compact Flash Data 5
20	CFD6	Input/Output	Compact Flash Data 6
21	CFD7	Input/Output	Compact Flash Data 7
22	CFD0	Input/Output	Compact Flash data 0
23	CFD1	Input/Output	Compact Flash data 1
24	CFD2	Input/Output	Compact Flash data 2
25	GND	Ground	Ground
26	GND	Ground	Ground
27	GND	Ground	Ground
28	GND	Ground	Ground
29	CFRST	Output	Compact Flash reset signal
30	CFWTN	Input	Compact Flash wait signal
31	CFOEN	Output	Compact Flash output enable
32	CFAD9	Output	Compact Flash address 9
33	CFAD3	Output	Compact Flash address 3
34	CFAD2	Output	Compact Flash address 2
35	VCCK	Power	Kernel Vcc
36	GNDK	Ground	Kernel Ground
37	CT2		Connected to Ground
38	IOWRN	Output	Compact Flash I/O write signal
39	IORDN	Output	Compact Flash I/O read signal
40	CFCDN	Input	Compact Flash Card Detect
41	CFAD0	Output	Compact Flash address 0
42	CFAD1	Output	Compact Flash address 1
43	GPI0	Input	General Purpose I (*1)
44	GPI1	Input	General Purpose I (*1)
45	GPI2	Input	General Purpose I
46	GPO6	Output	General Purpose Output
47	GPO7	Output	General Purpose Output, used for LED activity
48	CT1		Connected to Ground

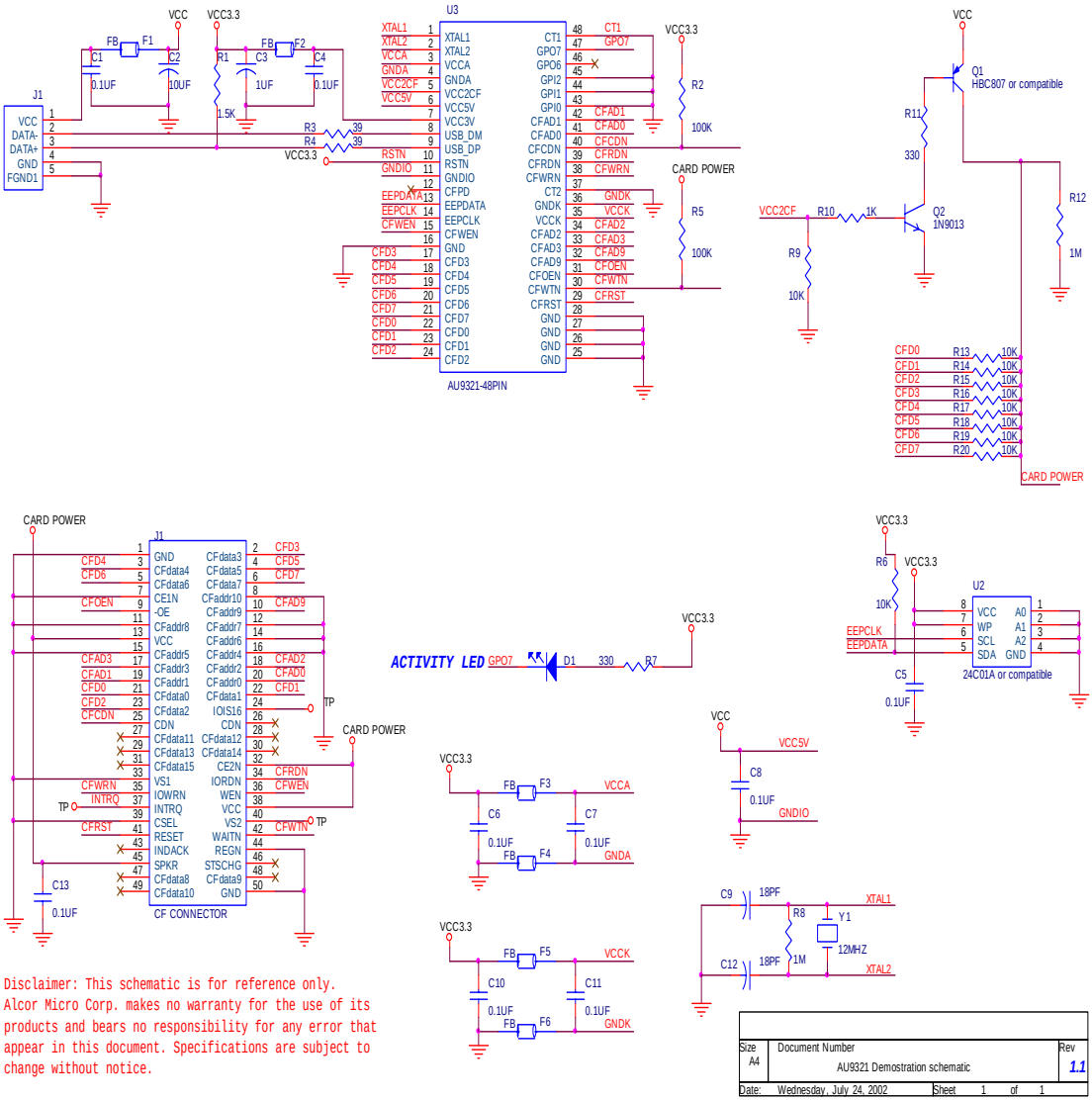
4.0 System Architecture and Reference Design

4.1 AU9321 Block Diagram

Alcor Micro - AU9321 Flash Memory Card Reader Block Diagram



4.2 Sample Schematics



Disclaimer: This schematic is for reference only. Alcor Micro Corp. makes no warranty for the use of its products and bears no responsibility for any error that appear in this document. Specifications are subject to change without notice.

5.0 Electrical Characteristics

5.0 Recommended Operating Conditions

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
V_{CC}	Power Supply	4.75	5	5.25	V
V_{IN}	Input Voltage	0		V_{CC}	V
T_{OPR}	Operating Temperature	0		85	^{O}C
T_{STG}	Storage Temperature	-40		125	^{O}C

5.1 General DC Characteristics

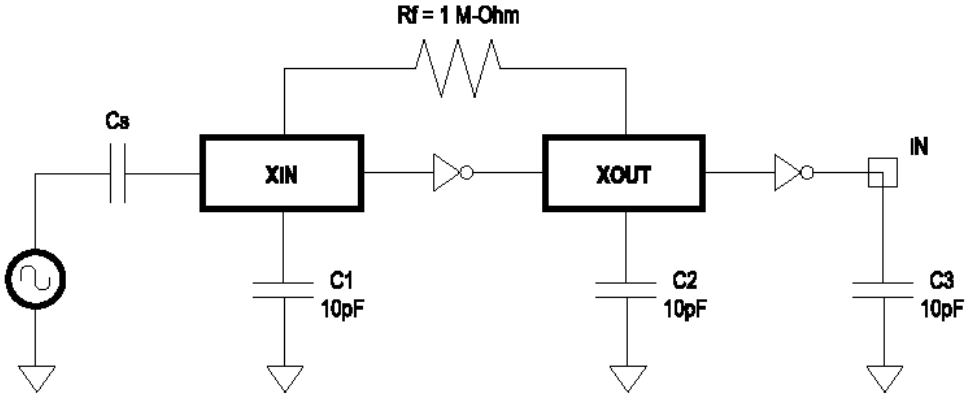
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{IL}	Input low current	no pull-up or pull-down	-1		1	µA
I_{IH}	Input high current	no pull-up or pull-down	-1		1	µA
I_{OZ}	Tri-state leakage current		-10		10	µA
C_{IN}	Input capacitance			5		ρF
C_{OUT}	Output capacitance			5		ρF
C_{BID}	Bi-directional buffer capacitance			5		ρF

5.2 DC Electrical Characteristics for 3.3 volts operation

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{IL}	Input Low Voltage	CMOS			0.9	V
V_{IH}	Input Hight Voltage	CMOS	2.3			V
V_{OL}	Output low voltage	I_{OL}=4mA, 16mA			0.4	V
V_{OH}	Output high voltage	I_{OH}=4mA,16mA	2.4			V
R_I	Input Pull-up/down resistance	Vil=0_V or Vih=V_{CC}		10k/200k		KΩ

5.4 Crystal Oscillator Circuit Setup for Characteristics

The following setup was used to measure the open loop voltage gain for crystal oscillator circuits. The feedback resistor serves to bias the circuit at its quiescent operating point and the AC coupling capacitor, Cs, is much larger than C1 and C2.



5.5 ESD Test Results

Test Description : ESD Testing was performed on a Zapmaster system using the Human-Body –Model (HBM) and Machine-Model (MM), according to MIL_STD 883 and EIAJ IC_121 respectively.

- Human-Body-Model stress devices by sudden application of a high voltage supplied by a 100 PF capacitor through 1.5 Kohm resistance.
- Machine-Model stresses devices by sudden application of a high voltage supplied by a 200 PF capacitor through very low (0 ohm) resistance

Test circuit & condition

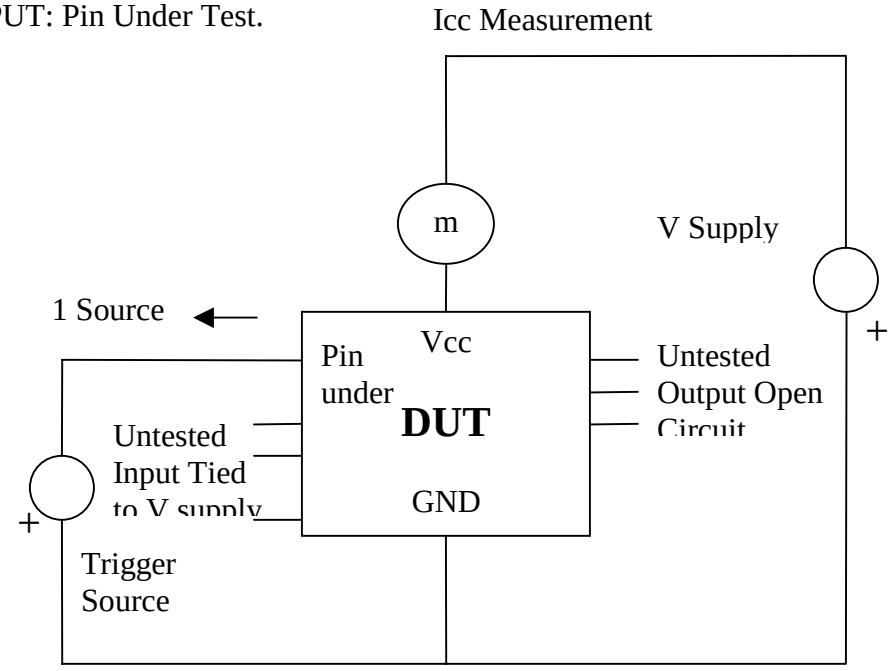
- Zap Interval : 1 second
- Number of Zaps : 3 positive and 3 negative at room temperature
- Critera : I-V Curve Tracing

Model	**Model**	**S/S**	**TARGET**	**Results**
HBM	Vdd, Vss, I/C	15	4000V	Pass
MM	Vdd, Vss, I/C	15	200V	Pass

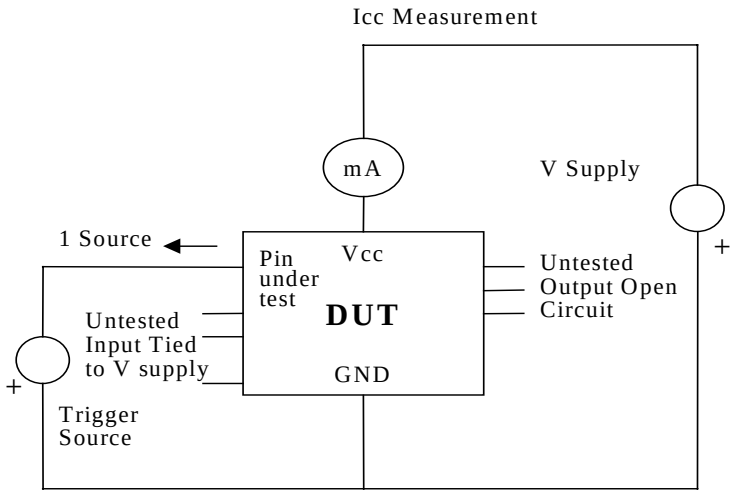
5.6 Latch-Up Test Results

Test Description: Latch-Up testing was performed at room ambient using an IMCS-4600 system which applies a stepped voltage to one pin per device with all other pins open except Vdd and Vss which were biased to 5 Volts and ground respectively.
Testing was started at 5.0 V (Positive) or 0 V(Negative), and the DUT was biased for 0.5 seconds.
If neither the PUT current supply nor the device current supply reached the predefined limit (DUT=0 mA , Icc=100 mA), then the voltage was increased by 0.1 Volts and the pin was tested again.
This procedure was recommended by the JEDEC JC-40.2 CMOS Logic standardization committee.

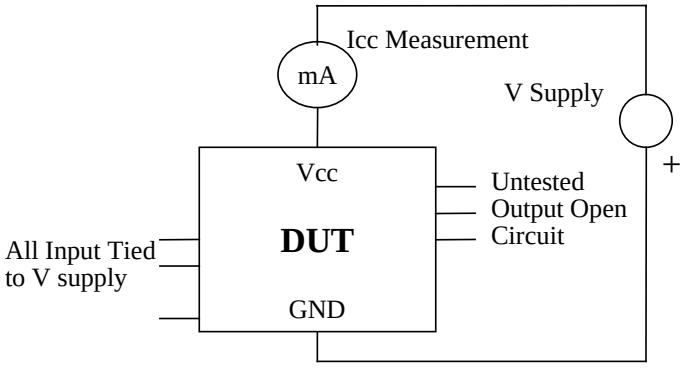
Notes:
1. DUT: Device Under Test.
2. PUT: Pin Under Test.



Test Circuit : Positive Input/ output Overvoltage /Overcurrent



Test Circuit : Negative Input/ Output Overvoltage /Overcurrent

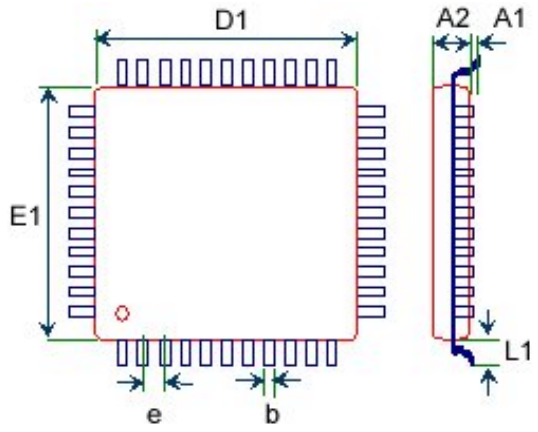


Supply Voltage test

Latch–Up Data

Model	Model	Voltage (v)/ Current (mA)	S/S	Results
Voltage	+	11.0	5	Pass
	-	11.0		
Current	+	200	5	
	-	200		
Vdd-Vxx		9.0	5	Pass

6.0 Mechanical Information



body size		lead count	A1	A2	L1	b	c	e
D1	E1							
7	7	48	0.1	1.4	1	0.2	0.127	0.5

A1	stand-off
A2	body thickness
L1	lead length
b	lead width
c	lead thickness
e	lead pitch