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Data Book

AU9384

USB Flash Disk Controller

Technical Reference Manual

Product Specification

Official Release

Revision 1.01

Public

Jul 2004



Data sheet status

Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.

Revision History

Date	Revision	Description
Mar 2004	1.00	Initial release
Jul 2004	1.01	To modify 1.2 feature



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1.0 Introduction

1.1 Description

AU9384 is a highly integrated single chip USB flash disk controller. It provides the most cost efficient bridge between USB enabled PC and NAND type flash memory. Not only it can be used as a removable storage disk in Windows PC, Apple Macintosh, Notebook and Linux/Unix workstation, it also can be configured as bootable disk for system reparation.

AU9384 gives USB storage device a new life. It will automatically execute your program & play content including Video MPEG, Audio MP3, Advertisements and Applications. AU9384 is an outstanding USB storage device controller, it enables auto run features in Windows 98, XP, 2000 and ME. These unique features give hardware device maker and software vendor tremendous opportunity to develop user-friendly appliance and application.

AU9384 works with 1 to 8 NAND type flash memory chip with the combination of popular flash memory types such as 8M, 16M, 32M, 64M, 128M and 256M. Additional features include write protection switch, activity LED and password protected security.

1.2 Features

- Support USB v1.1 specification and USB Device Class Definition for Mass Storage, Bulk-Transport v1.0
- Work with default driver from Windows ME, Windows 2000, Windows XP, and Mac 9.2, Mac OS X. Windows 98SE is supported by vendor driver from Alcor.
- Support AutoRun feature
 - ◆ The vendor image designed (such as logo, disk icon and label) can be pre-installed to UFD and display automatically right after device plug in.
- AutoRun feature can be supported on Windows ME, Windows 2000, Windows XP and Windows 98.
- Provide vendor with hidden flash area where user cannot access.
- No extra CD needed for application program, all security and partition program can be pre-installed in hidden area and automatically running after device plug in. Enable vendor develops proactive killer application with incredible "No installation", "Without one click" & "Plug-N-Play" features.
- Security function supported with password protection
- Multiple FIFO implementation for concurrent bus operation
- 64-pin package supports to 8 pieces NAND Flash memory chip; total capacity reaches to 2G byte when working with 1G bit mono dies chip.
- 48-pin package supports to 4 pieces NAND Flash memory chip; total capacity reaches to 1G byte.
- Support mixed different size NAND Flash
- Vendor ID, product ID and strings can be customized by utility software from Alcor
- Can be configured to support dual partitions with dynamic logic disk space allocation.



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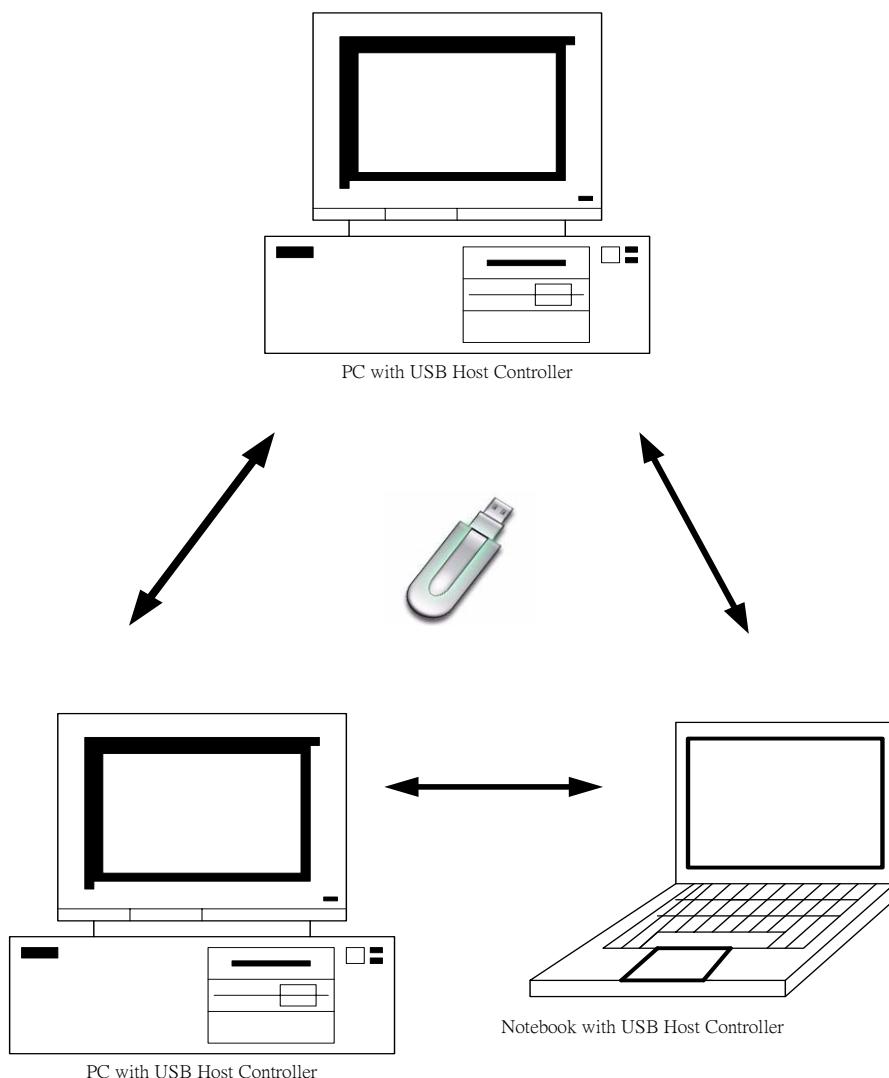
- LED for bus activity monitoring
- Runs at 12MHz, built-in 48 MHz PLL
- Built-in 3.3V regulator
- Built-in power switch and power management circuit to achieve 500uA suspend current required by USB specification.
- Built-in power on reset circuit
- Dedicated DMA engine to ensure highest throughput in read and write
- 48-pin LQFP package as standard package and 64-pin LQFP package for choice.



2.0 Application Block Diagram

Following is the application diagram of a typical flash disk product with AU9384. By connecting the flash disk to a desktop or notebook PC through USB bus, AU9384 is implemented as a bus-powered, full speed USB disk, which can be used as a bridge for data transfer between Desktop PC and Notebook PC.

Figure 2.1 Au9384 Application Block Diagram

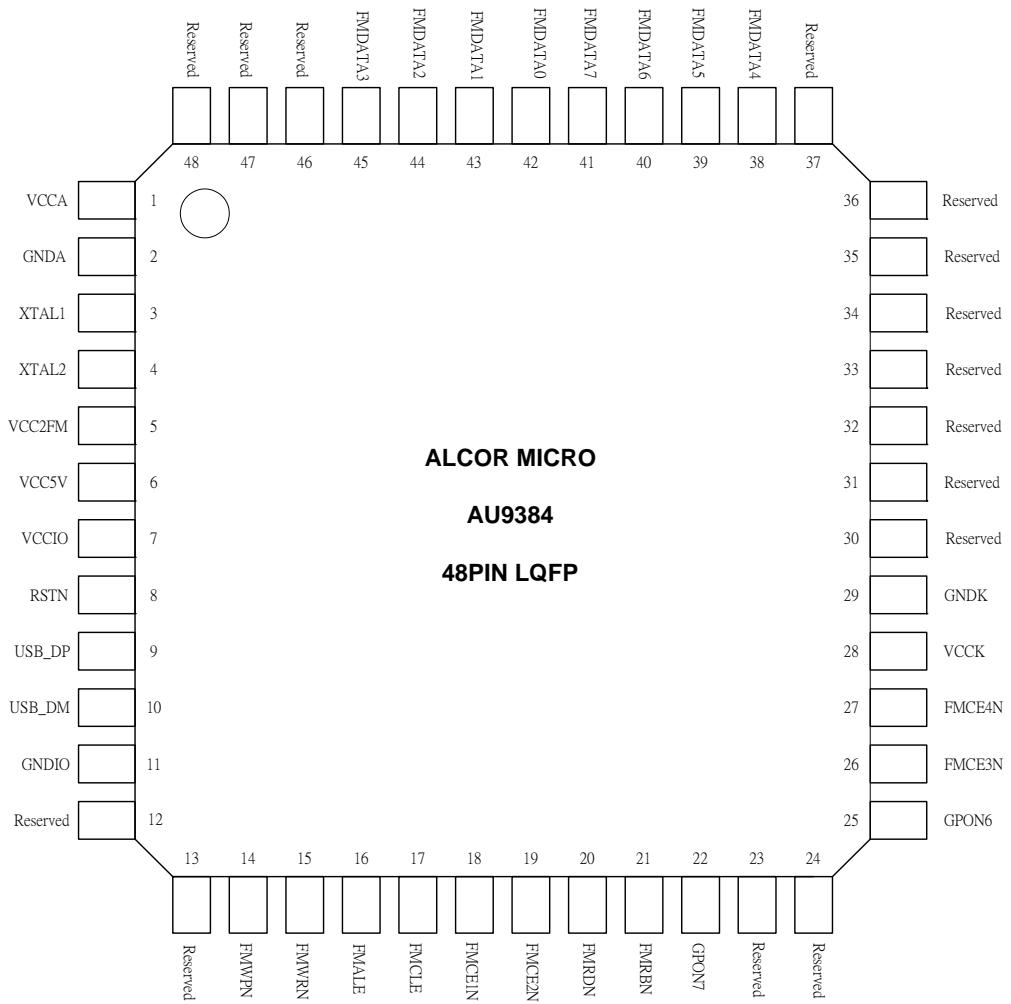




3.0 Pin Assignment

The AU9384 is packed in 48-pin LQFP form factor. The figure on the following page shows the signal names for each of the pins on the chip. Accompanying the figure is the table that describes each of the pin signals.

Figure 3.1 Pin Assignment Diagram



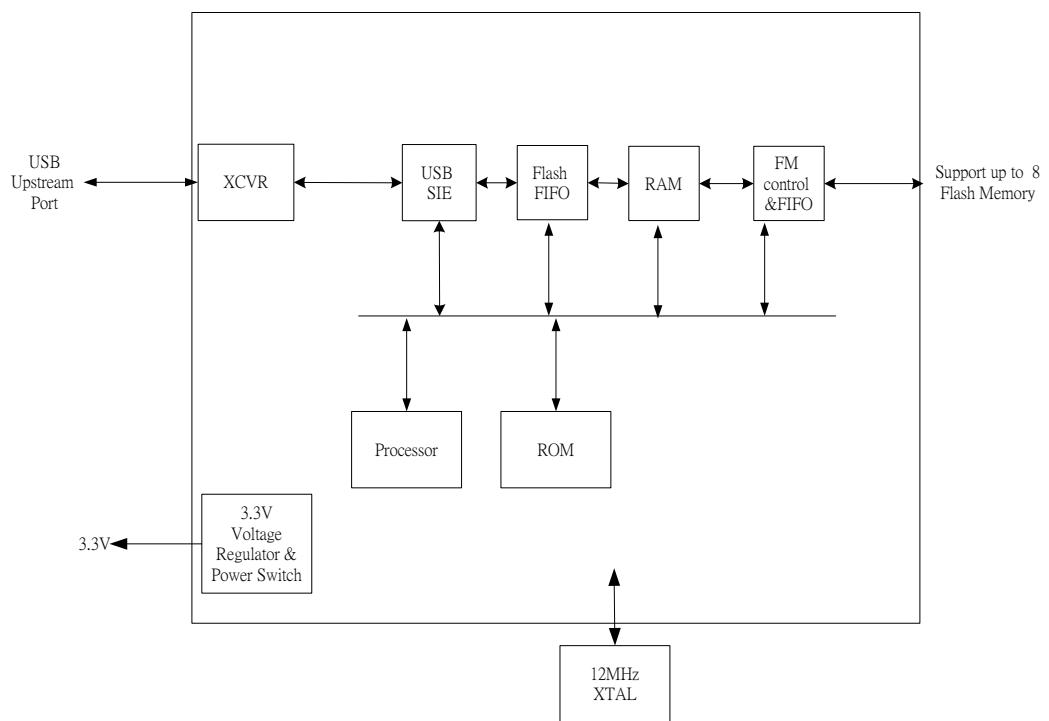
**Table 3.1 Pin Descriptions**

Pin	Pin Name	I/O Type	Description
1	VCCA	PWR	3.3V input for PLL
2	GNDA	PWR	Ground
3	XTAL1	I	Crystal Oscillator Input (12MHz)
4	XTAL2	O	Crystal Oscillator Output (12MHz)
5	VCC2FM	O	Connect to Flash Memory VCC
6	VCC5V	PWR	5V power supply
7	VCCIO	PWR	Regulator 3.3V output/ IO 3.3V input
8	RSTN	I	Hardware reset (Active Low)
9	USB_DP	I/O	USB D+
10	USB_DM	I/O	USB D-
11	GNDIO	PWR	Ground
12	Reserved		Reserved
13	Reserved		Reserved
14	FMWPN	I	Connect to Flash Memory Write Protect
15	FMWRN	O	Connect to Flash Memory Write Enable
16	FMALE	O	Connect to Flash Memory Address Latch Enable
17	FMCLE	O	Connect to Flash Memory Command Latch Enable
18	FMCE1N	O	Connect to Flash Memory Chip1 Enable
19	FMCE2N	O	Connect to Flash Memory Chip2 Enable
20	FMRDN	O	Connect to Flash Memory Read Enable
21	FMRBN	I	Connect to Flash Memory Ready/Busy Output
22	GPON7	O	General Purpose Output pin, used as activity LED
23	Reserved		Reserved
24	Reserved		
25	GPON6	O	Floating
26	FMCE3N	O	Connect to Flash Memory Chip3 Enable
27	FMCE4N	O	Connect to Flash Memory Chip4 Enable
28	VCCK	PWR	Core 3.3V Input
29	GNDK	PWR	Ground
30	Reserved		Connect to VCC
31	Reserved		Connect to ground
32	Reserved		Connect to ground
33	Reserved		Connect to ground
34	Reserved		Connect to ground
35	Reserved		Connect to ground
36	Reserved		
37	Reserved		Reserved
38	FMDATA4	I/O	Connect to Flash Memory Data IO4
39	FMDATA5	I/O	Connect to Flash Memory Data IO5
40	FMDATA6	I/O	Connect to Flash Memory Data IO6
41	FMDATA7	I/O	Connect to Flash Memory Data IO7
42	FMDATA0	I/O	Connect to Flash Memory Data IO0
43	FMDATA1	I/O	Connect to Flash Memory Data IO1
44	FMDATA2	I/O	Connect to Flash Memory Data IO2
45	FMDATA3	I/O	Connect to Flash Memory Data IO3
46	Reserved		Reserved
47	Reserved		Reserved
48	Reserved		Reserved

4.0 System Architecture and Reference Design

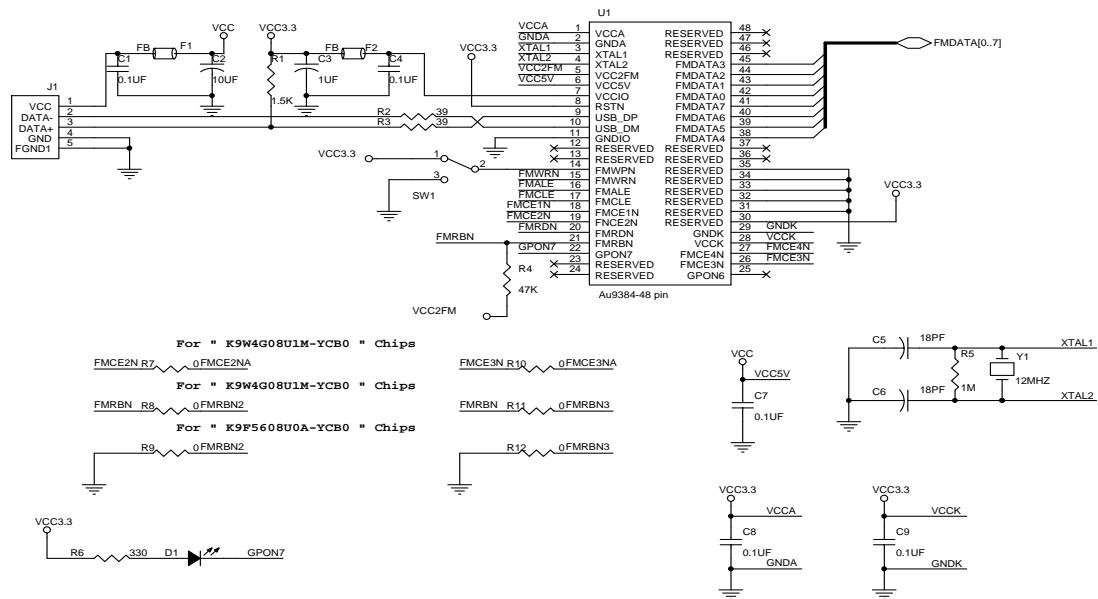
4.1 AU9384 Block Diagram

Figure 4.1 AU9384 Block Diagram



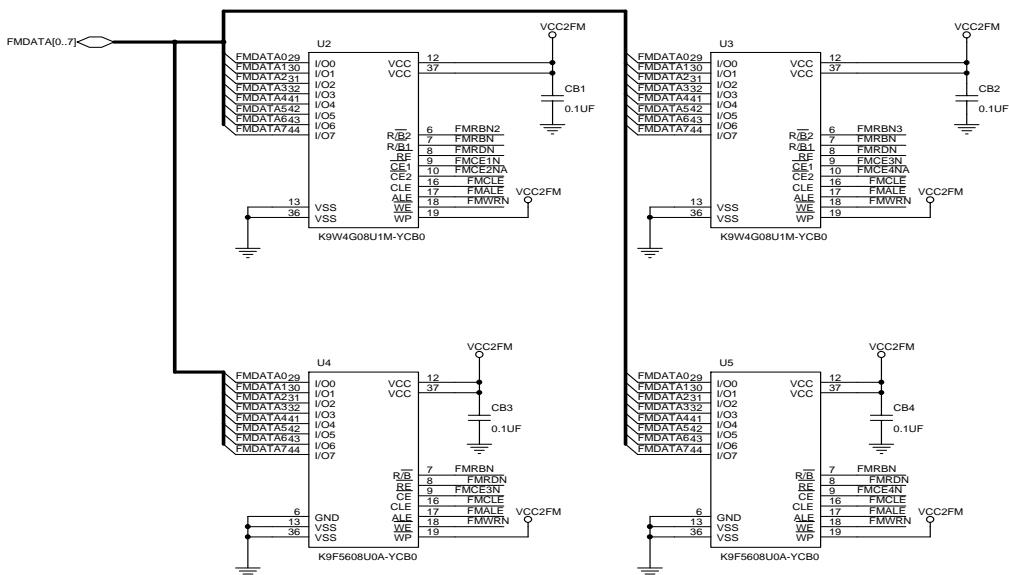


4.2 Sample Schematics



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Size	Document Number	Rev
A	AU9384 flash memory demonstration schematic	1.01



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Size A	Document Number	Au9384 flash memory demonstration schematic	Rev 1.01
Date: Monday, September 22, 2003	Sheet 2 of 2		



5.0 Electrical Characteristics

5.1 Recommended Operating Conditions

Table 5.1 Recommended Operating Conditions

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
V_{CC}	Power Supply	4.75	5	5.25	V
V_{IN}	Input Voltage	0		V_{CC}	V
T_{OPR}	Operating Temperature	0		85	°C
T_{STG}	Storage Temperature	-40		125	°C

5.2 General DC Characteristics

Table 5.2 General DC Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{IL}	Input low current	no pull-up or pull-down	-1		1	µA
I_{IH}	Input high current	no pull-up or pull-down	-1		1	µA
I_{OZ}	Tri-state leakage current		-10		10	µA
C_{IN}	Input capacitance			5		pf
C_{OUT}	Output capacitance			5		pf
C_{BID}	Bi-directional buffer capacitance			5		pf

5.3 DC Electrical Characteristics for 3.3 volts operation

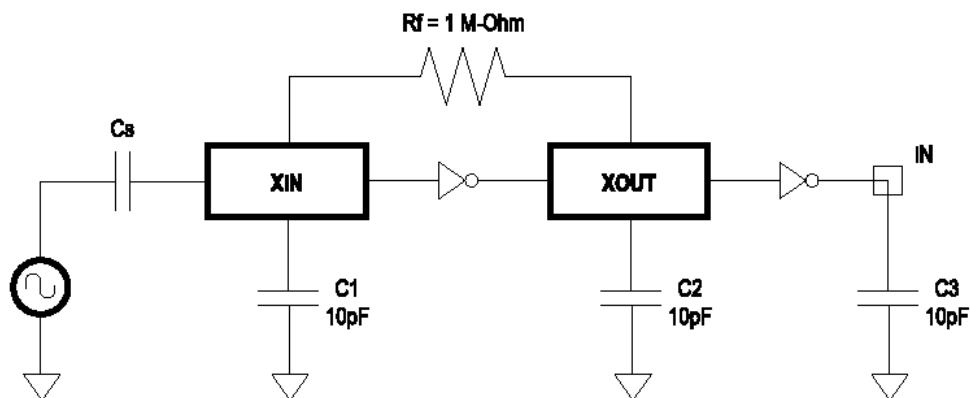
Table 5.3 DC Electrical Characteristics for 3.3 volts operation

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{IL}	Input Low Voltage	CMOS			0.9	V
V_{IH}	Input Hight Voltage	CMOS	2.3			V
V_{OL}	Output low voltage	$I_{OL}=4mA, 16mA$			0.4	V
V_{OH}	Output high voltage	$I_{OH}=4mA, 16mA$	2.4			V
R_I	Input Pull-up/down resistance	$V_{il}=0V$ or $V_{ih}=V_{CC}$		10k/200k		KΩ

5.4 Crystal Oscillator Circuit Setup for Characterization

The following setup was used to measure the open loop voltage gain for crystal oscillator circuits. The feedback resistor serves to bias the circuit at its quiescent operating point and the AC coupling capacitor, C_s , is much larger than C_1 and C_2 .

Figure 5.1 Crystal Oscillator Circuit Setup for Characterization



5.5 ESD Test Results

Test Description: ESD Testing was performed on a Zapmaster system using the Human-Body –Model (HBM) and Machine-Model (MM), according to MIL_STD 883 and EIAJ IC_121 respectively.

- Human-Body-Model stress devices by sudden application of a high voltage supplied by a 100 PF capacitor through 1.5 Kohm resistance.
- Machine-Model stresses devices by sudden application of a high voltage supplied by a 200 PF capacitor through very low (0 ohm) resistance

Test circuit & condition

- Zap Interval: 1 second
- Number of Zaps: 3 positive and 3 negative at room temperature
- Criteria: I-V Curve Tracing

Table 5.4 ESD Data

Model	Model	S/S	TARGET	Results
HBM	Vdd, Vss, I/C	15	4000V	Pass
MM	Vdd, Vss, I/C	15	200V	Pass



5.6 Latch-Up Test Results

Test Description: Latch-Up testing was performed at room ambient using an IMCS-4600 system which applies a stepped voltage to one pin per device with all other pins open except Vdd and Vss which were biased to 5 Volts and ground respectively.

Testing was started at 5.0 V (Positive) or 0 V(Negative), and the DUT was biased for 0.5 seconds.

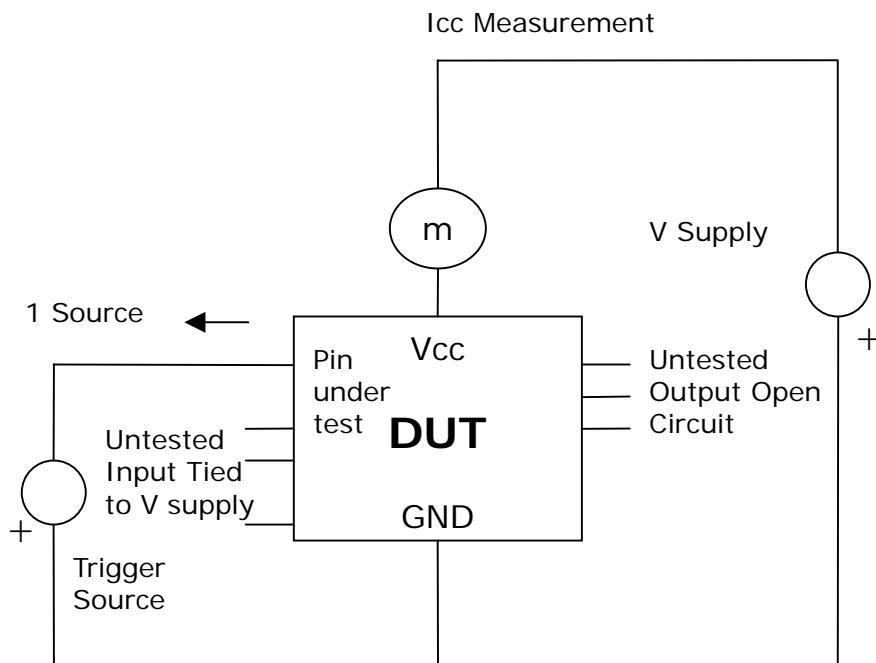
If neither the PUT current supply nor the device current supply reached the predefined limit (DUT=0 mA , Icc=100 mA), then the voltage was increased by 0.1 Volts and the pin was tested again.

This procedure was recommended by the JEDEC JC-40.2 CMOS Logic standardization committee.

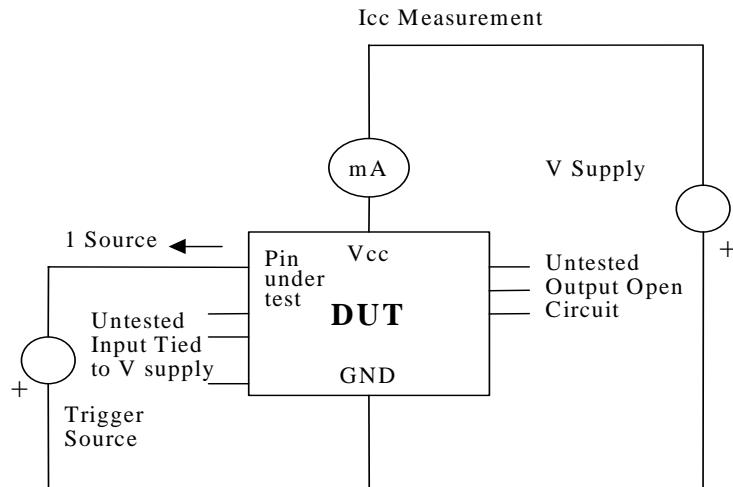
Notes:

1. DUT: Device Under Test.
2. PUT: Pin Under Test.

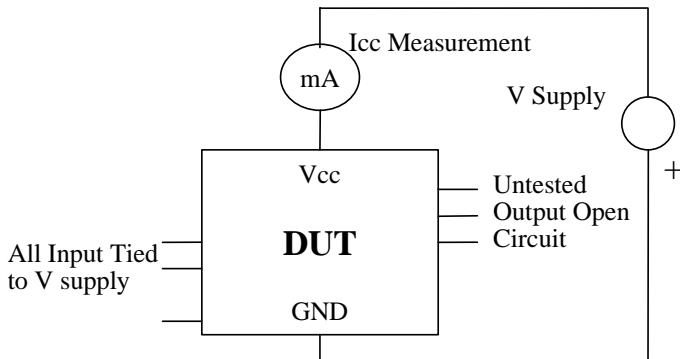
Figure 5.2 Latch-Up Test Results



Test Circuit: Positive Input/ output Overvoltage /Overcurrent



Test Circuit: Negative Input/Output Overvoltage/ Overcurrent



Supply voltage Test

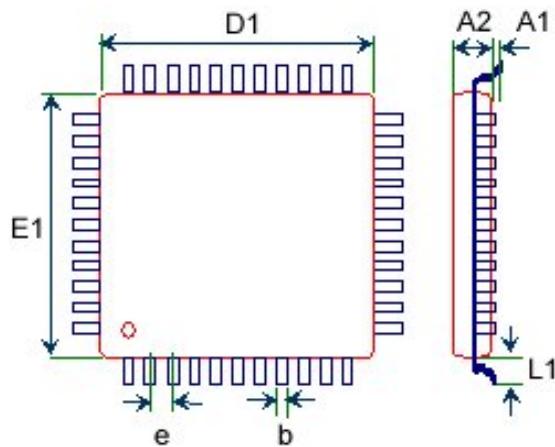
Table 5.5 Latch-Up Data

Model	Model	Voltage (v)/ Current (mA)	S/S	Results
Voltage	+	11.0	5	Pass
	-	11.0		
Current	+	200	5	
	-	200		
Vdd-Vxx		9.0	5	Pass

6.0 Mechanical Information

Following diagrams show the dimensions of the AU9384 48-pin LQFP and 64-pin LQFP. Measurements are in inches.

Figure 6.1 Mechanical Information Diagram



body size		lead count	A1	A2	L1	b	c	e
D1	E1							
7	7	48	0.1	1.4	1	0.2	0.127	0.5
10	10	64	0.1	1.4	1	0.2	0.127	0.5

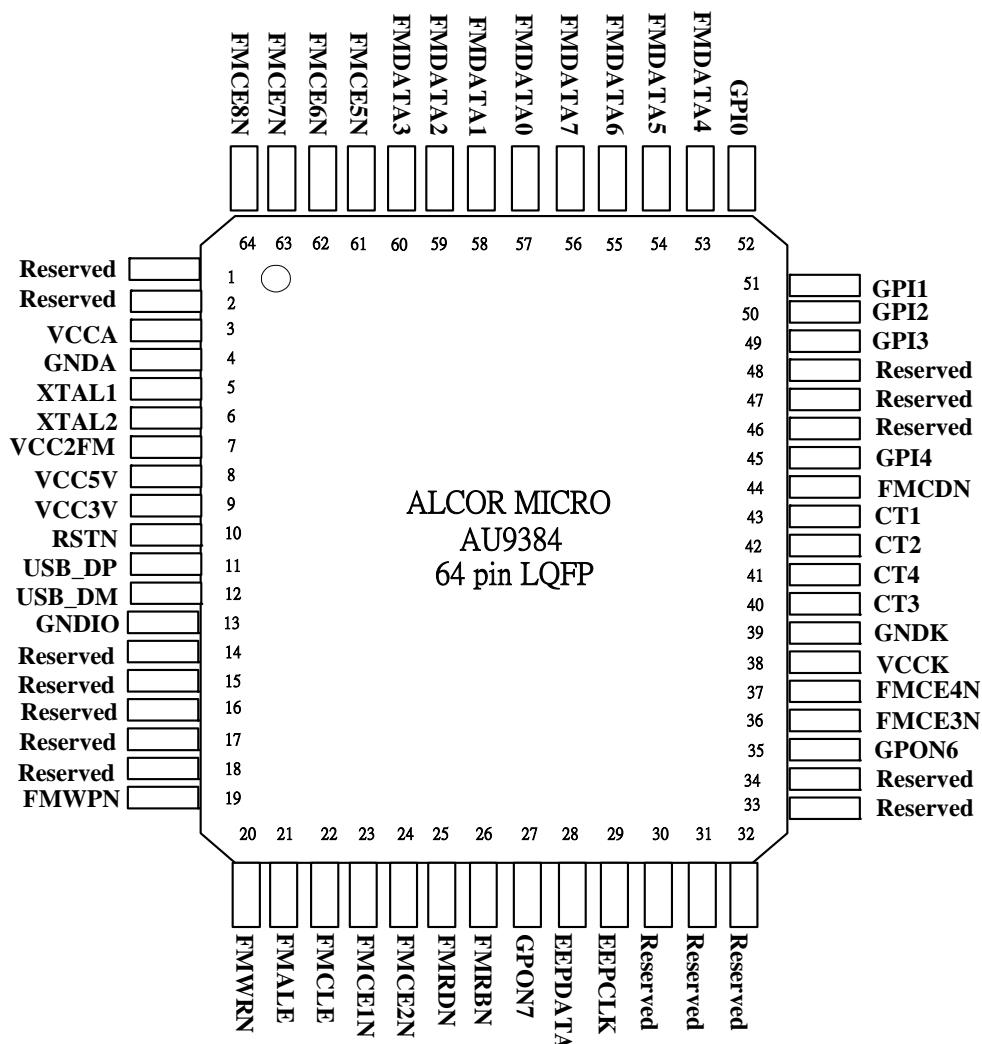
A1	stand-off
A2	body thickness
L1	lead length
b	lead width
c	lead thickness
e	lead pitch



7.0 APPENDIX-A-64 Pin LQFP Package

7.1 64 LQFP Pin assignment

Figure 7.1 64 LQFP Pin Assignment





7.2 64 LQFP Pin Descriptions

Table 7.1 64 LQFP Pin Descriptions

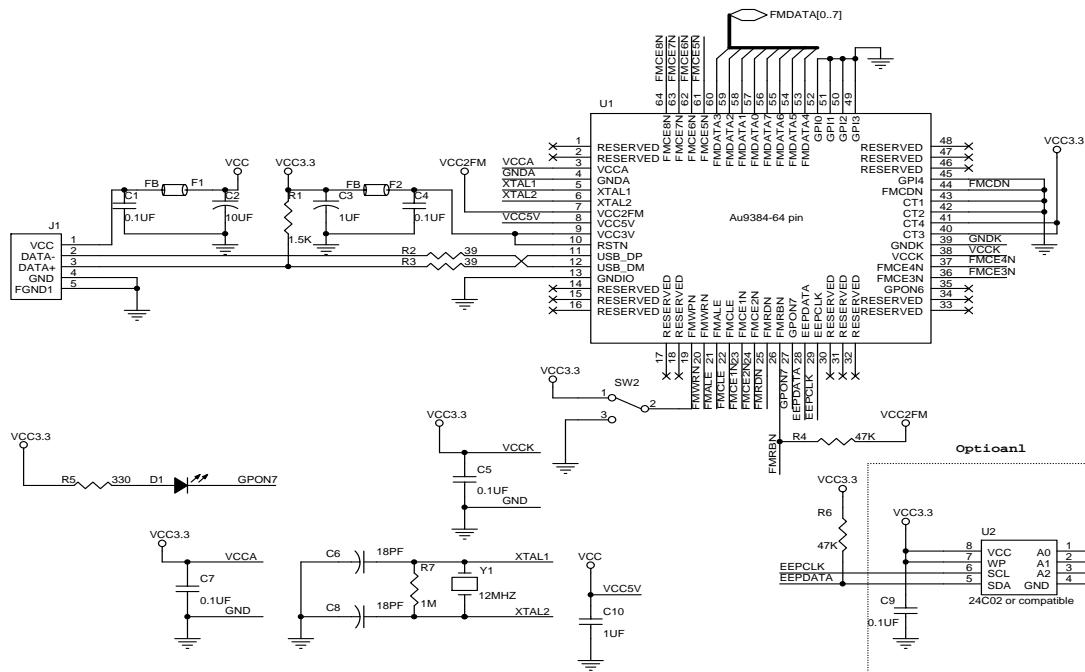
PIN	PIN Name	I/O Type	Description
1	Reserved		Reserved
2	Reserved		Reserved
3	VCCA	PWR	Analog 3.3V input
4	GNDA	PWR	Ground
5	XTAL1	I	Crystal Oscillator Input (12MHz)
6	XTAL2	O	Crystal Oscillator Output (12MHz)
7	VCC2FM	O	Connect to Flash Memory VCC
8	VCC5V	PWR	5V power supply
9	VCC3V	PWR	Regular 3.3V output/ IO 3.3V input
10	RSTN	I	Hardware reset (Active Low)
11	USB_DP	I/O	USB D+
12	USB_DM	I/O	USB D-
13	GNDIO	PWR	Ground
14	Reserved		Reserved
15	Reserved		Reserved
16	Reserved		Reserved
17	Reserved		Reserved
18	Reserved		Reserved
19	FMWPN	I	Connect to Flash Memory Write Protect
20	FMWRN	O	Connect to Flash Memory Write Enable
21	FMALE	O	Connect to Flash Memory Address Latch Enable
22	FMCLE	O	Connect to Flash Memory Command Latch Enable
23	FMCE1N	O	Connect to Flash Memory Chip1 Enable
24	FMCE2N	O	Connect to Flash Memory Chip2 Enable
25	FMRDN	O	Connect to Flash Memory Read Enable
26	FMRBN	I	Connect to Flash Memory Ready/Busy Output
27	GPON7	O	General Purpose Output pin, used as activity LED
28	EEPDATA	I/O	Connect to I2C Serial Data
29	EEPCLK	O	Connect to I2C Serial Clock Input
30	Reserved		Reserved
31	Reserved		Reserved
32	Reserved		Reserved
33	Reserved		Reserved
34	Reserved		Reserved
35	GPON6	O	Floating
36	FMCE3N	O	Connect to Flash Memory Chip3 Enable
37	FMCE4N	O	Connect to Flash Memory Chip4 Enable
38	VCCK	PWR	Core 3.3V Input
39	GNDK	PWR	Ground
40	CT3	I	Connect to VCC
41	CT4	I	Connect to VCC



42	CT2	I	Connect to ground
43	CT1	I	Connect to ground
44	FMCND	I	Flash Memory Mode: Connect to Ground
45	GPI4	I	Connect to ground.
46	Reserved		Reserved
47	Reserved		Reserved
48	Reserved		Reserved
49	GPI3	I	Connect to ground.
50	GPI2	I	Connect to ground.
51	GPI1	I	Connect to ground.
52	GPIO	I	Connect to ground.
53	FMDATA4	I/O	Connect to Flash Memory Data IO4
54	FMDATA5	I/O	Connect to Flash Memory Data IO5
55	FMDATA6	I/O	Connect to Flash Memory Data IO6
56	FMDATA7	I/O	Connect to Flash Memory Data IO7
57	FMDATA0	I/O	Connect to Flash Memory Data IO0
58	FMDATA1	I/O	Connect to Flash Memory Data IO1
59	FMDATA2	I/O	Connect to Flash Memory Data IO2
60	FMDATA3	I/O	Connect to Flash Memory Data IO3
61	FMCE5N	O	Connect to Flash Memory Chip5 Enable
62	FMCE6N	O	Connect to Flash Memory Chip6 Enable
63	FMCE7N	O	Connect to Flash Memory Chip7 Enable
64	FMCE8N	O	Connect to Flash Memory Chip8 Enable



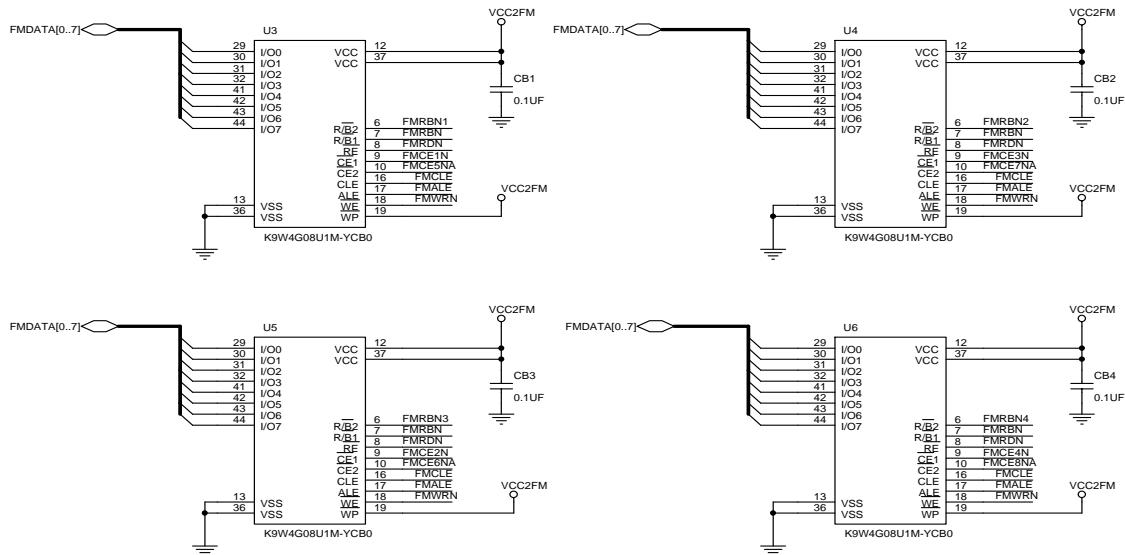
7.3 Sample Schematics





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