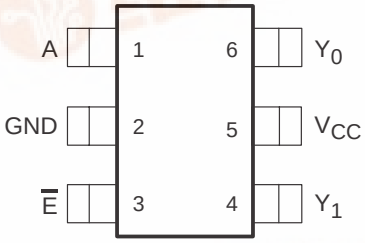
SN74AUC1G19
1-OF-2 DECODER/DEMULTIPLEXER

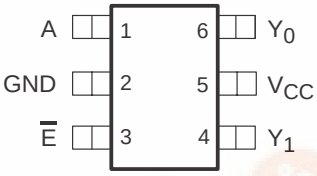
SCES626B – MARCH 2005 – JUNE 2005

- Available in the Texas Instruments NanoStar™ and NanoFree™ Package
- Optimized for 1.8-V Operation and is 3.6-V I/O Tolerant to Support Mixed-Mode Signal Operation
- I_{off} Supports Partial-Power-Down Mode Operation
- Sub-1-V Operable
- ±8-mA Output Drive at 1.8 V V_{CC}
- Max t_{pd} of 3 ns at 1.8 V V_{CC}
- Low Power Consumption, 10-μA Max I_{CC}
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

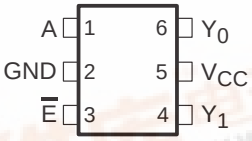
DBV PACKAGE
(TOP VIEW)



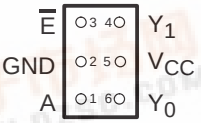
DCK PACKAGE
(TOP VIEW)



DRL PACKAGE
(TOP VIEW)



YEA, YEP, YZA,
OR YZP PACKAGE
(BOTTOM VIEW)



See mechanical drawings for dimensions.

description/ordering information

This 1-of-2 decoder/demultiplexer is operational at 0.8-V to 2.7-V V_{CC}, but is designed specifically for 1.65-V to 1.95-V V_{CC} operation.

The SN74AUC1G19 is a 1-of-2 decoder/demultiplexer. This device buffers the data on input A and passes it to the outputs Y_0 (true) and Y_1 (complement) when the enable ($\overline{E}$) input signal is low.

NanoStar™ and NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING‡
−40°C to 85°C	NanoStar™ – WCSP (DSBGA) 0.23-mm Large Bump – YEP	Reel of 3000	SN74AUC1G19YEPR	U5_
	NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)		SN74AUC1G19YZPR	
	SOT (SOT-23) – DBV	Reel of 3000	SN74AUC1G19DBVR	U19_
		Reel of 250	SN74AUC1G19DBVT	U19_
	SOT (SC-70) – DCK	Reel of 3000	SN74AUC1G19DCKR	U5_
		Reel of 250	SN74AUC1G19DCKT	
	SOT (SOT-553) – DRL	Reel of 4000	SN74AUC1G19DRLR	U5_

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

‡ DBV/DCK/DRL: The actual top-side marking has one additional character that designates the assembly/test site. YEP/YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, ● = Pb-free).

description/ordering information

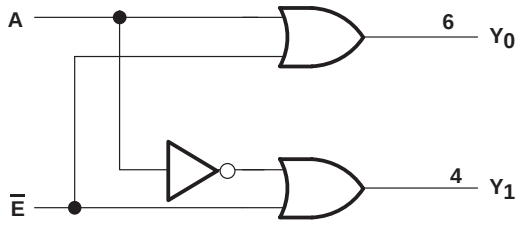
This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

For more information about AUC Little Logic devices, please refer to the TI application report, *Applications of Texas Instruments AUC Sub−1−V Little Logic Devices*, literature number SCEA027.

FUNCTION TABLE

INPUTS		OUTPUTS	
$\overline{E}$	A	Y_0	Y_1
L	L	L	H
L	H	H	L
H	X	H	H

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . −0.5 V to 3.6 V
Input voltage range, V_I (see Note 1) . . . . . −0.5 V to 3.6 V
Voltage range applied to any output in the high-impedance or power-off state, V_O
(see Note 1) . . . . . −0.5 V to 3.6 V
Voltage range applied to any output in the high or low state, V_O
(see Note 1 and Note 2) . . . . . −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0) . . . . . −50 mA
Output clamp current, I_{OK} (V_O < 0) . . . . . −50 mA
Continuous output current, I_O . . . . . ±20 mA
Continuous current through V_{CC} or GND . . . . . ±100 mA
Package thermal impedance, θ_{JA} (see Note 3): DBV package . . . . . 206°C/W
DCK package . . . . . 252°C/W
DRL package . . . . . 142°C/W
YEP/YZP package . . . . . 123°C/W
Storage temperature range, T_{stg} . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The value of V_{CC} is provided in the recommended operatng conditions table.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V_{CC}	Supply voltage	Operating	0.8	2.7	V
V_{IH}	High-level control input voltage	V_{CC} = 0.8 V	V_{CC}	3.6	V
		V_{CC} = 1.1 V to 1.95 V	$0.65 \times V_{CC}$	3.6	V
		V_{CC} = 2.3 V to 2.7 V	1.7	3.6	
V_{IL}	Low-level control input voltage	V_{CC} = 0.8 V		0	V
		V_{CC} = 1.1 V to 1.95 V	0	$0.35 \times V_{CC}$	V
		V_{CC} = 2.3 V to 2.7 V	0	0.7	
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level control output current	V_{CC} = 0.8 V		−0.7	mA
		V_{CC} = 1.1 V		−3	
		V_{CC} = 1.4 V		−5	
		V_{CC} = 1.65 V		−8	
		V_{CC} = 2.3 V		−9	
I_{OL}	Low-level control output current	V_{CC} = 0.8 V		0.7	mA
		V_{CC} = 1.1 V		3	
		V_{CC} = 1.4 V		5	
		V_{CC} = 1.65 V		8	
		V_{CC} = 2.3 V		9	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 0.8 V to 1.95 V		20	ns/V
		V_{CC} = 2.3 V to 2.7 V		15	ns/V
T_A	Operating free-air temperature		−40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	MIN	TYP†	MAX	UNIT
V_{OH}	I_{OH} = −100 μA		0.8 V to 2.7 V	V_{CC} − 0.1			V
	I_{OH} = −0.7 mA		0.8 V		0.55		
	I_{OH} = −3 mA		1.1 V	0.8			
	I_{OH} = −5 mA		1.4 V	1			
	I_{OH} = −8 mA		1.65 V	1.2			
	I_{OH} = −9 mA		2.3 V	1.8			
V_{OL}	I_{OL} = 100 μA		0.8 V to 2.7 V			0.2	V
	I_{OL} = 0.7 mA		0.8 V		0.25		
	I_{OL} = 3 mA		1.1 V			0.3	
	I_{OL} = 5 mA		1.4 V			0.4	
	I_{OL} = 8 mA		1.65 V			0.45	
	I_{OL} = 9 mA		2.3 V			0.6	
I_I	$V_I = V_{CC}$ or GND		0 to 2.7 V			±5	μA
I_{off}	V_I or V_O = 2.7 V		0			±10	μA
I_{CC}	$V_I = V_{CC}$ or GND,	I_O = 0	0.8 V to 2.7 V			10	μA
C_i	$V_I = V_{CC}$ or GND		2.5 V		2.5		pF

† All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.

switching characteristics over recommended operating free-air temperature range, C_L = 15 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 0.8 V	V_{CC} = 1.1 V ± 0.1 V		V_{CC} = 1.5 V ± 0.1 V		V_{CC} = 1.8 V ± 0.15 V		V_{CC} = 2.5 V ± 0.2 V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or $\overline{E}$	Y	7.5	0.5	4.6	0.4	3.0	0.3	2.4	0.2	1.7	ns

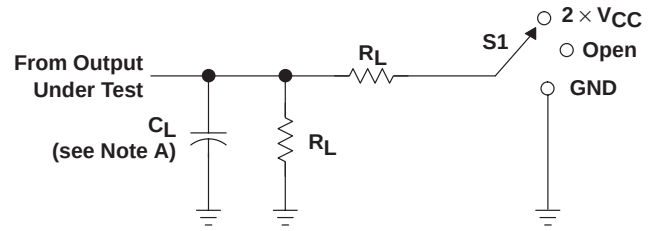
switching characteristics over recommended operating free-air temperature range, C_L = 30 pF (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 1.8 V ± 0.15 V		V_{CC} = 2.5 V ± 0.2 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}	A or $\overline{E}$	Y_0 or Y_1	0.5	2.8	0.4	2.0	ns

operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC} = 0.8 V	V_{CC} = 1.2 V	V_{CC} = 1.5 V	V_{CC} = 1.8 V	V_{CC} = 2.5 V	UNIT
			TYP	TYP	TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance	f = 10 MHz	13	13	13	13	14	pF

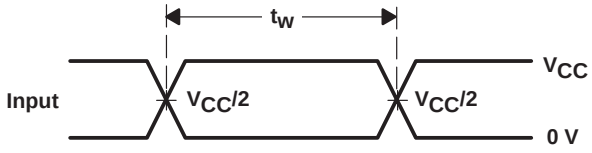
PARAMETER MEASUREMENT INFORMATION



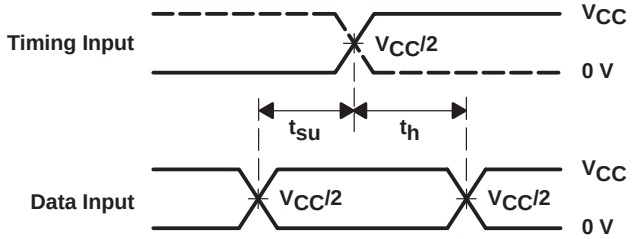
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND

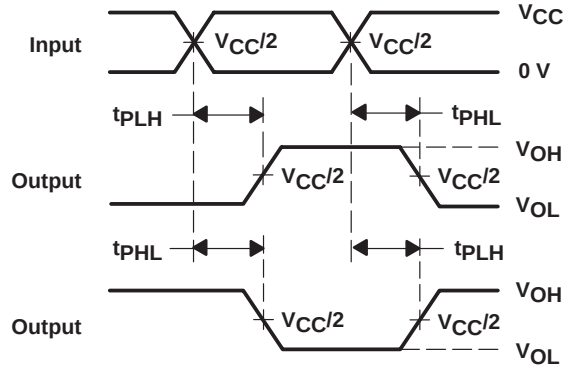
V_{CC}	C_L	R_L	V_Δ
0.8 V	15 pF	2 kΩ	0.1 V
1.2 V ± 0.1 V	15 pF	2 kΩ	0.1 V
1.5 V ± 0.1 V	15 pF	2 kΩ	0.1 V
1.8 V ± 0.15 V	15 pF	2 kΩ	0.15 V
2.5 V ± 0.2 V	15 pF	2 kΩ	0.15 V
1.8 V ± 0.15 V	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	30 pF	500 Ω	0.15 V



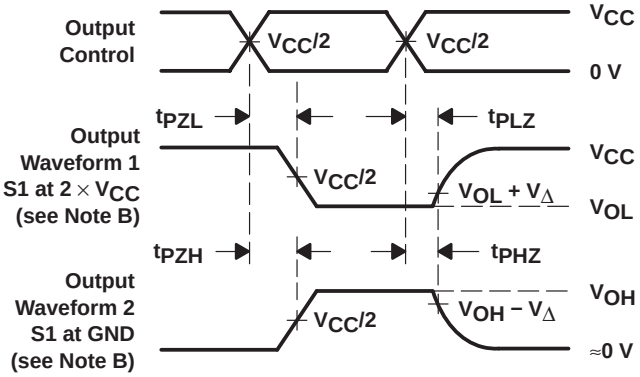
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, slew rate ≥ 1 V/ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

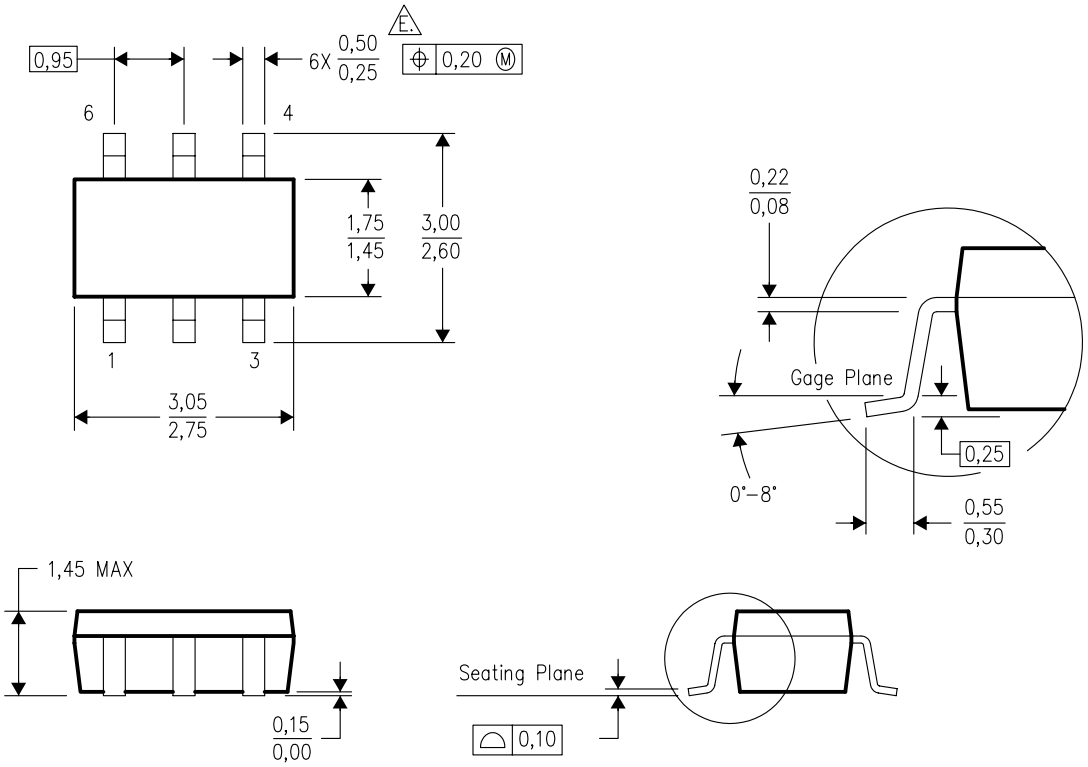
Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
SN74AUC1G19DBVR	ACTIVE	SOT-23	DBV	6	3000	Pb-Free (RoHS)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUC1G19DBVRE4	ACTIVE	SOT-23	DBV	6	3000	Pb-Free (RoHS)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUC1G19DBVT	ACTIVE	SOT-23	DBV	6	250	Pb-Free (RoHS)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUC1G19DBVTE4	ACTIVE	SOT-23	DBV	6	250	Pb-Free (RoHS)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUC1G19DCKR	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUC1G19DCKRE4	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUC1G19DCKT	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUC1G19DCKTE4	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUC1G19DRLR	ACTIVE	SOP	DRL	6	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUC1G19YEPR	ACTIVE	WCSP	YEP	6	3000	TBD	SNPB	Level-1-260C-UNLIM
SN74AUC1G19YZPR	ACTIVE	WCSP	YZP	6	3000	Pb-Free (RoHS)	SNAGCU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

DBV (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE

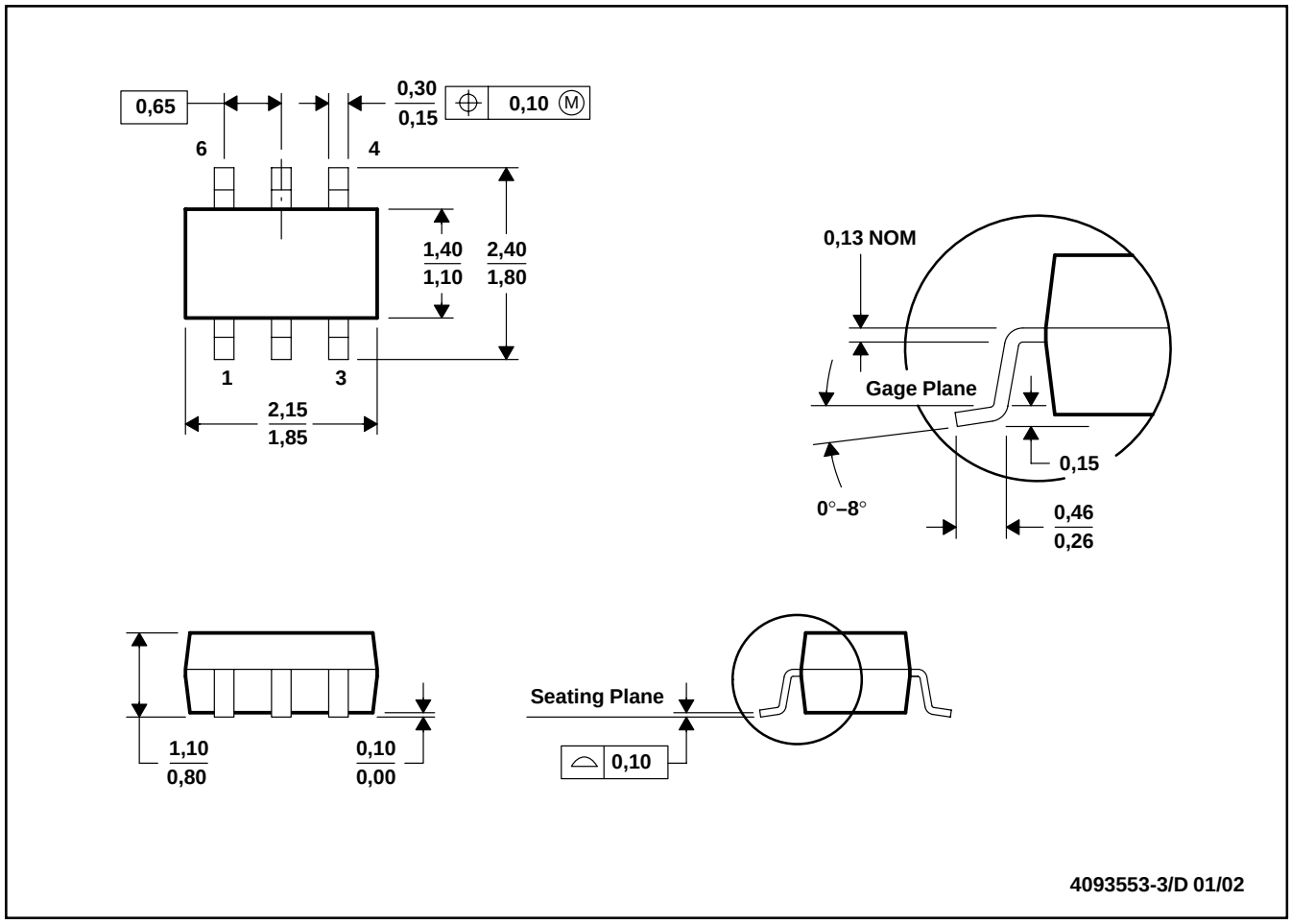


4073253–5/I 04/2005

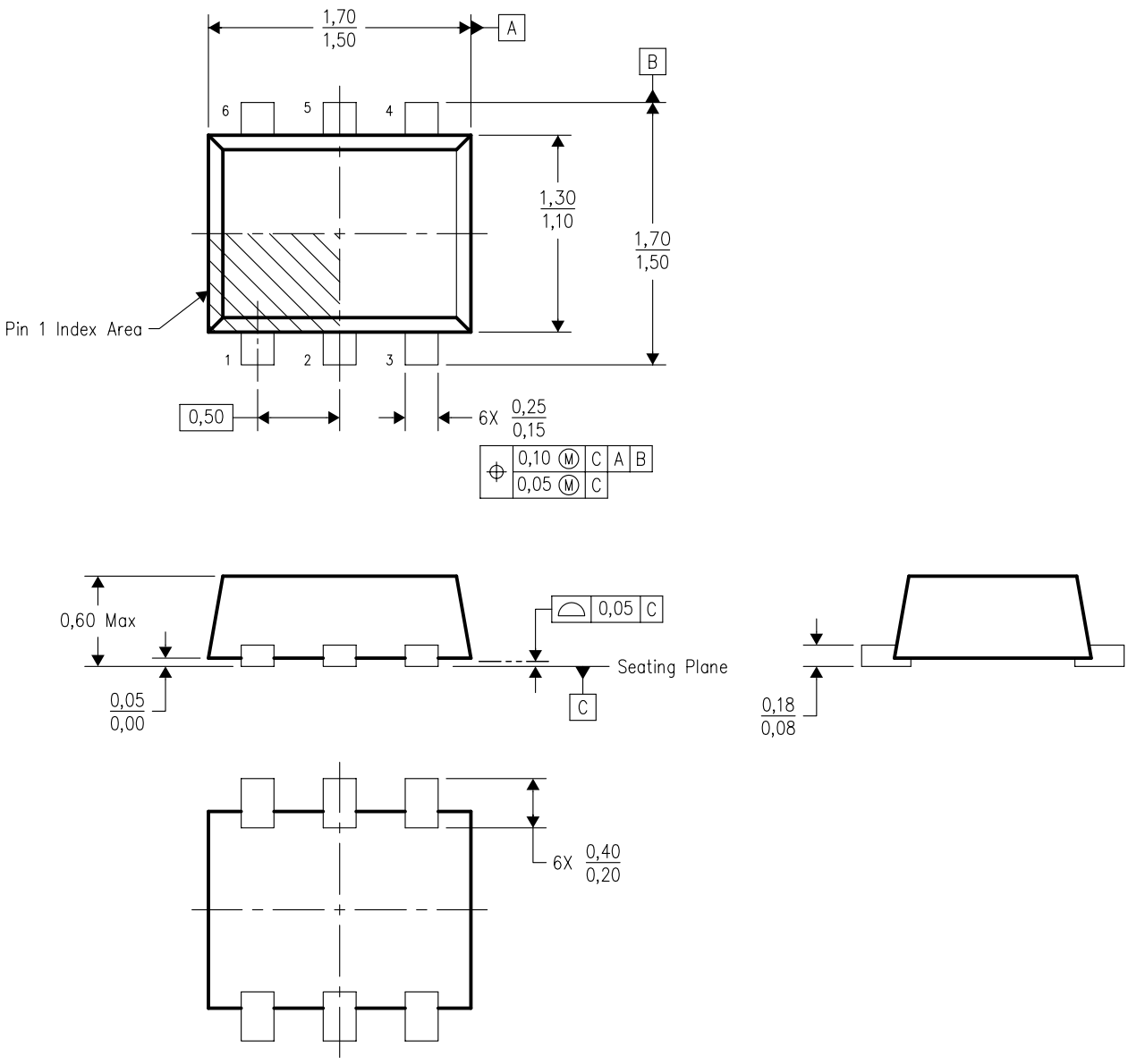
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
E. Falls within JEDEC MO–178 Variation AB, except minimum lead width.

MPDS114 – FEBRUARY 2002

DCK (R-PDSO-G6) **PLASTIC SMALL-OUTLINE PACKAGE**

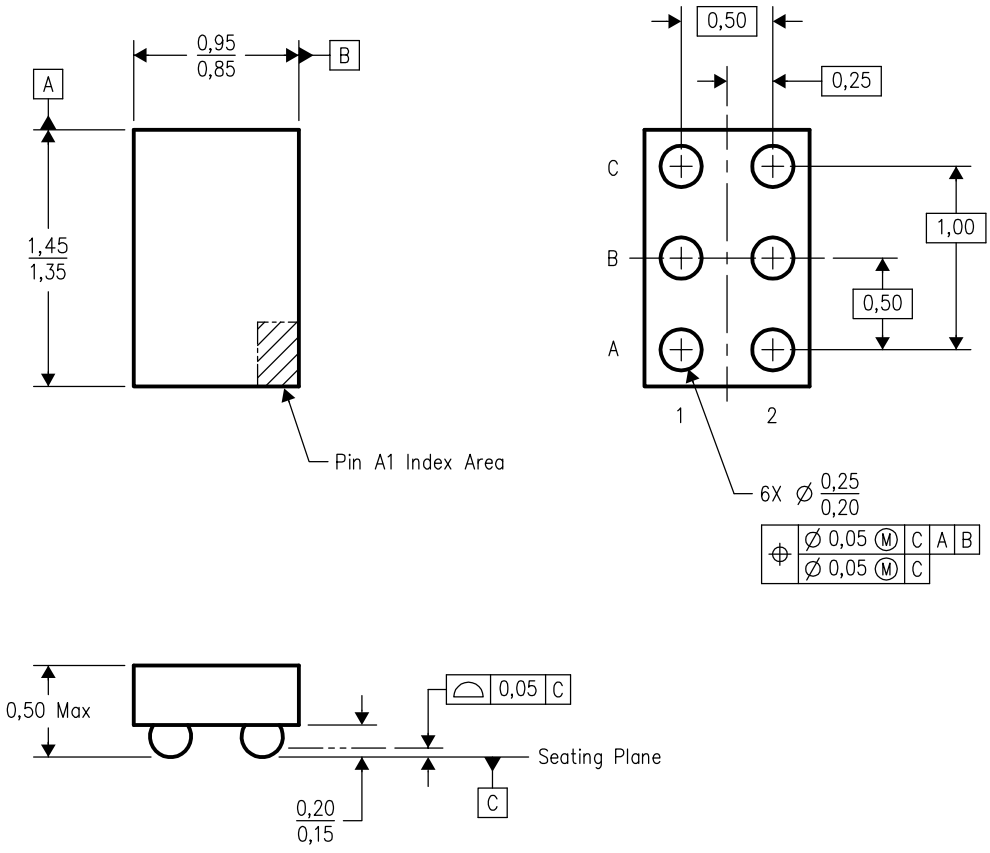


NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO-203



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. JEDEC package registration is pending.

YZP (R–XBGA–N6) DIE–SIZE BALL GRID ARRAY

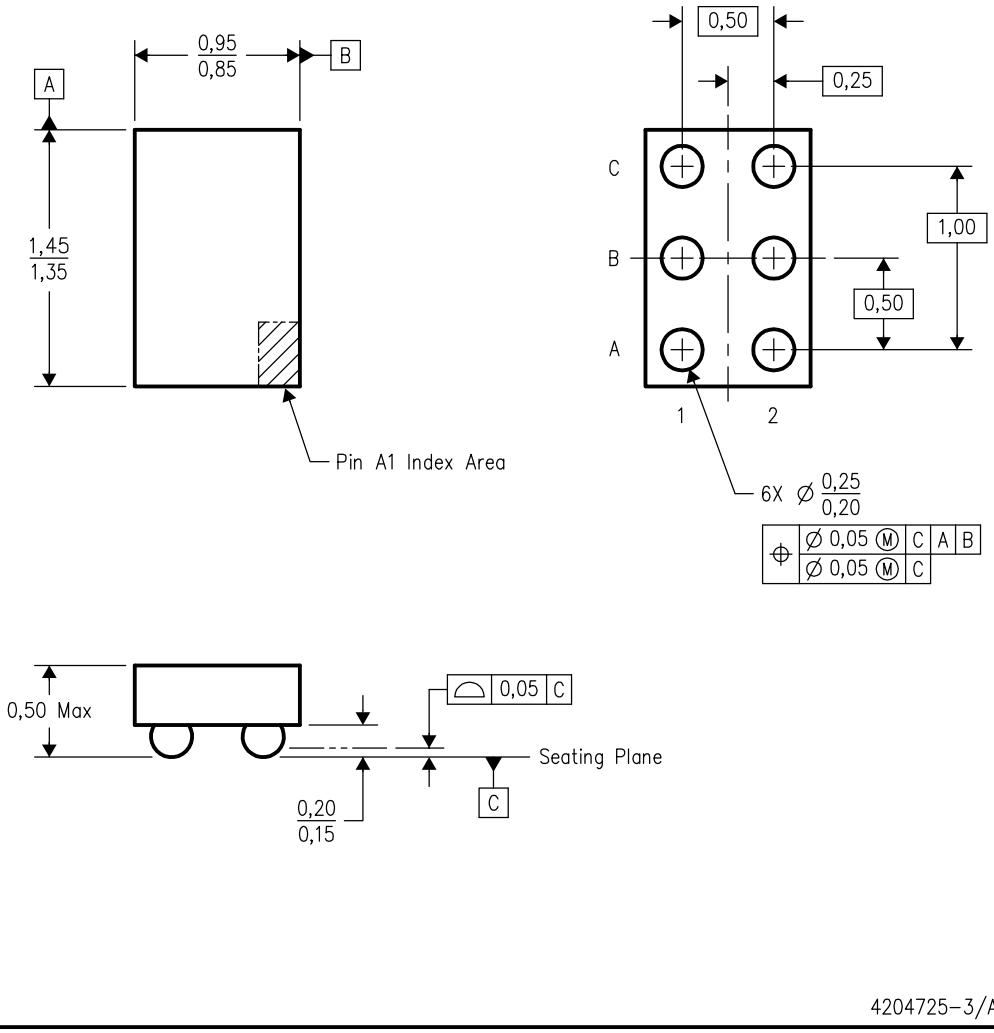


4204741–3/A 10/2002

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.
D. This package is lead–free. Refer to the 6 YEP package (drawing 4204725) for tin–lead (SnPb).

NanoFree is a trademark of Texas Instruments.

YEP (R–XBGA–N6) DIE–SIZE BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. NanoStar™ package configuration.
D. This package is tin–lead (SnPb). Refer to the 6 YZP package (drawing 4204741) for lead–free.

NanoStar is a trademark of Texas Instruments.

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