

- Member of the Texas Instruments Widebus+™ Family
- Optimized for 1.8-V Operation and is 3.6-V I/O Tolerant to Support Mixed-Mode Signal Operation
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Sub 1-V Operable
- Max  $t_{pd}$  of 2.8 ns at 1.8 V
- Low Power Consumption, 40- $\mu$ A Max  $I_{CC}$

- $\pm 8$ -mA Output Drive at 1.8 V
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

#### description/ordering information

This 32-bit edge-triggered D-type flip-flop is operational at 0.8-V to 2.7-V  $V_{CC}$ , but is designed specifically for 1.65-V to 1.95-V  $V_{CC}$  operation.

The SN74AUCH32374 is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers. It can be used as four 8-bit flip-flops, two 16-bit flip-flops, or one 32-bit flip-flop. On the positive transition of the clock (CLK) input, the Q outputs of the flip-flop take on the logic levels set up at the data (D) inputs.

A buffered output-enable ( $\overline{OE}$ ) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

$\overline{OE}$  does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

#### ORDERING INFORMATION

TA	PACKAGE <sup>†</sup>	ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	LFBGA – GKE	Tape and reel	SN74AUCH32374GKER

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

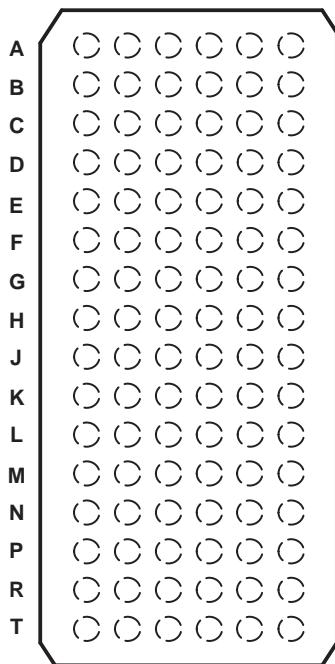
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**SN74AUCH32374**  
**32-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP**  
**WITH 3-STATE OUTPUTS**

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**GKE PACKAGE**  
**(TOP VIEW)**

1 2 3 4 5 6



**terminal assignments**

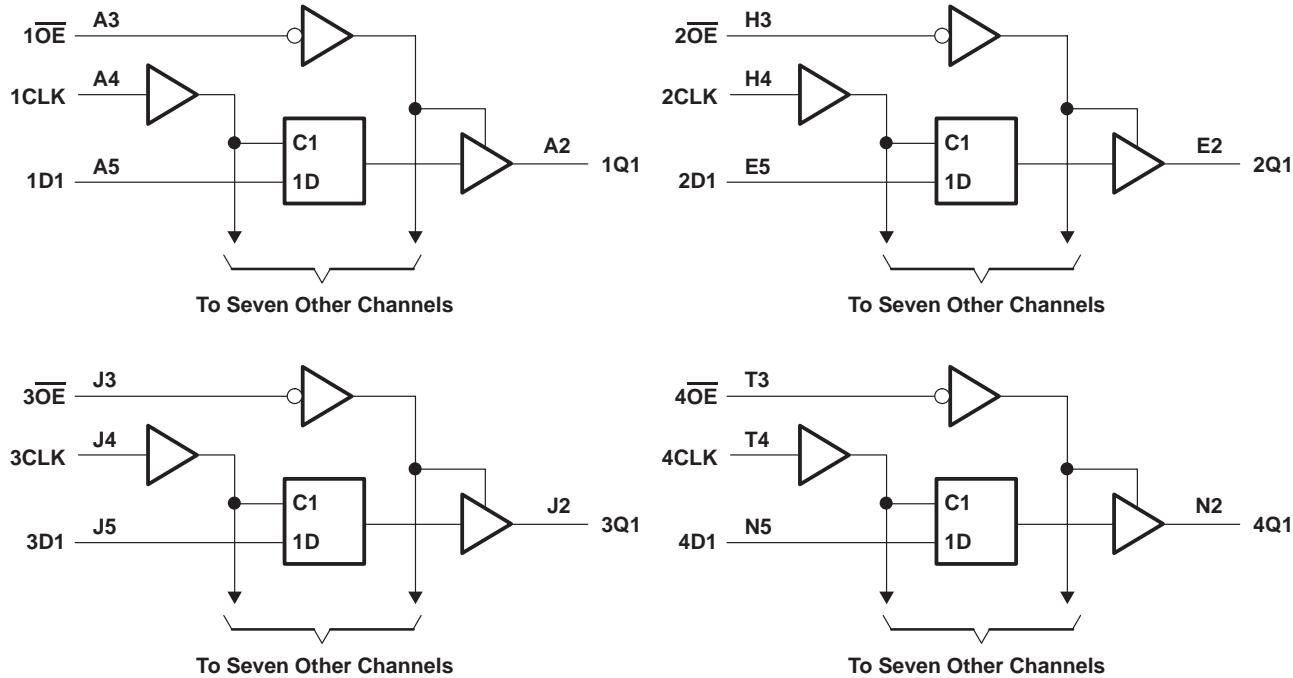
	1	2	3	4	5	6
<b>A</b>	1Q2	1Q1	$\overline{1OE}$	1CLK	1D1	1D2
<b>B</b>	1Q4	1Q3	GND	GND	1D3	1D4
<b>C</b>	1Q6	1Q5	V <sub>CC</sub>	V <sub>CC</sub>	1D5	1D6
<b>D</b>	1Q8	1Q7	GND	GND	1D7	1D8
<b>E</b>	2Q2	2Q1	GND	GND	2D1	2D2
<b>F</b>	2Q4	2Q3	V <sub>CC</sub>	V <sub>CC</sub>	2D3	2D4
<b>G</b>	2Q6	2Q5	GND	GND	2D5	2D6
<b>H</b>	2Q7	2Q8	$\overline{2OE}$	2CLK	2D8	2D7
<b>J</b>	3Q2	3Q1	$\overline{3OE}$	3CLK	3D1	3D2
<b>K</b>	3Q4	3Q3	GND	GND	3D3	3D4
<b>L</b>	3Q6	3Q5	V <sub>CC</sub>	V <sub>CC</sub>	3D5	3D6
<b>M</b>	3Q8	3Q7	GND	GND	3D7	3D8
<b>N</b>	4Q2	4Q1	GND	GND	4D1	4D2
<b>P</b>	4Q4	4Q3	V <sub>CC</sub>	V <sub>CC</sub>	4D3	4D4
<b>R</b>	4Q6	4Q5	GND	GND	4D5	4D6
<b>T</b>	4Q7	4Q8	$\overline{4OE}$	4CLK	4D8	4D7

**FUNCTION TABLE**  
(*each flip-flop*)

INPUTS			OUTPUT Q
$\overline{OE}$	CLK	D	
L	↑	H	H
L	↑	L	L
L	H or L	X	$Q_0$
H	X	X	Z

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**logic diagram (positive logic)**



**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>**

Supply voltage range, $V_{CC}$ .....	-0.5 V to 3.6 V
Input voltage range, $V_I$ (see Note 1) .....	-0.5 V to 3.6 V
Voltage range applied to any output in the high-impedance or power-off state, $V_O$ (see Note 1) .....	-0.5 V to 3.6 V
Output voltage range, $V_O$ (see Note 1) .....	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....	-50 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ ) .....	-50 mA
Continuous output current, $I_O$ .....	$\pm 20$ mA
Continuous current through $V_{CC}$ or GND .....	$\pm 100$ mA
Package thermal impedance, $\theta_{JA}$ (see Note 2) .....	40°C/W
Storage temperature range, $T_{stg}$ .....	-65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51-7.

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**recommended operating conditions (see Note 3)**

			MIN	MAX	UNIT
$V_{CC}$	Supply voltage		0.8	2.7	V
$V_{IH}$	High-level input voltage	$V_{CC} = 0.8\text{ V}$	$V_{CC}$		V
		$V_{CC} = 1.1\text{ V to }1.95\text{ V}$	$0.65 \times V_{CC}$		
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	1.7		
$V_{IL}$	Low-level input voltage	$V_{CC} = 0.8\text{ V}$	0		V
		$V_{CC} = 1.1\text{ V to }1.95\text{ V}$	$0.35 \times V_{CC}$		
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	0.7		
$V_I$	Input voltage		0	3.6	V
$V_O$	Output voltage	Active state	0	$V_{CC}$	V
		3-state	0	3.6	V
$I_{OH}$	High-level output current	$V_{CC} = 0.8\text{ V}$	–0.7		mA
		$V_{CC} = 1.1\text{ V}$	–3		
		$V_{CC} = 1.4\text{ V}$	–5		
		$V_{CC} = 1.65\text{ V}$	–8		
		$V_{CC} = 2.3\text{ V}$	–9		
$I_{OL}$	Low-level output current	$V_{CC} = 0.8\text{ V}$	0.7		mA
		$V_{CC} = 1.1\text{ V}$	3		
		$V_{CC} = 1.4\text{ V}$	5		
		$V_{CC} = 1.65\text{ V}$	8		
		$V_{CC} = 2.3\text{ V}$	9		
$\Delta t/\Delta V$	Input transition rise or fall rate		20		ns/V
$T_A$	Operating free-air temperature		–40	85	°C

NOTE 3: All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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**32-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP  
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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP <sup>†</sup>	MAX	UNIT
V <sub>OH</sub>	I <sub>OH</sub> = -100 $\mu$ A		0.8 V to 2.7 V	V <sub>CC</sub> -0.1			V
	I <sub>OH</sub> = -0.7 mA		0.8 V		0.55		
	I <sub>OH</sub> = -3 mA		1.1 V		0.8		
	I <sub>OH</sub> = -5 mA		1.4 V		1		
	I <sub>OH</sub> = -8 mA		1.65 V		1.2		
	I <sub>OH</sub> = -9 mA		2.3 V		1.8		
V <sub>OL</sub>	I <sub>OL</sub> = 100 $\mu$ A		0.8 V to 2.7 V		0.2		V
	I <sub>OL</sub> = 0.7 mA		0.8 V		0.25		
	I <sub>OL</sub> = 3 mA		1.1 V		0.3		
	I <sub>OL</sub> = 5 mA		1.4 V		0.4		
	I <sub>OL</sub> = 8 mA		1.65 V		0.45		
	I <sub>OL</sub> = 9 mA		2.3 V		0.6		
I <sub>I</sub>	All inputs	V <sub>I</sub> = V <sub>CC</sub> or GND	0 to 2.7 V		$\pm 5$		$\mu$ A
I <sub>BHL</sub> <sup>‡</sup>	V <sub>I</sub> = 0.35 V		1.1 V		10		$\mu$ A
	V <sub>I</sub> = 0.47 V		1.4 V		15		
	V <sub>I</sub> = 0.57 V		1.65 V		20		
	V <sub>I</sub> = 0.7 V		2.3 V		40		
I <sub>BHH</sub> <sup>§</sup>	V <sub>I</sub> = 0.8 V		1.1 V		-5		$\mu$ A
	V <sub>I</sub> = 0.9 V		1.4 V		-15		
	V <sub>I</sub> = 1.07 V		1.65 V		-20		
	V <sub>I</sub> = 1.7 V		2.3 V		-40		
I <sub>BHLO</sub> <sup>¶</sup>	V <sub>I</sub> = 0 to V <sub>CC</sub>		1.3 V		75		$\mu$ A
			1.6 V		125		
			1.95 V		175		
			2.7 V		275		
I <sub>BHHO</sub> <sup>#</sup>	V <sub>I</sub> = 0 to V <sub>CC</sub>		1.3 V		-75		$\mu$ A
			1.6 V		-125		
			1.95 V		-175		
			2.7 V		-275		
I <sub>off</sub>	V <sub>I</sub> or V <sub>O</sub> = 2.7 V		0		$\pm 10$		$\mu$ A
I <sub>OZ</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND		2.7 V		$\pm 10$		$\mu$ A
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0		0.8 V to 2.7 V		40		$\mu$ A
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND		2.5 V		3		pF
C <sub>o</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND		2.5 V		5		pF

<sup>†</sup> All typical values are at T<sub>A</sub> = 25°C.

<sup>‡</sup> The bus-hold circuit can sink at least the minimum low sustaining current at V<sub>IL</sub> max. I<sub>BHL</sub> should be measured after lowering V<sub>IN</sub> to GND and then raising it to V<sub>IL</sub> max.

<sup>§</sup> The bus-hold circuit can source at least the minimum high sustaining current at V<sub>IH</sub> min. I<sub>BHH</sub> should be measured after raising V<sub>IN</sub> to V<sub>CC</sub> and then lowering it to V<sub>IH</sub> min.

<sup>¶</sup> An external driver must source at least I<sub>BHLO</sub> to switch this node from low to high.

<sup>#</sup> An external driver must sink at least I<sub>BHHO</sub> to switch this node from high to low.

# SN74AUCH32374

## 32-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP

### WITH 3-STATE OUTPUTS

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		V <sub>CC</sub> = 0.8 V	V <sub>CC</sub> = 1.2 V ± 0.1 V		V <sub>CC</sub> = 1.5 V ± 0.1 V		V <sub>CC</sub> = 1.8 V ± 0.15 V		V <sub>CC</sub> = 2.5 V ± 0.2 V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	
f <sub>clock</sub>	Clock frequency	85		250		250		250		250	MHz
t <sub>w</sub>	Pulse duration, CLK high or low	5.9		1.9		1.9		1.9		1.9	ns
t <sub>su</sub>	Setup time, data before CLK↑	1.4		1.2		0.7		0.6		0.6	ns
t <sub>h</sub>	Hold time, data after CLK↑	0.1		0.4		0.4		0.4		0.4	ns

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 0.8 V	V <sub>CC</sub> = 1.2 V ± 0.1 V		V <sub>CC</sub> = 1.5 V ± 0.1 V		V <sub>CC</sub> = 1.8 V ± 0.15 V			V <sub>CC</sub> = 2.5 V ± 0.2 V		UNIT
				TYP	MIN	MAX	MIN	MAX	MIN	TYP	MAX	MIN	
f <sub>max</sub>			85	250		250		250		250		250	MHz
t <sub>pd</sub>	CLK	Q	7.3	1	4.5	0.8	2.9	0.7	1.5	2.8	0.7	2.2	ns
t <sub>en</sub>	OE	Q	7	1.2	5.3	0.8	3.6	0.8	1.5	2.9	0.7	2.2	ns
t <sub>dis</sub>	OE	Q	8.2	2	7.1	1	4.8	1.4	2.7	4.5	0.5	2.2	ns

### operating characteristics, T<sub>A</sub> = 25°C†

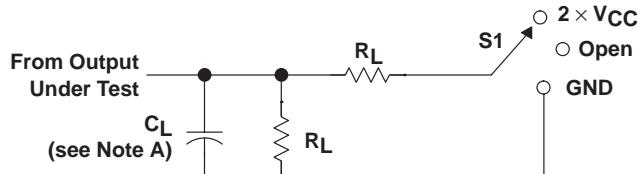
PARAMETER	TEST CONDITIONS	V <sub>CC</sub> = 0.8 V	V <sub>CC</sub> = 1.2 V		V <sub>CC</sub> = 1.5 V		V <sub>CC</sub> = 1.8 V		V <sub>CC</sub> = 2.5 V		UNIT
			TYP	TYP	TYP	TYP	TYP	TYP	TYP	TYP	
C <sub>pd</sub> ‡ (each output)	Power dissipation capacitance	Outputs enabled, 1 output switching	1 f <sub>data</sub> = 5 MHz 1 f <sub>clk</sub> = 10 MHz 1 f <sub>out</sub> = 5 MHz OE = GND C <sub>L</sub> = 0 pF	24	24	24.1	26.2	31.2			pF
C <sub>pd</sub> (Z)	Power dissipation capacitance	Outputs disabled, 1 clock and 1 data switching	1 f <sub>data</sub> = 5 MHz 1 f <sub>clk</sub> = 10 MHz f <sub>out</sub> = not switching OE = V <sub>CC</sub> C <sub>L</sub> = 0 pF	7.5	7.5	8	9.4	13.2			pF
C <sub>pd</sub> § (each clock)	Power dissipation capacitance	Outputs disabled, clock only switching	1 f <sub>data</sub> = 0 MHz 1 f <sub>clk</sub> = 10 MHz f <sub>out</sub> = not switching OE = V <sub>CC</sub> C <sub>L</sub> = 0 pF	13.8	13.8	14	14.7	17.5			pF

† Total device C<sub>pd</sub> for multiple (n) outputs switching and (y) clocks inputs switching = {n \* C<sub>pd</sub> (each output)} + {y \* C<sub>pd</sub> (each clock)}.

‡ C<sub>pd</sub> (each output) is the C<sub>pd</sub> for each data bit (input and output circuitry) as it operates at 5 MHz (Note: the clock is operating at 10 MHz in this test, but its I<sub>CC</sub> component has been subtracted out).

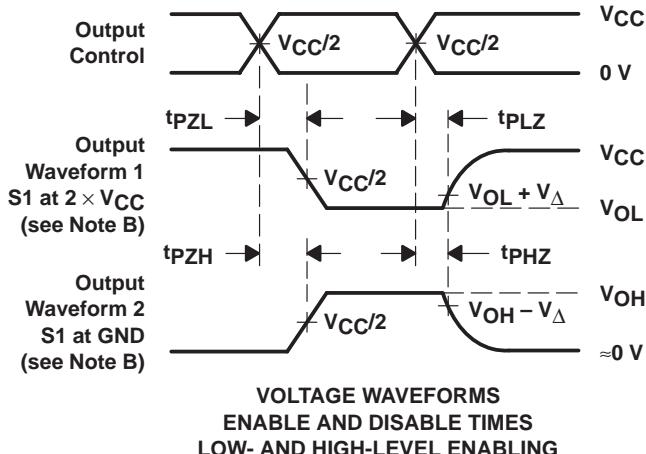
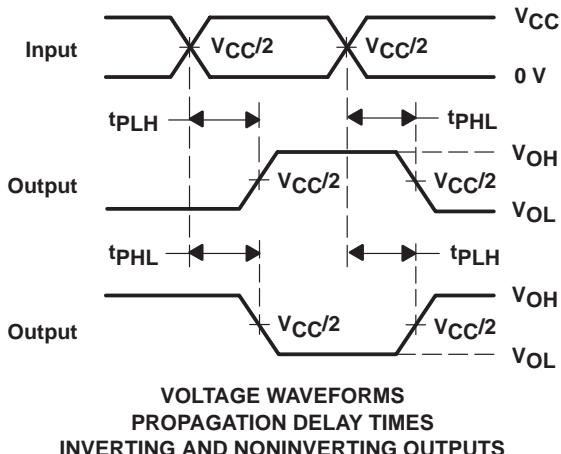
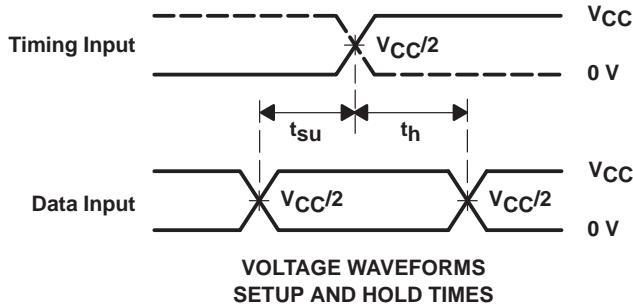
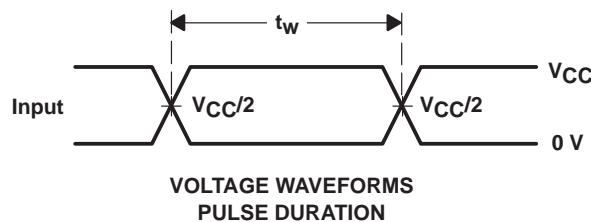
§ C<sub>pd</sub> (each clock) is the C<sub>pd</sub> for the clock circuitry only as it operates at 10 MHz.

## PARAMETER MEASUREMENT INFORMATION



TEST	S1
tPLH/tPHL	Open
tPLZ/tPZL	$2 \times V_{CC}$
tPHZ/tPZH	GND

$V_{CC}$	$C_L$	$R_L$	$V_\Delta$
0.8 V	15 pF	2 k $\Omega$	0.1 V
1.2 V $\pm$ 0.1 V	15 pF	2 k $\Omega$	0.1 V
1.5 V $\pm$ 0.1 V	15 pF	2 k $\Omega$	0.1 V
1.8 V $\pm$ 0.15 V	30 pF	1 k $\Omega$	0.15 V
2.5 V $\pm$ 0.2 V	30 pF	500 $\Omega$	0.15 V



NOTES:

- A.  $C_L$  includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50 \Omega$ , slew rate  $\geq 1 \text{ V/ns}$ .
- D. The outputs are measured one at a time with one transition per measurement.
- E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
- G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
- H. All parameters and waveforms are not applicable to all devices.

**Figure 1. Load Circuit and Voltage Waveforms**

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN74AUCH32374GKER	ACTIVE	LFBGA	GKE	96	1000	None	SNPB	Level-3-220C-168 HR
SN74AUCH32374ZKER	ACTIVE	LFBGA	ZKE	96	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-250C-168 HR

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - May not be currently available - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**None:** Not yet available Lead (Pb-Free).

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDECindustry standard classifications, and peak solder temperature.

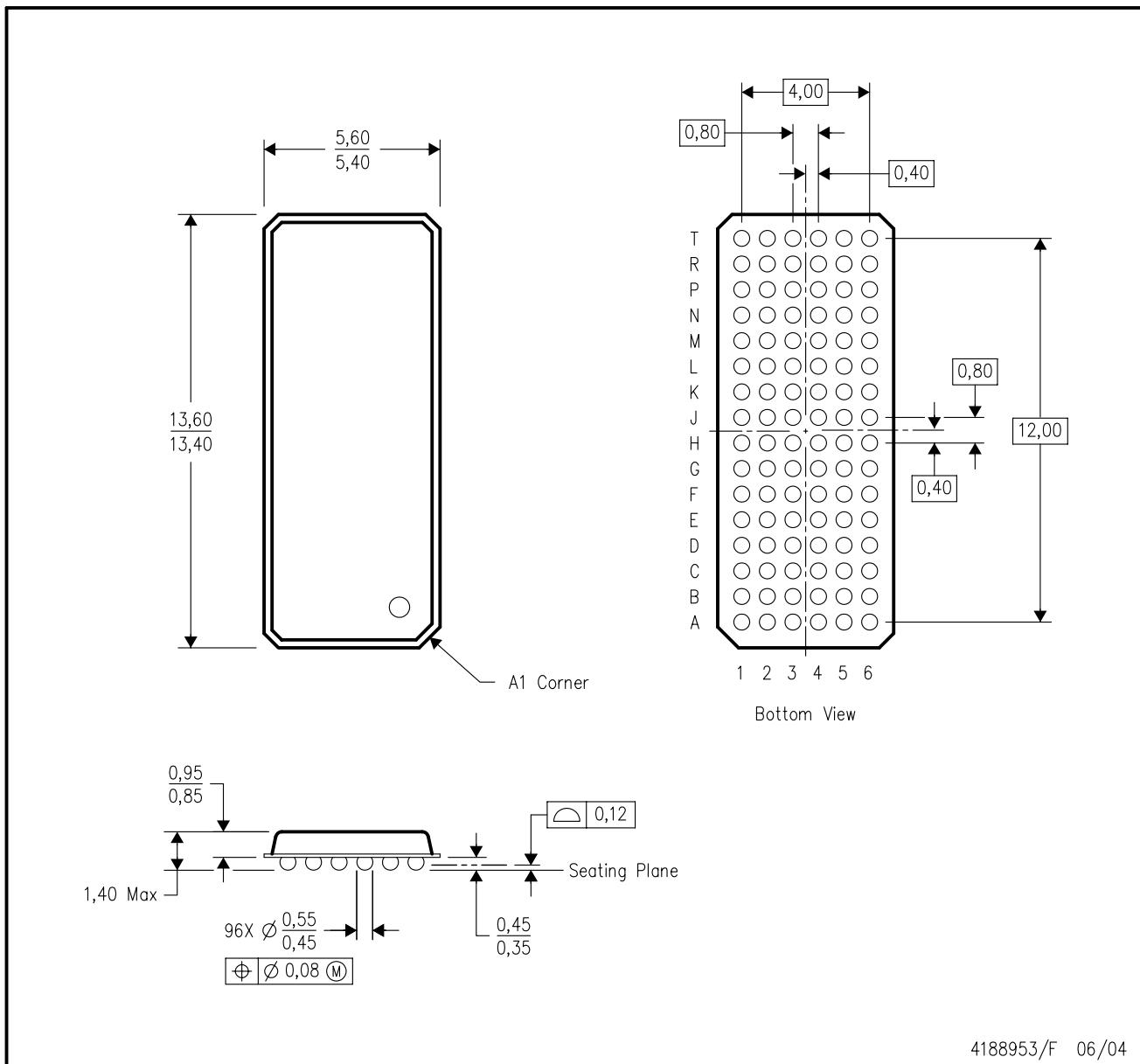
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## MECHANICAL DATA

## GKE (R-PBGA-N96)

## PLASTIC BALL GRID ARRAY

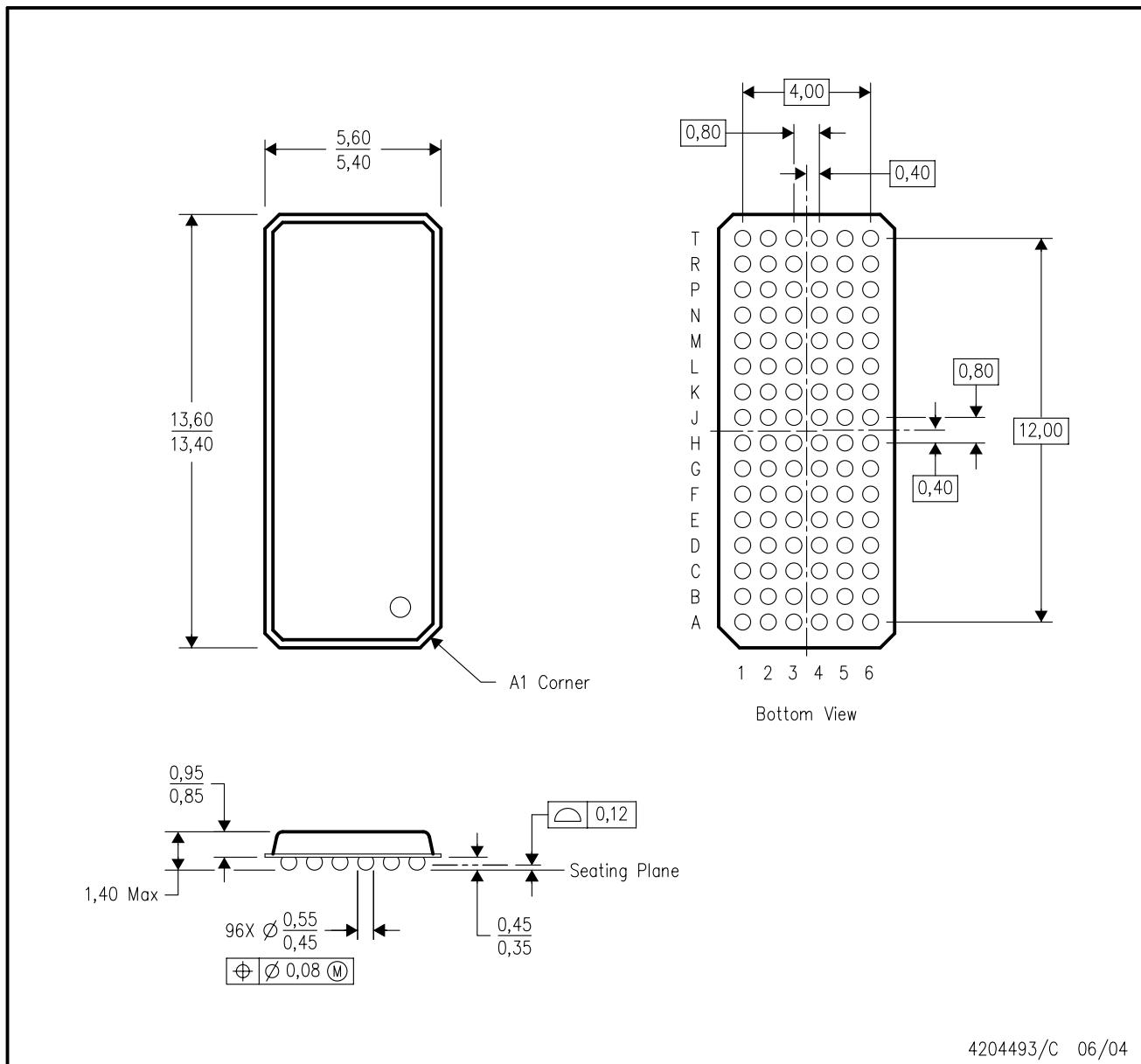


NOTES: A. All linear dimensions are in millimeters.  
B. This drawing is subject to change without notice.  
C. Falls within JEDEC M0-205 variation CC.  
D. This package is tin-lead (SnPb). Refer to the 96 ZKE package (drawing 4204493) for lead-free.

## MECHANICAL DATA

ZKE (R-PBGA-N96)

## PLASTIC BALL GRID ARRAY



NOTES: A. All linear dimensions are in millimeters.  
B. This drawing is subject to change without notice.  
C. Falls within JEDEC MO-205 variation CC.  
D. This package is lead-free. Refer to the 96 GKE package (drawing 4188953) for tin-lead (SnPb).

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