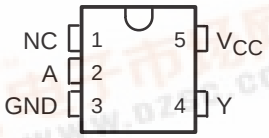
SN74AUP1G14
LOW-POWER SINGLE SCHMITT-TRIGGER INVERTER

SCES578 – JUNE 2004

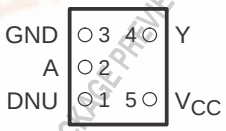
- Available in the Texas Instruments NanoStar™ and NanoFree™ Packages
- Low Static-Power Consumption; I_{CC} = 0.9-μA Max
- Low Dynamic-Power Consumption; C_{pd} = 4.4 pF Typical at 3.3 V
- Low Input Capacitance; C_i = 1.5 pF Typical
- Low Noise − Overshoot and Undershoot <10% of V_{CC}
- I_{off} Supports Partial-Power-Down Mode Operation
- Includes Schmitt-Trigger Inputs
- Wide Operating V_{CC} Range of 0.8 V to 3.6 V
- Optimized for 3.3-V Operation
- 3.6-V I/O Tolerant to Support Mixed-Mode Signal Operation
- t_{pd} = 4.9 ns Max at 3.3 V
- Suitable for Point-to-Point Applications
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
  - 2000-V Human-Body Model (A114-B, Class II)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)
- ESD Protection Exceeds ±5000-V With Human-Body Model

DBV OR DCK PACKAGE
(TOP VIEW)



NC − No internal connection

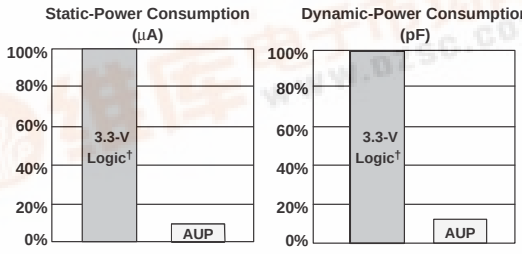
YEP OR YZP PACKAGE
(BOTTOM VIEW)



DNU − Do not use

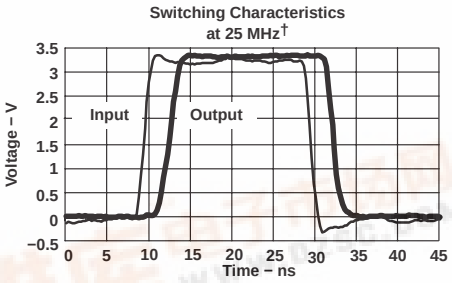
description/ordering information

The AUP family is TI's premier solution to the industry's low-power needs in battery-powered portable applications. This family ensures a very low static and dynamic power consumption across the entire V_{CC} range of 0.8 V to 3.6 V, resulting in an increased battery life. This product also maintains excellent signal integrity (see Figures 1 and 2).



† Single, dual, and triple gates.

Figure 1. AUP–The Lowest-Power Family



† AUP1G08 data at C_L = 15 pF.

Figure 2. Excellent Signal Integrity

This device functions as an independent gate with Schmitt-trigger inputs, which allows for slow input transition and better switching-noise immunity at the input.

NanoStar™ and NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

description/ordering information (continued)

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING‡
−40°C to 85°C	NanoStar™ – WCSP (DSBGA) 0.23-mm Large Bump – YEP	Reel of 3000	SN74AUP1G14YEPR	_ _ _HF_
	NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)		SN74AUP1G14YZPR	
	SOT (SOT-23) – DBV	Reel of 3000	SN74AUP1G14DBVR	H14_
		Reel of 250	SN74AUP1G14DBVT	
	SOT (SC-70) – DCK	Reel of 3000	SN74AUP1G14DCKR	HF_
		Reel of 250	SN74AUP1G14DCKT	

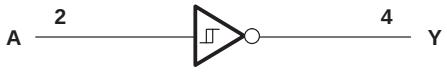
† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

‡ DBV/DCK: The actual top-side marking has one additional character that designates the assembly/test site.
YEP/YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).

FUNCTION TABLE

INPUT A	OUTPUT Y
H	L
L	H

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) . . . . . −0.5 V to 4.6 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1) . . . . . −0.5 V to 4.6 V
Output voltage range in the high or low state, V_O (see Note 1) . . . . . −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0) . . . . . −50 mA
Output clamp current, I_{OK} (V_O < 0) . . . . . −50 mA
Continuous output current, I_O . . . . . ±20 mA
Continuous current through V_{CC} or GND . . . . . ±50 mA
Package thermal impedance, θ_{JA} (see Note 2): DBV package . . . . . 206°C/W
DCK package . . . . . 252°C/W
YEP/YZP package . . . . . 132°C/W
Storage temperature range, T_{stg} . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and outpu negative-voltaget ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		0.8	3.6	V
V_I	Input voltage		0	3.6	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}‡	High-level output current	V_{CC} = 0.8 V		−20	μA
		V_{CC} = 1.1 V		−1.1	mA
		V_{CC} = 1.4 V		−1.7	
		V_{CC} = 1.65		−1.9	
		V_{CC} = 2.3 V		−3.1	
		V_{CC} = 3 V		−4	
I_{OL}‡	Low-level output current	V_{CC} = 0.8 V		20	μA
		V_{CC} = 1.1 V		1.1	mA
		V_{CC} = 1.4 V		1.7	
		V_{CC} = 1.65 V		1.9	
		V_{CC} = 2.3 V		3.1	
		V_{CC} = 3 V		4	
Δt/Δv	Input transition rise or fall rate	V_{CC} = 0.8 V to 3.6 V		200	ns/V
T_A	Operating free-air temperature		−40	85	°C

‡ Defined by the signal-integrity requirements and design-goal priorities.

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25 °C			T_A = −40 °C TO 85 °C		UNIT
				MIN	TYP	MAX	MIN	MAX	
V_{T+} Positive-going input threshold voltage			0.8 V	0.3		0.6	0.3	0.6	V
			1.1 V	0.53		0.9	0.53	0.9	
			1.4 V	0.74		1.11	0.74	1.11	
			1.65 V	0.91		1.29	0.91	1.29	
			2.3 V	1.37		1.77	1.37	1.77	
			3 V	1.88		2.29	1.88	2.29	
V_{T-} Negative-going input threshold voltage			0.8 V	0.1		0.6	0.1	0.6	V
			1.1 V	0.26		0.65	0.26	0.65	
			1.4 V	0.39		0.75	0.39	0.75	
			1.65 V	0.47		0.84	0.47	0.84	
			2.3 V	0.69		1.04	0.69	1.04	
			3 V	0.88		1.24	0.88	1.24	
ΔV_T Hysteresis ($V_{T+} - V_{T-}$)			0.8 V	0.07		0.5	0.07	0.5	V
			1.1 V	0.08		0.46	0.08	0.46	
			1.4 V	0.18		0.56	0.18	0.56	
			1.65 V	0.27		0.66	0.27	0.66	
			2.3 V	0.53		0.92	0.53	0.92	
			3 V	0.79		1.31	0.79	1.31	
V_{OH}	I_{OH} = −20 μA		0.8 V to 3.6 V	V_{CC} − 0.1			V_{CC} − 0.1		V
	I_{OH} = −1.1 mA		1.1 V	0.75 × V_{CC}			0.7 × V_{CC}		
	I_{OH} = −1.7 mA		1.4 V	1.11			1.03		
	I_{OH} = −1.9 mA		1.65 V	1.32			1.3		
	I_{OH} = −2.3 mA		2.3 V	2.05			1.97		
	I_{OH} = −3.1 mA			1.9			1.85		
	I_{OH} = −2.7 mA		3 V	2.72			2.67		
	I_{OH} = −4 mA			2.6			2.55		
V_{OL}	I_{OL} = 20 μA		0.8 V to 3.6 V			0.1		0.1	V
	I_{OL} = 1.1 mA		1.1 V			0.3 × V_{CC}		0.3 × V_{CC}	
	I_{OL} = 1.7 mA		1.4 V			0.31		0.37	
	I_{OL} = 1.9 mA		1.65 V			0.31		0.35	
	I_{OL} = 2.3 mA		2.3 V			0.31		0.33	
	I_{OL} = 3.1 mA					0.44		0.45	
	I_{OL} = 2.7 mA		3 V			0.31		0.33	
	I_{OL} = 4 mA					0.44		0.45	
I_I A input	V_I = GND to 3.6 V		0 V to 3.6 V			0.1		0.5	μA
I_{off}	V_I or V_O = 0 V to 3.6 V		0 V			0.2		0.6	μA
ΔI_{off}	V_I or V_O = 0 V to 3.6 V		0 V to 0.2 V			0.2		0.6	μA
I_{CC}	V_I = GND or (V_{CC} to 3.6 V)	I_O = 0	0.8 V to 3.6 V			0.5		0.9	μA
ΔI_{CC}	V_I = V_{CC} − 0.6 V	I_O = 0	3.3 V			40		50	μA

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

PARAMETER	TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	MIN	MAX	UNIT
C_i	$V_I = V_{CC}$ or GND	0 V		1.5				pF
		3.6 V		1.5				
C_o	V_O = GND	0 V		2.5				pF

switching characteristics over recommended operating free-air temperature range, C_L = 5 pF (unless otherwise noted) (see Figures 3 and 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25 °C			T_A = −40 °C TO 85 °C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A	Y	0.8 V		16.3				ns
			1.2 V ± 0.1 V	4.2	6.9	11.7	0.9	15	
			1.5 V ± 0.1 V	3.7	5.2	8.4	1.7	10.7	
			1.8 V ± 0.15 V	3.3	4.4	6.9	1.9	8.5	
			2.5 V ± 0.2 V	2.8	3.5	4.8	1.8	6.1	
			3.3 V ± 0.3 V	2.5	3	4	1.7	4.9	

switching characteristics over recommended operating free-air temperature range, C_L = 10 pF (unless otherwise noted) (see Figures 3 and 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25 °C			T_A = −40 °C TO 85 °C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A	Y	0.8 V		18.4				ns
			1.2 V ± 0.1 V	4.6	7.9	13.4	1.3	16.7	
			1.5 V ± 0.1 V	4	6	9.6	2.2	11.8	
			1.8 V ± 0.15 V	3.6	5	7.9	2.4	9.5	
			2.5 V ± 0.2 V	3.2	4	5.5	2.3	6.8	
			3.3 V ± 0.3 V	2.9	3.5	4.6	2.1	5.6	

switching characteristics over recommended operating free-air temperature range, C_L = 15 pF (unless otherwise noted) (see Figures 3 and 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25 °C			T_A = −40 °C TO 85 °C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A	Y	0.8 V		20.1				ns
			1.2 V ± 0.1 V	5.5	8.7	14	2.5	17.3	
			1.5 V ± 0.1 V	4.7	6.7	10	3	12.5	
			1.8 V ± 0.15 V	4.2	5.6	8.3	3	10.1	
			2.5 V ± 0.2 V	3.6	4.5	5.9	2.7	7.4	
			3.3 V ± 0.3 V	3.3	3.9	5	2.5	6.1	

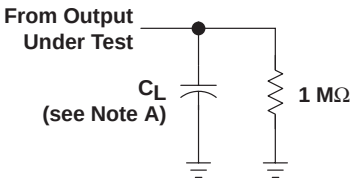
switching characteristics over recommended operating free-air temperature range, C_L = 30 pF (unless otherwise noted) (see Figures 3 and 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25 °C			T_A = −40 °C TO 85 °C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A	Y	0.8 V		25.7				ns
			1.2 V ± 0.1 V	7.4	11.2	17.1	4.5	20.5	
			1.5 V ± 0.1 V	6.1	8.5	12.3	4.6	14.7	
			1.8 V ± 0.15 V	5.4	7.2	10.3	4.1	12	
			2.5 V ± 0.2 V	4.7	5.7	7.4	3.7	8.8	
			3.3 V ± 0.3 V	4.2	5	6.2	3.5	7.3	

operating characteristics, T_A = 25°C

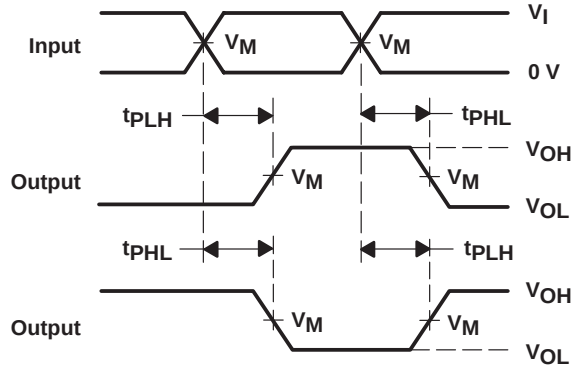
PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	f = 10 MHz	0.8 V	4	pF
			1.2 V ± 0.1 V	4	
			1.5 V ± 0.1 V	4.1	
			1.8 V ± 0.15 V	4.1	
			2.5 V ± 0.2 V	4.3	
			3.3 V ± 0.3 V	4.4	

PARAMETER MEASUREMENT INFORMATION
(Propagation Delays, Setup and Hold Times, and Pulse Width)

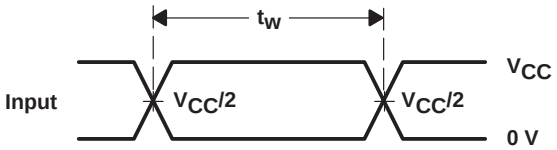


LOAD CIRCUIT

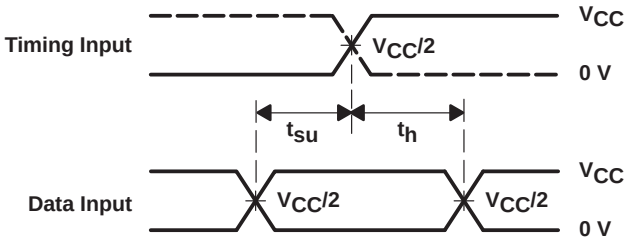
	V_{CC} = 0.8 V	V_{CC} = 1.2 V ± 0.1 V	V_{CC} = 1.5 V ± 0.1 V	V_{CC} = 1.8 V ± 0.15 V	V_{CC} = 2.5 V ± 0.2 V	V_{CC} = 3.3 V ± 0.3 V
C_L	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
V_M	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$
V_I	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
PULSE DURATION

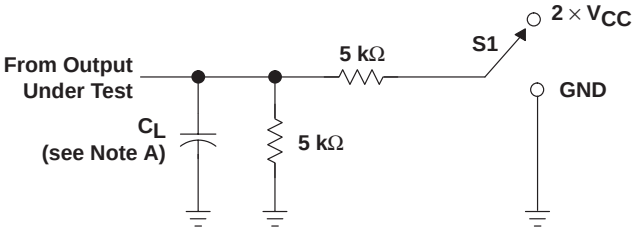


VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f = 3 ns.
C. The outputs are measured one at a time, with one transition per measurement.
D. t_{PLH} and t_{PHL} are the same as t_{pd}.
E. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms

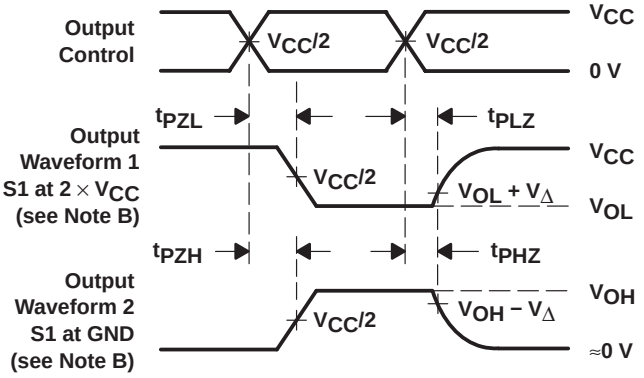
PARAMETER MEASUREMENT INFORMATION
(Enable and Disable Times)



LOAD CIRCUIT

TEST	S1
t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	$2 \times V_{CC}$ GND

	V_{CC} = 0.8 V	V_{CC} = 1.2 V ± 0.1 V	V_{CC} = 1.5 V ± 0.1 V	V_{CC} = 1.8 V ± 0.15 V	V_{CC} = 2.5 V ± 0.2 V	V_{CC} = 3.3 V ± 0.3 V
C_L	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
V_M	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$
V_I	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
V_Δ	0.1 V	0.1 V	0.1 V	0.15 V	0.15 V	0.3 V

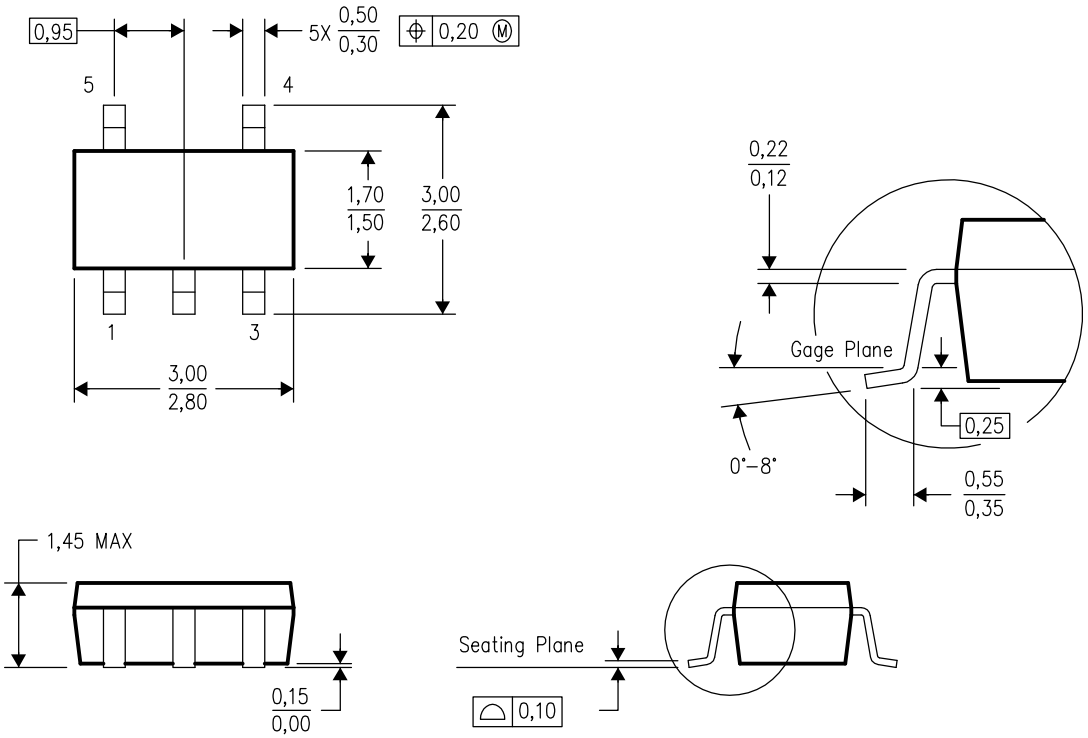


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f = 3 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. All parameters and waveforms are not applicable to all devices.

Figure 4. Load Circuit and Voltage Waveforms

DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



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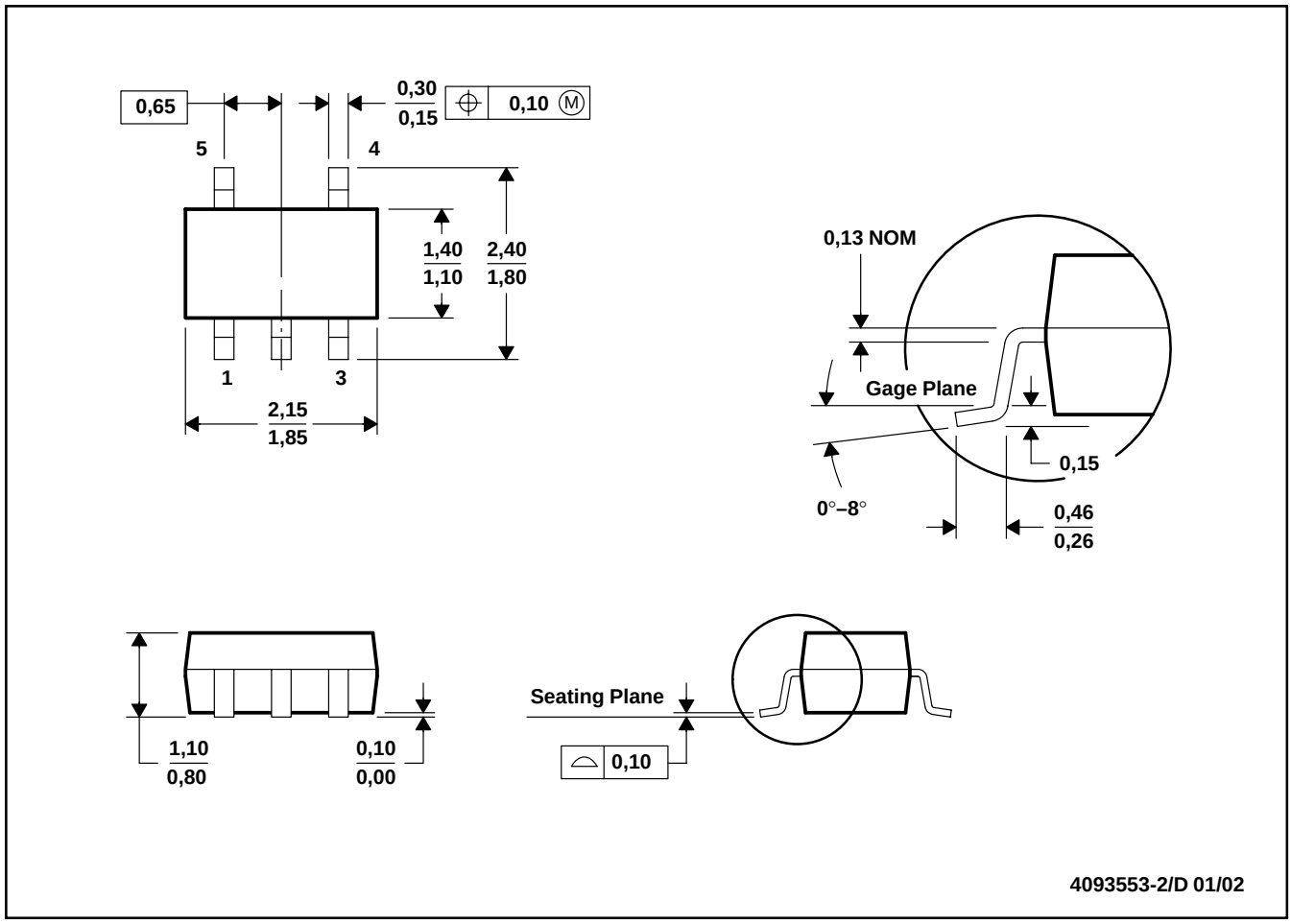
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–178 Variation AA.

DCK (R-PDSO-G5) **PLASTIC SMALL-OUTLINE PACKAGE**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO-203

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