

DATA SHEET

74ALVT16731

2.5V/3.3V 1-to-4 address register/driver
(3-State)

Product specification

1999 Mar 23

IC24 Data Handbook

2.5V/3.3V 1-to-4 address register/driver (3-State)

74ALVT16731

FEATURES

- 5V I/O Compatible
- 3-State outputs
- Output capability: +64 mA/-32 mA
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power-up reset
- Power-up 3-State
- Positive edge triggered registers
- Latch-up protection exceeds 500 mA per JEDEC JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per machine model
- Bus hold data inputs eliminate the need for external pull-up resistors to hold unused inputs

DESCRIPTION

The 74ALVT16731 is a high-performance BiCMOS product designed for V_{CC} operation at 2.5V to 3.3V with I/O compatibility up to 5V.

This device is a 1-to-4 address register/driver featuring non-inverting 3-State outputs. The state of the outputs are controlled by two enable inputs (OE1 and OE2). Each enable input controls the state of two of the four common outputs for each input. When an OEn input is a logic High, the respective outputs will be in the high impedance state. When an OEn input is a logic Low, the respective outputs are active. The device can be configured for a transparent mode from input to output or a register mode by the SEL input. When SEL is a logic High the device is configured for transparent mode and when SEL is a logic Low it is configured for register mode. While in the register mode the output follows the input on the rising edge of the CLK input. The function of the data registers is not effected by either SEL or OEn.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_{amb} = 25^{\circ}\text{C}; \text{GND} = 0\text{V}$	TYPICAL		UNIT
			2.5V	3.3V	
t_{PLH} t_{PHL}	Propagation delay nAx to nYx	$C_L = 50\text{pF}$	3.1 2.3	2.1 1.8	ns
C_{IN}	Input capacitance	$V_I = 0\text{V}$ or V_{CC}	4	4	pF
C_{OUT}	Output capacitance	Outputs disabled; $V_O = 0\text{V}$ or V_{CC}	9	9	pF
I_{CCZ}	Total supply current	Outputs disabled	40	70	μA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
56-Pin Plastic SSOP Type III	-40°C to $+85^{\circ}\text{C}$	74ALVT16731 DL	AV16731 DL	SOT371-1
56-Pin Plastic TSSOP Type II	-40°C to $+85^{\circ}\text{C}$	74ALVT16731 DGG	AV16731 DGG	SOT364-1

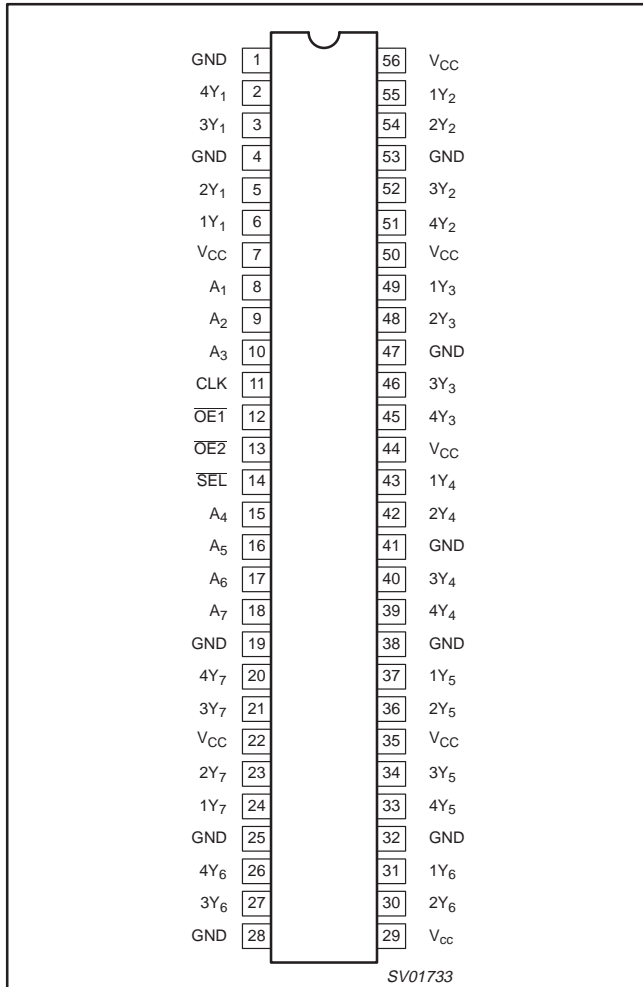
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 4, 19, 25, 28, 32, 38, 41, 47, 53	GND	Ground
5, 6, 23, 24, 30, 31, 36, 37, 42, 43, 48, 49, 54, 55	$1Y_n, 2Y_n$	Output, controlled by OE1
2, 3, 20, 21, 26, 27, 33, 34, 39, 40, 45, 46, 51, 52	$3Y_n, 4Y_n$	Output, controlled by OE2
7, 22, 29, 35, 44, 50, 56	V_{CC}	Positive power supply
8, 9, 10, 15, 16, 17, 18	A_n	Data inputs
14	SEL	Select input, controls mode of device
11	CLK	Clock input
12, 13	OE_n	Output enable

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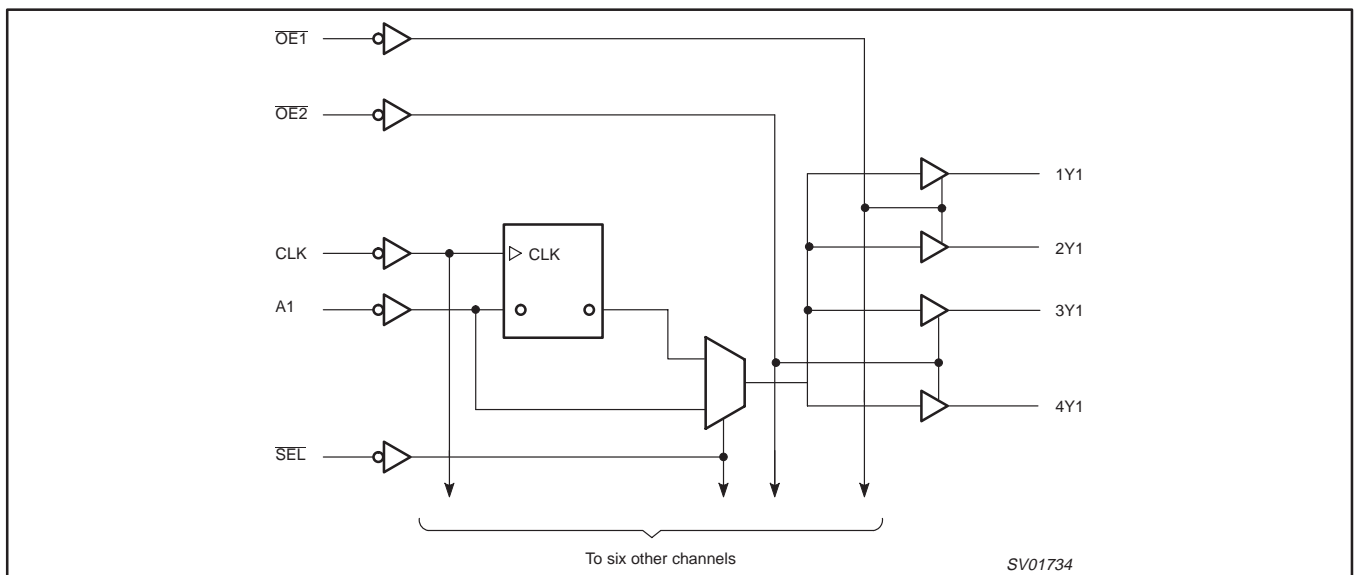
PIN CONFIGURATION



FUNCTION TABLE

INPUTS				OUTPUTS
OE	SEL	CLK	A	Y
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	↑	L	L
L	L	↑	H	H

LOGIC DIAGRAM



2.5V/3.3V 1-to-4 address register/driver (3-State)

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ABSOLUTE MAXIMUM RATINGS^{1, 2}

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V _{CC}	DC supply voltage		-0.5 to +4.6	V
I _{IK}	DC input diode current	V _I < 0	-50	mA
V _I	DC input voltage ³		-0.5 to +7.0	V
I _{OK}	DC output diode current	V _O < 0	-50	mA
V _{OUT}	DC output voltage ³	Output in Off or High state	-0.5 to +7.0	V
I _{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	-64	
T _{stg}	Storage temperature range		-65 to +150	°C

NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
- The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	2.5V RANGE LIMITS		3.3V RANGE LIMITS		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	DC supply voltage	2.3	2.7	3.0	3.6	V
V _I	Input voltage	0	5.5	0	5.5	V
V _{IH}	High-level input voltage	1.7		2.0		V
V _{IL}	Input voltage		0.7		0.8	V
I _{OH}	High-level output current		-8		-32	mA
I _{OL}	Low-level output current		8		32	mA
	Low-level output current; current duty cycle ≤ 50%; f ≥ 1kHz		24		64	
Δt/Δv	Input transition rise or fall rate; Outputs enabled		10		10	ns/V
T _{amb}	Operating free-air temperature range	-40	+85	-40	+85	°C

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DC ELECTRICAL CHARACTERISTICS (3.3V ± 0.3V RANGE)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP ¹	MAX	
V _{IK}	Input clamp voltage	V _{CC} = 3.0V; I _{IK} = -18mA		-0.85	-1.2	V
V _{OH}	High-level output voltage	V _{CC} = 3.0 to 3.6V; I _{OH} = -100μA	V _{CC} -0.2	V _{CC}		V
		V _{CC} = 3.0V; I _{OH} = -32mA	2.0	2.3		
V _{OL}	Low-level output voltage	V _{CC} = 3.0V; I _{OL} = 100μA		0.07	0.2	V
		V _{CC} = 3.0V; I _{OL} = 16mA		0.25	0.4	
		V _{CC} = 3.0V; I _{OL} = 32mA		0.3	0.5	
		V _{CC} = 3.0V; I _{OL} = 64mA		0.4	0.55	
V _{RST}	Power-up output low voltage ⁶	V _{CC} = 3.6V; I _O = 1mA; V _I = V _{CC} or GND			0.55	V
I _I	Input leakage current	V _{CC} = 3.6V; V _I = V _{CC} or GND	Control pins	0.1	±1	μA
		V _{CC} = 0 or 3.6V; V _I = 5.5V		0.1	10	
		V _{CC} = 3.6V; V _I = V _{CC}	Data pins ⁴	0.5	1	
		V _{CC} = 3.6V; V _I = 0		0.1	-5	
I _{OFF}	Off current	V _{CC} = 0V; V _I or V _O = 0 to 4.5V		0.1	±100	μA
I _{HOLD}	Bus Hold current Data inputs ⁷	V _{CC} = 3V; V _I = 0.8V		75	130	μA
		V _{CC} = 3V; V _I = 2.0V		-75	-225	
		V _{CC} = 0V to 3.6V; V _{CC} = 3.6V		±500		
I _{EX}	Current into an output in the High state when V _O > V _{CC}	V _O = 5.5V; V _{CC} = 3.0V		10	125	μA
I _{PU/PD}	Power up/down 3-State output current ³	V _{CC} ≤ 1.2V; V _O = 0.5V to V _{CC} ; V _I = GND or V _{CC} OE/OE = Don't care		1	±100	μA
I _{OZH}	3-State output High current	V _{CC} = 3.6V; V _O = 3.0V; V _I = V _{IL} or V _{IH}		0.5	5	μA
I _{OZL}	3-State output Low current	V _{CC} = 3.6V; V _O = 0.5V; V _I = V _{IL} or V _{IH}		0.5	-5	μA
I _{CCH}	Quiescent supply current	V _{CC} = 3.6V; Outputs High, V _I = GND or V _{CC} , I _O = 0		0.05	0.1	mA
I _{CCL}		V _{CC} = 3.6V; Outputs Low, V _I = GND or V _{CC} , I _O = 0		7.0	9.0	
I _{CCZ}		V _{CC} = 3.6V; Outputs Disabled; V _I = GND or V _{CC} , I _O = 0 ⁵		0.06	0.1	
ΔI _{CC}	Additional supply current per input pin ²	V _{CC} = 3V to 3.6V; One input at V _{CC} -0.6V, Other inputs at V _{CC} or GND		0.04	0.4	mA

NOTES:

- All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
- This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
- This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 0.3V a transition time of 100μsec is permitted. This parameter is valid for T_{amb} = 25°C only.
- Unused pins at V_{CC} or GND.
- I_{CCZ} is measured with outputs pulled up to V_{CC} or pulled down to ground.
- For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.
- This is the bus hold overdrive current required to force the input to the opposite logic state.

2.5V/3.3V 1-to-4 address register/driver (3-State)

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AC CHARACTERISTICS (3.3V ± 0.3V RANGE)GND = 0V; $t_R = t_F = 2.5\text{ns}$; $C_L = 50\text{pF}$; $R_L = 500\Omega$; $T_{\text{amb}} = -40^\circ\text{C}$ to $+85^\circ\text{C}$.

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			$V_{CC} = 3.3V \pm 0.3V$			
			MIN	TYP ¹	MAX	
t_{PLH} t_{PHL}	Propagation delay nAx to nYx	1	1.0 1.0	2.1 1.8	4.0 3.4	ns
t_{PLH} t_{PHL}	Propagation delay CLK to nYx	3	1.5 1.5	2.8 2.7	4.7 4.4	ns
t_{PLH} t_{PHL}	Propagation delay SEL to nYx	1	1.5 1.0	3.5 2.7	5.4 4.4	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.0 1.0	3.3 2.3	5.2 4.1	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low Level	2	1.5 1.5	3.7 3.0	5.6 4.5	ns

NOTE:1. All typical values are at $V_{CC} = 3.3V$ and $T_{\text{amb}} = 25^\circ\text{C}$.**AC SETUP REQUIREMENTS (3.3V ± 0.3V RANGE)**GND = 0V; $t_R = t_F = 2.5\text{ns}$; $C_L = 50\text{pF}$; $R_L = 500\Omega$; $T_{\text{amb}} = -40^\circ\text{C}$ to $+85^\circ\text{C}$.

SYMBOL	PARAMETER	WAVEFORM	LIMITS		UNIT
			$V_{CC} = 3.3V \pm 0.3V$		
			MIN	TYP ¹	
$t_{s(H)}$ $t_{s(L)}$	Setup time, High or Low Ax to CLK	4	1.5 1.5	1.0 1.0	ns
$t_{h(H)}$ $t_{h(L)}$	Hold time, High or Low Ax to CLK	4	0 0	-0.9 -0.9	ns
$t_{w(H)}$ $t_{w(L)}$	Pulse width, High or Low CLK	3	1.5 1.5		ns

NOTE:1. All typical values are at $V_{CC} = 3.3V$ and $T_{\text{amb}} = 25^\circ\text{C}$.

2.5V/3.3V 1-to-4 address register/driver (3-State)

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DC ELECTRICAL CHARACTERISTICS (2.5V ± 0.2V RANGE)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP ¹	MAX	
V _{IK}	Input clamp voltage	V _{CC} = 2.3V; I _{IK} = -18mA		-0.85	-1.2	V
V _{OH}	High-level output voltage	V _{CC} = 2.3 to 3.6V; I _{OH} = -100µA	V _{CC} -0.2	V _{CC}		V
		V _{CC} = 2.3V; I _{OH} = -8mA	1.8	2.1		
V _{OL}	Low-level output voltage	V _{CC} = 2.3V; I _{OL} = 100µA		0.07	0.2	V
		V _{CC} = 2.3V; I _{OL} = 24mA		0.3	0.5	
		V _{CC} = 2.3V; I _{OL} = 8mA			0.4	
V _{RST}	Power-up output low voltage ⁷	V _{CC} = 2.7V; I _O = 1mA; V _I = V _{CC} or GND			0.55	V
I _I	Input leakage current	V _{CC} = 2.7V; V _I = V _{CC} or GND	Control pins	0.1	±1	µA
		V _{CC} = 0 or 2.7V; V _I = 5.5V		0.1	10	
		V _{CC} = 2.7V; V _I = V _{CC}	Data pins ⁴	0.1	10	
		V _{CC} = 2.7V; V _I = 0		0.1	-5	
I _{OFF}	Off current	V _{CC} = 0V; V _I or V _O = 0 to 4.5V		0.1	±100	µA
I _{HOLD}	Bus Hold current Data inputs ⁶	V _{CC} = 2.3V; V _I = 0.7V		90		µA
		V _{CC} = 2.3V; V _I = 1.7V		-10		µA
I _{EX}	Current into an output in the High state when V _O > V _{CC}	V _O = 5.5V; V _{CC} = 2.3V		10	125	µA
I _{PU/PD}	Power up/down 3-State output current ³	V _{CC} ≤ 1.2V; V _O = 0.5V to V _{CC} ; V _I = GND or V _{CC} OE/OE = Don't care		1	±100	µA
I _{OZH}	3-State output High current	V _{CC} = 2.7V; V _O = 2.3V; V _I = V _{IL} or V _{IH}		0.5	5	µA
I _{OZL}	3-State output Low current	V _{CC} = 2.7V; V _O = 0.5V; V _I = V _{IL} or V _{IH}		0.5	-5	µA
I _{CCH}	Quiescent supply current	V _{CC} = 2.7V; Outputs High, V _I = GND or V _{CC} , I _O = 0		0.04	0.1	mA
I _{CCL}		V _{CC} = 2.7V; Outputs Low, V _I = GND or V _{CC} , I _O = 0		5.0	7.0	
I _{CCZ}		V _{CC} = 2.7V; Outputs Disabled; V _I = GND or V _{CC} , I _O = 0 ⁵		0.04	0.1	
ΔI _{CC}	Additional supply current per input pin ²	V _{CC} = 2.3V to 2.7V; One input at V _{CC} -0.6V, Other inputs at V _{CC} or GND		0.04	0.4	mA

NOTES:

- All typical values are at V_{CC} = 2.5V and T_{amb} = 25°C.
- This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
- This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 2.5V ± 0.2V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
- Unused pins at V_{CC} or GND.
- I_{CCZ} is measured with outputs pulled up to V_{CC} or pulled down to ground.
- Not guaranteed.
- For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.

AC CHARACTERISTICS (2.5V ± 0.2V RANGE)

GND = 0V; t_R = t_F = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = -40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			V _{CC} = 2.5V ± 0.2V			
			MIN	TYP ¹	MAX	
t _{PLH} t _{PHL}	Propagation delay nAx to nYx	1	1.0 1.0	3.1 2.3	5.5 4.2	ns
t _{PLH} t _{PHL}	Propagation delay CLK to nYx	3	2.2 2.2	4.0 3.5	6.6 6.0	ns
t _{PLH} t _{PHL}	Propagation delay SEL to nYx	1	1.5 1.0	4.8 3.3	7.9 6.1	ns
t _{PZH} t _{PZL}	Output enable time to High and Low level	2	2.0 2.0	4.7 3.2	7.7 5.6	ns
t _{PHZ} t _{PLZ}	Output disable time from High and Low Level	2	1.5 1.5	4.5 3.7	6.9 5.9	ns

NOTE:

2.5V/3.3V 1-to-4 address register/driver (3-State)

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1. All typical values are at $V_{CC} = 2.5V$ and $T_{amb} = 25^{\circ}C$.

AC SETUP REQUIREMENTS (2.5V ± 0.2V RANGE)

$GND = 0V$; $t_R = t_F = 2.5ns$; $C_L = 50pF$, $R_L = 500\Omega$; $T_{amb} = -40^{\circ}C$ to $+85^{\circ}C$.

SYMBOL	PARAMETER	WAVEFORM	LIMITS		UNIT
			$V_{CC} = 2.5V \pm 0.2V$		
			MIN	TYP ¹	
$t_{s(H)}$ $t_{s(L)}$	Setup time, High or Low Ax to CLK	4	2.4 2.3	0.9 0.8	ns
$t_{h(H)}$ $t_{h(L)}$	Hold time, High or Low Ax to CLK	4	0 0	-0.7 -0.6	ns
$t_{w(H)}$ $t_{w(L)}$	Pulse width, High or Low CLK	3	1.5 1.5		ns

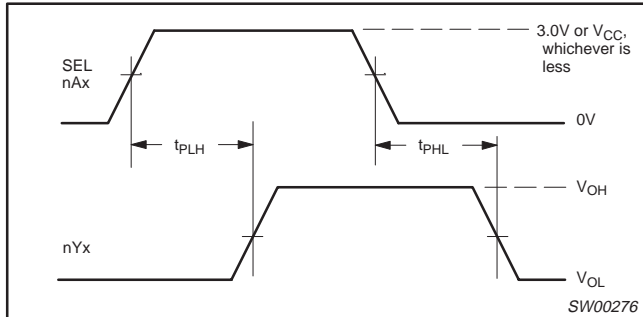
NOTE:

1. All typical values are at $V_{CC} = 2.5V$ and $T_{amb} = 25^{\circ}C$.

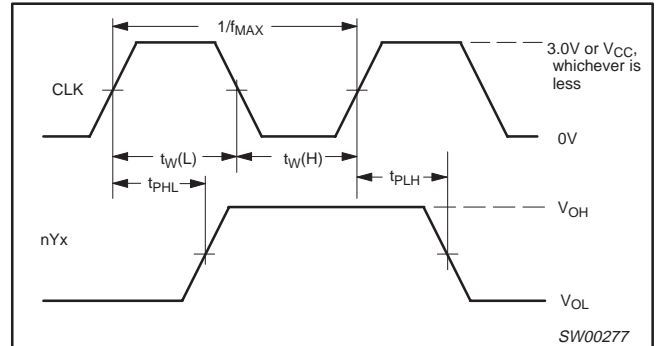
AC WAVEFORMS

NOTES:

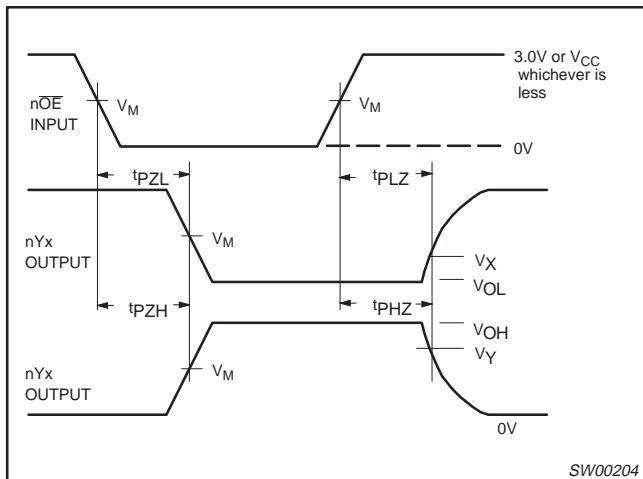
- $V_M = 1.5V$ at $V_{CC} \geq 3.0V$, $V_M = V_{CC}/2$ at $V_{CC} \leq 2.7V$
- $V_X = V_{OL} + 0.3V$ at $V_{CC} \geq 3.0V$, $V_X = V_{OL} + 0.150V$ at $V_{CC} \leq 2.7V$
- $V_Y = V_{OH} - 0.3V$ at $V_{CC} \geq 3.0V$, $V_Y = V_{OH} - 0.150V$ at $V_{CC} \leq 2.7V$



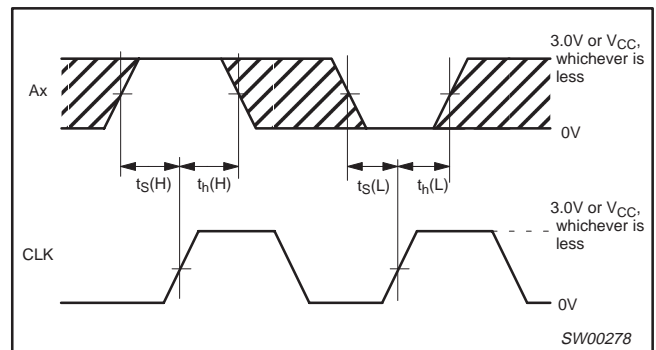
Waveform 1. Input (Ax) to Output (nYx) Propagation Delay, transparent mode. SEL to Output (nYx) Propagation Delay



Waveform 3. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



Waveform 2. 3-State Output Enable and Disable Times

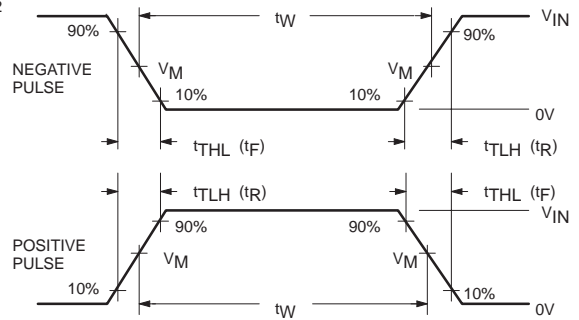
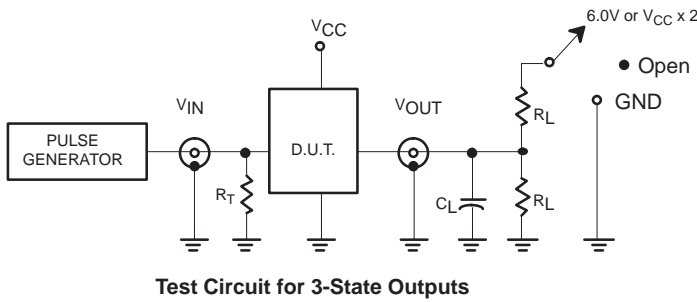


Waveform 4. Data Setup and Hold Times

2.5V/3.3V 1-to-4 address register/driver (3-State)

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TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs

SWITCH POSITION

TEST	SWITCH
t_{PLZ}/t_{PZL}	6V or $V_{CC} \times 2$
t_{PLH}/t_{PHL}	Open
t_{PHZ}/t_{PZH}	GND

DEFINITIONS

- R_L = Load resistor; see AC CHARACTERISTICS for value.
- C_L = Load capacitance includes jig and probe capacitance: See AC CHARACTERISTICS for value.
- R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

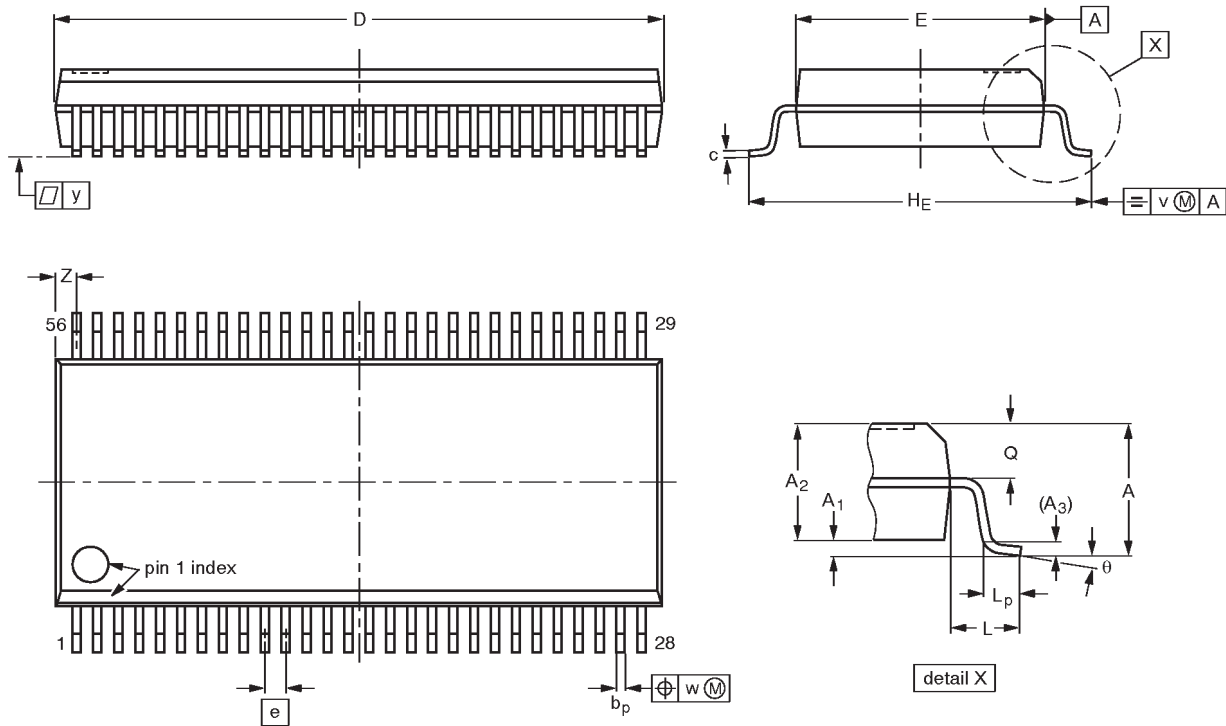
FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ALVT16	3.0V or V_{CC} whichever is less	$\leq 10\text{MHz}$	500ns	$\leq 2.5\text{ns}$	$\leq 2.5\text{ns}$

2.5 V/3.3 V 1-to-4 address register/driver (3-State)

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SSOP56: plastic shrink small outline package; 56 leads; body width 7.5 mm

SOT371-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	2.8	0.4 0.2	2.35 2.20	0.25	0.3 0.2	0.22 0.13	18.55 18.30	7.6 7.4	0.635	10.4 10.1	1.4	1.0 0.6	1.2 1.0	0.25	0.18	0.1	0.85 0.40	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

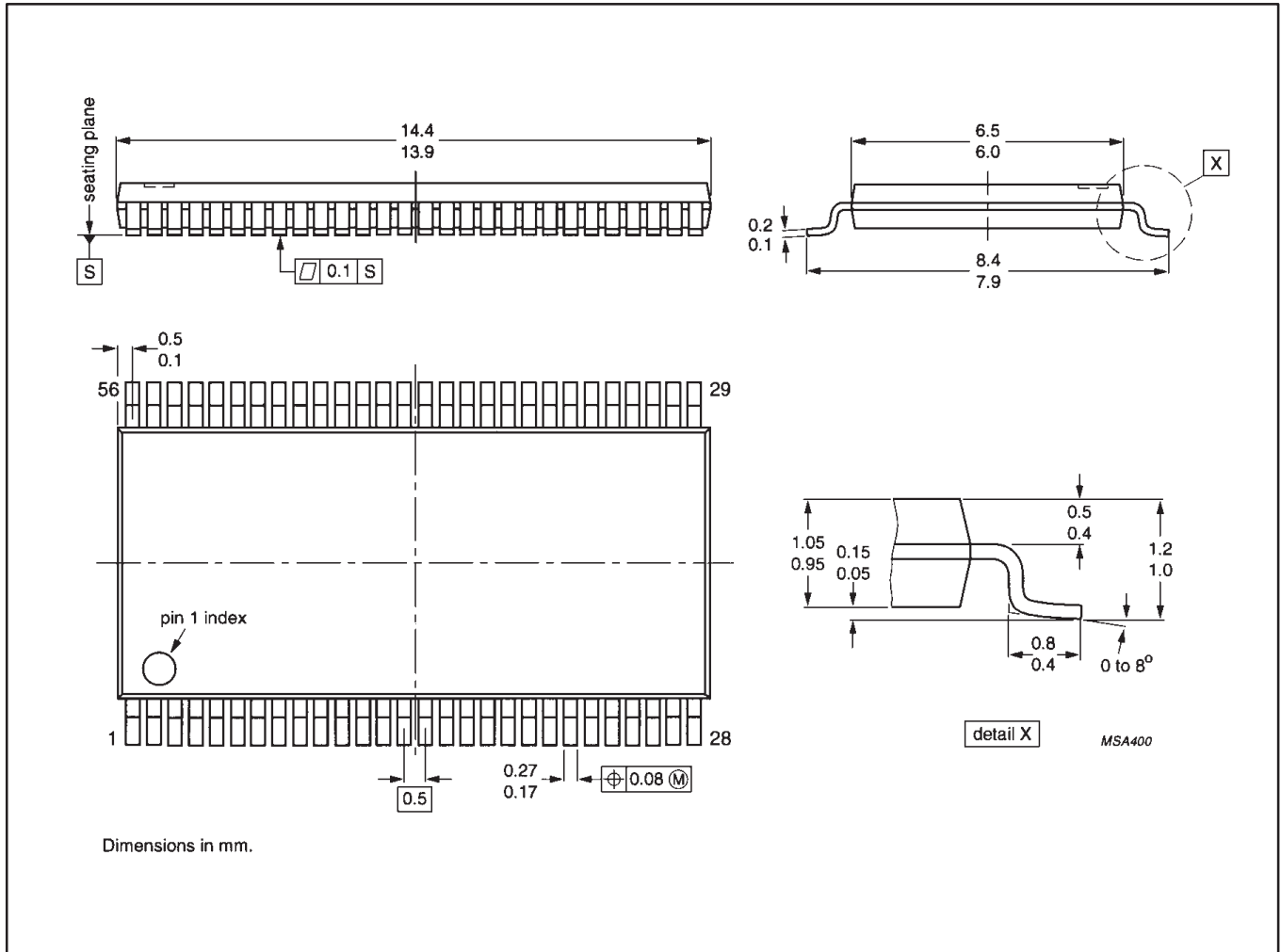
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT371-1		MO-118AB				93-11-02 95-02-04

2.5 V/3.3 V 1-to-4 address register/driver (3-State)

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TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1mm

SOT364-1



2.5V/3.3V 1-to-4 address register/driver (3-State)

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DEFINITIONS

Data Sheet Identification	Product Status	Definition
<i>Objective Specification</i>	Formative or in Design	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
<i>Preliminary Specification</i>	Preproduction Product	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
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