

DATA SHEET

74ALVT16841

2.5V/3.3V ALVT 20-bit bus interface latch
(3-State)

Product specification
Supersedes data of 1996 Aug 28
IC23 Data Handbook

1998 Feb 13

2.5V/3.3V 20-bit bus interface latch (3-State)

74ALVT16841

FEATURES

- High speed parallel latches
- 5V I/O Compatible
- Live insertion/extraction permitted
- Extra data width for wide address/data paths or buses carrying parity
- Power-up 3-State
- Power-up reset
- Ideal where high speed, light loading, or increased fan-in are required with MOS microprocessors
- Output capability: +64mA/−32mA
- Latch-up protection exceeds 500mA per Jedec Std 17
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The 74ALVT16841 Bus interface latch is designed to provide extra data width for wider data/address paths of buses carrying parity. It is designed for V_{CC} operation at 2.5V or 3.3V with I/O compatibility to 5V.

The 74ALVT16841 consists of two sets of ten D-type latches with 3-State outputs. The flip-flops appear transparent to the data when Latch Enable (nLE) is High. This allows asynchronous operation, as the output transition follows the data in transition. On the nLE High-to-Low transition, the data that meets the setup and hold time is latched.

Data appears on the bus when the Output Enable (nOE) is Low. When nOE is High the output is in the High-impedance state.

QUICK REFERENCE DATA

| SYMBOL | PARAMETER | CONDITIONS $T_{amb} = 25^{\circ}C$ | TYPICAL | | UNIT |
|------------------------|--|---------------------------------------|------------|------------|---------|
| | | | 2.5V | 3.3V | |
| t_{PLH} t_{PHL} | Propagation delay nDx to nQx | $C_L = 50pF$ | 1.8 2.1 | 1.5 1.7 | ns |
| C_{IN} | Input capacitance DIR, \overline{OE} | $V_I = 0V$ or V_{CC} | 3 | 3 | pF |
| C_{Out} | Output pin capacitance | $V_{I/O} = 0V$ or V_{CC} | 9 | 9 | pF |
| I_{CCZ} | Total supply current | Outputs disabled | 40 | 70 | μA |

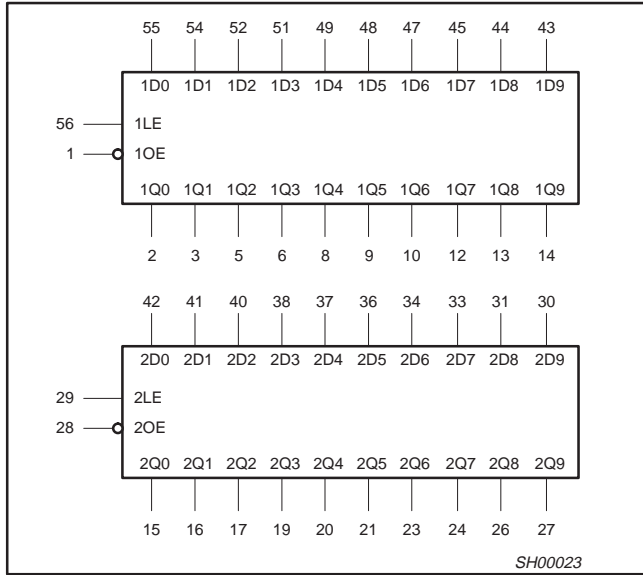
ORDERING INFORMATION

| PACKAGES | TEMPERATURE RANGE | OUTSIDE NORTH AMERICA | NORTH AMERICA | DWG NUMBER |
|------------------------------|-------------------|-----------------------|---------------|------------|
| 56-Pin Plastic SSOP Type III | −40°C to +85°C | 74ALVT16841 DL | AV16841 DL | SOT371-1 |
| 56-Pin Plastic TSSOP Type II | −40°C to +85°C | 74ALVT16841 DGG | AV16841 DGG | SOT364-1 |

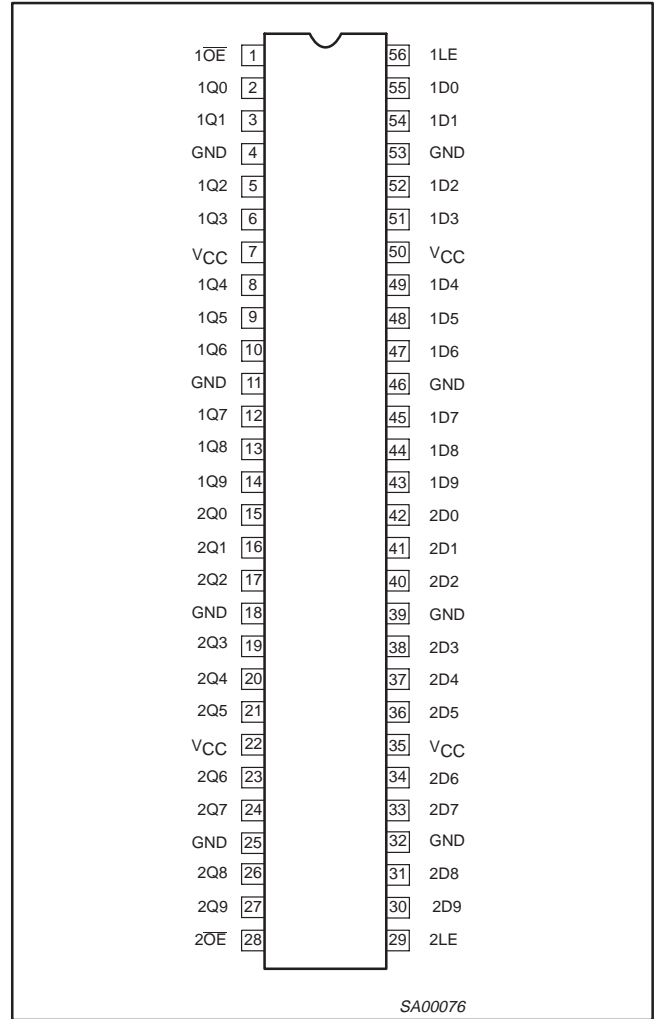
2.5V/3.3V 20-bit bus interface latch (3-State)

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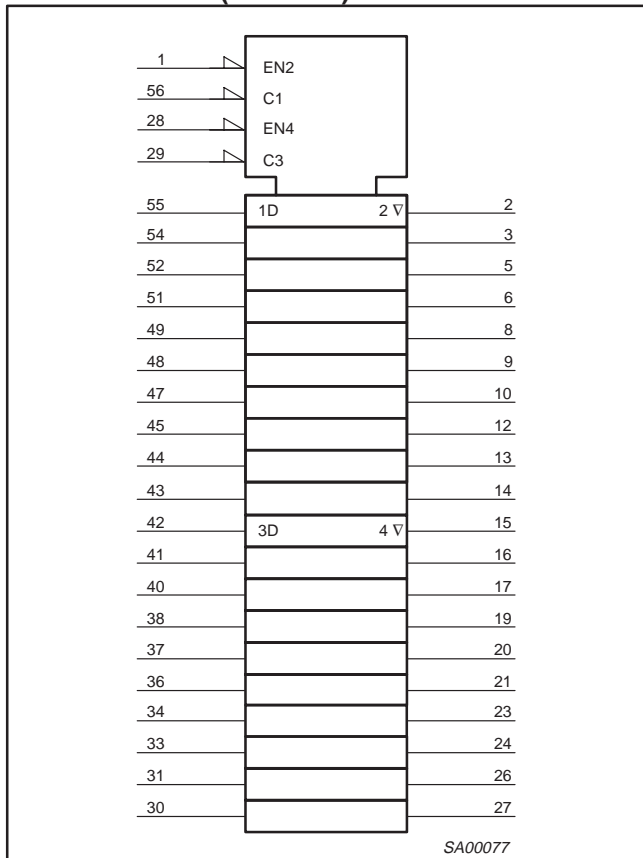
LOGIC SYMBOL



PIN CONFIGURATION



LOGIC SYMBOL (IEEE/IEC)



2.5V/3.3V 20-bit bus interface latch (3-State)

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PIN DESCRIPTION

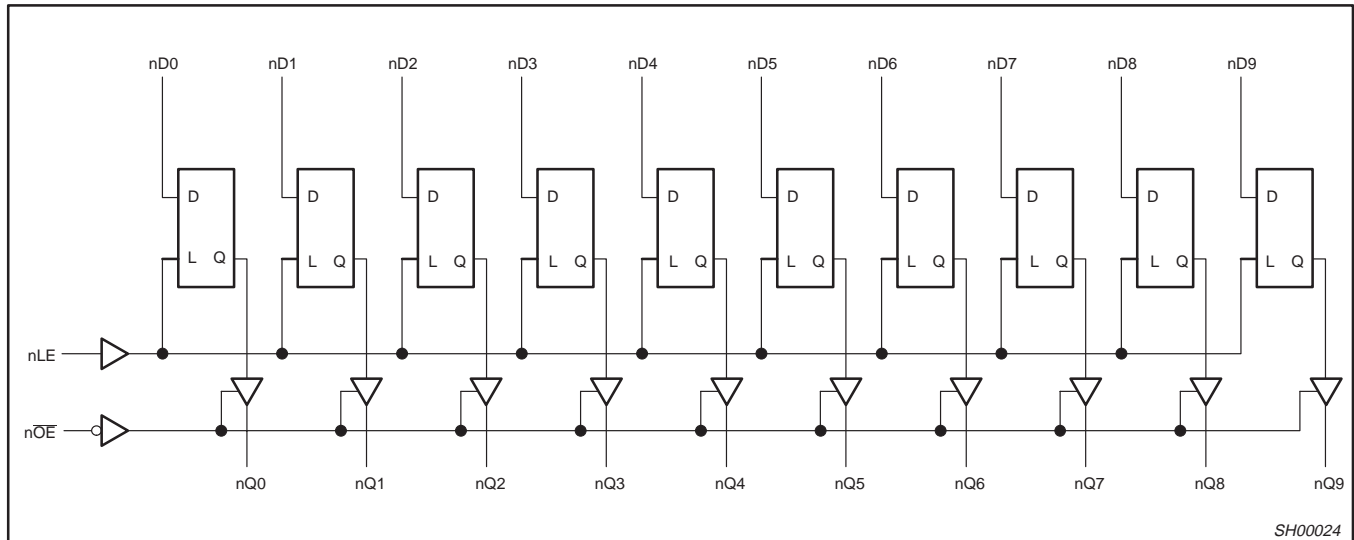
| PIN NUMBER | SYMBOL | FUNCTION |
|--|------------------------|--|
| 55, 54, 52, 51, 49, 48, 47, 45, 44, 43, 42, 41, 40, 38, 37, 36, 34, 33, 31, 30 | 1D0 – 1D9 2D0 – 2D9 | Data inputs |
| 2, 3, 5, 6, 8, 9, 10, 12, 13, 14, 15, 16, 17, 19, 20, 21, 23, 24, 26, 27 | 1Q0 – 1Q9 2Q0 – 2Q9 | Data outputs |
| 1, 28 | 1OE, 2OE | Output enable inputs (active-Low) |
| 56, 29 | 1LE, 2LE | Latch enable inputs (active rising edge) |
| 4, 11, 18, 25, 32, 39, 46, 53 | GND | Ground (0V) |
| 7, 22, 35, 50 | V _{CC} | Positive supply voltage |

FUNCTION TABLE

| INPUTS | | | OUTPUTS | OPERATING MODE |
|--------|-----|-----|-----------|----------------|
| nOE | nLE | nDx | nQ0 – nQ9 | |
| L | H | L | L | Transparent |
| L | H | H | H | |
| L | ↓ | l | L | Latched |
| L | ↓ | h | H | |
| H | X | X | Z | High impedance |
| L | L | X | NC | Hold |

H = High voltage level
 h = High voltage level one set-up time prior to the High-to-Low LE transition
 L = Low voltage level
 l = Low voltage level one set-up time prior to the High-to-Low LE transition
 ↓ = High-to-Low LE transition
 NC = No change
 X = Don't care
 Z = High impedance "off" state

LOGIC DIAGRAM



2.5V/3.3V 20-bit bus interface latch (3-State)

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ABSOLUTE MAXIMUM RATINGS^{1, 2}

| SYMBOL | PARAMETER | CONDITIONS | RATING | UNIT |
|-----------|--------------------------------|-----------------------------|--------------|------|
| V_{CC} | DC supply voltage | | -0.5 to +4.6 | V |
| I_{IK} | DC input diode current | $V_I < 0$ | -50 | mA |
| V_I | DC input voltage ³ | | -1.2 to +7.0 | V |
| I_{OK} | DC output diode current | $V_O < 0$ | -50 | mA |
| V_{OUT} | DC output voltage ³ | Output in Off or High state | -0.5 to +7.0 | V |
| I_{OUT} | DC output current | Output in Low state | 128 | mA |
| | | Output in High state | -64 | |
| T_{stg} | Storage temperature range | | -65 to 150 | °C |

NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | 2.5V RANGE LIMITS | | 3.3V RANGE LIMITS | | UNIT |
|---------------------|---|-------------------|-----|-------------------|-----|------|
| | | MIN | MAX | MIN | MAX | |
| V_{CC} | DC supply voltage | 2.3 | 2.7 | 3.0 | 3.6 | V |
| V_I | Input voltage | 0 | 5.5 | 0 | 5.5 | V |
| V_{IH} | High-level input voltage | 1.7 | | 2.0 | | V |
| V_{IL} | Input voltage | | 0.7 | | 0.8 | V |
| I_{OH} | High-level output current | | -8 | | -32 | mA |
| I_{OL} | Low-level output current | | 8 | | 32 | mA |
| | Low-level output current; current duty cycle $\leq 50\%$; $f \geq 1$ kHz | | 24 | | 64 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate; Outputs enabled | | 10 | | 10 | ns/V |
| T_{amb} | Operating free-air temperature range | -40 | +85 | -40 | +85 | °C |

2.5V/3.3V 20-bit bus interface latch (3-State)

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DC ELECTRICAL CHARACTERISTICS (3.3V ± 0.3V RANGE)

| SYMBOL | PARAMETER | TEST CONDITIONS | LIMITS | | | UNIT |
|--------------------|--|--|------------------------|------------------|------|------|
| | | | Temp = -40°C to +85°C | | | |
| | | | MIN | TYP ¹ | MAX | |
| V _{IK} | Input clamp voltage | V _{CC} = 3.0V; I _{IK} = -18mA | | -0.85 | -1.2 | V |
| V _{OH} | High-level output voltage | V _{CC} = 3.0 to 3.6V; I _{OH} = -100μA | V _{CC} -0.2 | V _{CC} | | V |
| | | V _{CC} = 3.0V; I _{OH} = -32mA | 2.0 | 2.3 | | |
| V _{OL} | Low-level output voltage | V _{CC} = 3.0V; I _{OL} = 100μA | | 0.07 | 0.2 | V |
| | | V _{CC} = 3.0V; I _{OL} = 16mA | | 0.25 | 0.4 | |
| | | V _{CC} = 3.0V; I _{OL} = 32mA | | 0.3 | 0.5 | |
| | | V _{CC} = 3.0V; I _{OL} = 64mA | | 0.4 | 0.55 | |
| V _{RST} | Power-up output low voltage ⁶ | V _{CC} = 3.6V; I _O = 1mA; V _I = V _{CC} or GND | | | 0.55 | V |
| I _I | Input leakage current | V _{CC} = 3.6V; V _I = V _{CC} or GND | Control pins | 0.1 | ±1 | μA |
| | | V _{CC} = 0 or 3.6V; V _I = 5.5V | | 0.1 | 10 | |
| | | V _{CC} = 3.6V; V _I = V _{CC} | Data pins ⁴ | 0.5 | 1 | |
| | | V _{CC} = 3.6V; V _I = 0V | | 0.1 | -5 | |
| I _{OFF} | Off current | V _{CC} = 0V; V _I or V _O = 0 to 4.5V | | 0.1 | ±100 | μA |
| I _{HOLD} | Bus Hold current Data inputs ⁷ | V _{CC} = 3V; V _I = 0.8V | | 75 | 130 | μA |
| | | V _{CC} = 3V; V _I = 2.0V | | -75 | -140 | |
| | | V _{CC} = 0V to 3.6V; V _{CC} = 3.6V | | ±500 | | |
| I _{EX} | Current into an output in the High state when V _O > V _{CC} | V _O = 5.5V; V _{CC} = 3.0V | | 10 | 125 | μA |
| I _{PU/PD} | Power up/down 3-State output current ³ | V _{CC} ≤ 1.2V; V _O = 0.5V to V _{CC} ; V _I = GND or V _{CC} OE/OE = Don't care | | 1 | ±100 | μA |
| I _{OZH} | 3-State output High current | V _{CC} = 3.6V; V _O = 3.0V; V _I = V _{IL} or V _{IH} | | 0.5 | 5 | μA |
| I _{OZL} | 3-State output Low current | V _{CC} = 3.6V; V _O = 0.5V; V _I = V _{IL} or V _{IH} | | 0.5 | -5 | μA |
| I _{CCH} | Quiescent supply current | V _{CC} = 3.6V; Outputs High, V _I = GND or V _{CC} , I _O = 0 | | 0.07 | 0.1 | mA |
| I _{CCL} | | V _{CC} = 3.6V; Outputs Low, V _I = GND or V _{CC} , I _O = 0 | | 3.2 | 7 | |
| I _{CCZ} | | V _{CC} = 3.6V; Outputs Disabled; V _I = GND or V _{CC} , I _O = 0 ⁵ | | 0.07 | 0.1 | |
| ΔI _{CC} | Additional supply current per input pin ² | V _{CC} = 3V to 3.6V; One input at V _{CC} -0.6V, Other inputs at V _{CC} or GND | | 0.04 | 0.4 | mA |

NOTES:

- All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
- This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND.
- This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 0.3V a transition time of 100μsec is permitted. This parameter is valid for T_{amb} = 25°C only.
- Unused pins at V_{CC} or GND.
- I_{CCZ} is measured with outputs pulled up to V_{CC} or pulled down to ground.
- For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.
- This is the bus hold overdrive current required to force the input to the opposite logic state.

2.5V/3.3V 20-bit bus interface latch (3-State)

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AC CHARACTERISTICS (3.3V ± 0.3V RANGE)GND = 0V; $t_R = t_F = 2.5\text{ns}$; $C_L = 50\text{pF}$; $R_L = 500\Omega$; $T_{\text{amb}} = -40^\circ\text{C}$ to $+85^\circ\text{C}$.

| SYMBOL | PARAMETER | WAVEFORM | LIMITS | | | UNIT |
|--------------------------------------|--|----------|---|------------|------------|------|
| | | | $T_{\text{amb}} = -40$ to $+85^\circ\text{C}$ $V_{\text{CC}} = +3.3\text{V} \pm 0.3\text{V}$ | | | |
| | | | MIN | TYP | MAX | |
| t_{PLH} t_{PHL} | Propagation delay nDx to nQx | 2 | 0.5 0.5 | 1.5 1.7 | 2.5 2.7 | ns |
| t_{PLH} t_{PHL} | Propagation delay nLE to nQx | 1 | 1.0 1.5 | 2.1 3.4 | 3.2 5.5 | ns |
| t_{PZH} t_{PZL} | Output enable time to High and Low level | 4 5 | 1.0 0.5 | 2.3 1.3 | 3.6 2.3 | ns |
| t_{PHZ} t_{PLZ} | Output disable time from High and Low level | 4 5 | 1.5 1.5 | 3.2 2.8 | 4.9 4.3 | ns |

NOTE:1. All typical values are at $V_{\text{CC}} = 3.3\text{V}$ and $T_{\text{amb}} = 25^\circ\text{C}$.**AC SETUP REQUIREMENTS (3.3V ± 0.3V RANGE)**GND = 0V, $t_R = t_F = 2.5\text{ns}$, $C_L = 50\text{pF}$, $R_L = 500\Omega$

| SYMBOL | PARAMETER | WAVEFORM | LIMITS | | UNIT |
|------------------------------------|---------------------------------------|----------|---|------------|------|
| | | | $T_{\text{amb}} = -40$ to $+85^\circ\text{C}$ $V_{\text{CC}} = +3.3\text{V} \pm 0.3\text{V}$ | | |
| | | | Min | Typ | |
| $t_s(\text{H})$ $t_s(\text{L})$ | Setup time, High or Low nDx to nLE | 3 | 1.0 1.0 | 0 0 | ns |
| $t_h(\text{H})$ $t_h(\text{L})$ | Hold time, High or Low nDx to nLE | 3 | 1.2 1.2 | 0.1 0.3 | ns |
| $t_w(\text{H})$ | nLE pulse width High | 1 | 1.5 | | ns |

2.5V/3.3V 20-bit bus interface latch (3-State)

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DC ELECTRICAL CHARACTERISTICS (2.5V ± 0.2V RANGE)

| SYMBOL | PARAMETER | TEST CONDITIONS | LIMITS | | | UNIT |
|--------------------|--|---|------------------------|------------------|------|------|
| | | | Temp = -40°C to +85°C | | | |
| | | | MIN | TYP ¹ | MAX | |
| V _{IK} | Input clamp voltage | V _{CC} = 2.3V; I _{IK} = -18mA | | -0.85 | -1.2 | V |
| V _{OH} | High-level output voltage | V _{CC} = 2.3 to 3.6V; I _{OH} = -100µA | V _{CC} -0.2 | V _{CC} | | V |
| | | V _{CC} = 2.3V; I _{OH} = -8mA | 1.8 | 2.1 | | |
| V _{OL} | Low-level output voltage | V _{CC} = 2.3V; I _{OL} = 100µA | | 0.07 | 0.2 | V |
| | | V _{CC} = 2.3V; I _{OL} = 24mA | | 0.3 | 0.5 | |
| | | V _{CC} = 2.3V; I _{OL} = 8mA | | | 0.4 | |
| V _{RST} | Power-up output low voltage ⁷ | V _{CC} = 2.7V; I _O = 1mA; V _I = V _{CC} or GND | | | 0.55 | V |
| I _I | Input leakage current | V _{CC} = 2.7V; V _I = V _{CC} or GND | Control pins | 0.1 | ±1 | µA |
| | | V _{CC} = 0 or 2.7V; V _I = 5.5V | | 0.1 | 10 | |
| | | V _{CC} = 2.7V; V _I = V _{CC} | Data pins ⁴ | 0.1 | 1 | |
| | | V _{CC} = 2.7V; V _I = 0 | | 0.1 | -5 | |
| I _{OFF} | Off current | V _{CC} = 0V; V _I or V _O = 0 to 4.5V | | 0.1 | ±100 | µA |
| I _{HOLD} | Bus Hold current Data inputs ⁶ | V _{CC} = 2.3V; V _I = 0.7V | | 90 | | µA |
| | | V _{CC} = 2.3V; V _I = 1.7V | | -10 | | |
| I _{EX} | Current into an output in the High state when V _O > V _{CC} | V _O = 5.5V; V _{CC} = 2.3V | | 10 | 125 | µA |
| I _{PU/PD} | Power up/down 3-State output current ³ | V _{CC} ≤ 1.2V; V _O = 0.5V to V _{CC} ; V _I = GND or V _{CC} ; OE/OE = Don't care | | 1 | ±100 | µA |
| I _{OZH} | 3-State output High current | V _{CC} = 2.7V; V _O = 2.3V; V _I = V _{IL} or V _{IH} | | 0.5 | 5 | µA |
| I _{OZL} | 3-State output Low current | V _{CC} = 2.7V; V _O = 0.5V; V _I = V _{IL} or V _{IH} | | 0.5 | -5 | µA |
| I _{CCH} | Quiescent supply current | V _{CC} = 2.7V; Outputs High, V _I = GND or V _{CC} , I _O = 0 | | 0.04 | 0.1 | mA |
| I _{CCL} | | V _{CC} = 2.7V; Outputs Low, V _I = GND or V _{CC} , I _O = 0 | | 2.3 | 4.5 | |
| I _{CCZ} | | V _{CC} = 2.7V; Outputs Disabled; V _I = GND or V _{CC} , I _O = 0 ⁵ | | 0.04 | 0.1 | |
| ΔI _{CC} | Additional supply current per input pin ² | V _{CC} = 2.3V to 2.7V; One input at V _{CC} -0.6V, Other inputs at V _{CC} or GND | | 0.04 | 0.4 | mA |

NOTES:

- All typical values are at V_{CC} = 2.5V and T_{amb} = 25°C.
- This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND.
- This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 2.5V ± 0.2V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
- Unused pins at V_{CC} or GND.
- I_{CCZ} is measured with outputs pulled up to V_{CC} or pulled down to ground.
- Not guaranteed.
- For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.

2.5V/3.3V 20-bit bus interface latch (3-State)

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AC CHARACTERISTICS (2.5V ± 0.2V RANGE)GND = 0V; $t_R = t_F = 2.5\text{ns}$; $C_L = 50\text{pF}$; $R_L = 500\Omega$; $T_{\text{amb}} = -40^\circ\text{C}$ to $+85^\circ\text{C}$.

| SYMBOL | PARAMETER | WAVEFORM | LIMITS | | | UNIT |
|--------------------------------------|--|----------|---|------------|------------|------|
| | | | $T_{\text{amb}} = -40$ to $+85^\circ\text{C}$ $V_{\text{CC}} = +2.5\text{V} \pm 0.2\text{V}$ | | | |
| | | | MIN | TYP | MAX | |
| t_{PLH} t_{PHL} | Propagation delay nDx to nQx | 2 | 0.5 0.5 | 1.8 2.1 | 3.0 3.6 | ns |
| t_{PLH} t_{PHL} | Propagation delay nLE to nQx | 1 | 1.0 2.0 | 2.7 4.2 | 4.3 6.5 | ns |
| t_{PZH} t_{PZL} | Output enable time to High and Low level | 4 5 | 1.5 0.5 | 3.0 1.8 | 4.0 3.2 | ns |
| t_{PHZ} t_{PLZ} | Output disable time from High and Low level | 4 5 | 1.5 1.0 | 3.1 2.4 | 4.5 3.8 | ns |

NOTE:1. All typical values are at $V_{\text{CC}} = 3.3\text{V}$ and $T_{\text{amb}} = 25^\circ\text{C}$.**AC SETUP REQUIREMENTS (2.5V ± 0.2V RANGE)**GND = 0V, $t_R = t_F = 2.5\text{ns}$, $C_L = 50\text{pF}$, $R_L = 500\Omega$

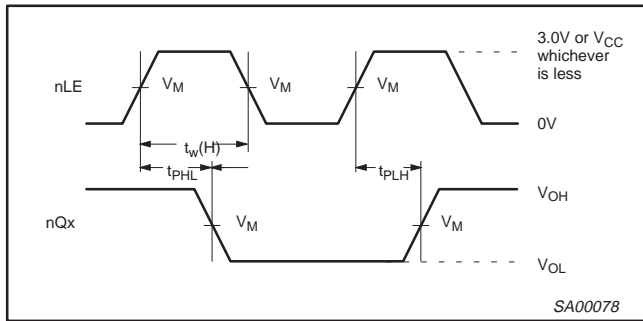
| SYMBOL | PARAMETER | WAVEFORM | LIMITS | | UNIT |
|------------------------------------|---------------------------------------|----------|---|----------|------|
| | | | $T_{\text{amb}} = -40$ to $+85^\circ\text{C}$ $V_{\text{CC}} = +2.5\text{V} \pm 0.2\text{V}$ | | |
| | | | Min | Typ | |
| $t_s(\text{H})$ $t_s(\text{L})$ | Setup time, High or Low nDx to nLE | 3 | 0.5 1.5 | 0 0.2 | ns |
| $t_h(\text{H})$ $t_h(\text{L})$ | Hold time, High or Low nDx to nLE | 3 | 1.8 2.0 | 0 0.8 | ns |
| $t_w(\text{H})$ | nLE pulse width High | 1 | 1.5 | | ns |

2.5V/3.3V 20-bit bus interface latch (3-State)

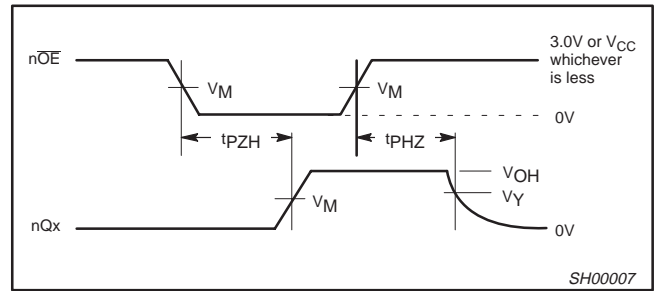
74ALVT16841

AC WAVEFORMS

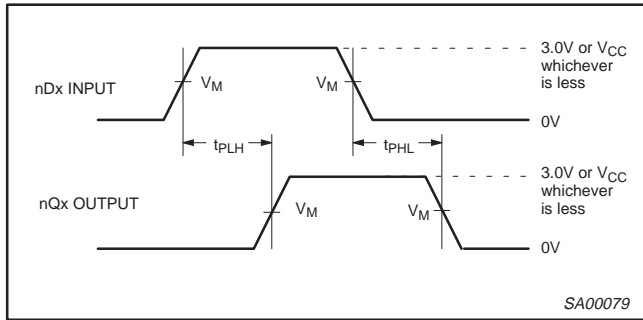
$V_M = 1.5V$ at $V_{CC} \geq 3.0V$; $V_M = V_{CC}/2$ at $V_{CC} \leq 2.7V$
 $V_X = V_{OL} + 0.3V$ at $V_{CC} \geq 3.0V$; $V_X = V_{OL} + 0.15V$ at $V_{CC} \leq 2.7V$
 $V_Y = V_{OH} - 0.3V$ at $V_{CC} \geq 3.0V$; $V_Y = V_{OH} - 0.15V$ at $V_{CC} \leq 2.7V$



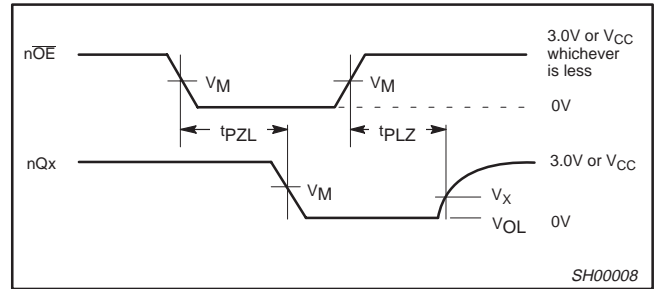
Waveform 1. Propagation Delay, Latch Enable Input to Output, and Enable Pulse Width



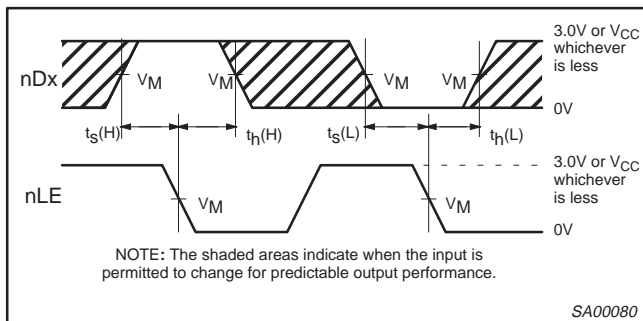
Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time from High Level



Waveform 2. Propagation Delay for Data to Outputs



Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level



Waveform 3. Data Setup and Hold Times

2.5V/3.3V 20-bit bus interface latch (3-State)

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TEST CIRCUIT AND WAVEFORM

The test circuit diagram shows a Pulse Generator connected to the input V_{IN} of a D.U.T. (Device Under Test). The input is terminated with a resistor R_T . The output V_{OUT} is connected to a load resistor R_L and a load capacitor C_L . A switch selects the load condition: 6.0V or $V_{CC} \times 2$, Open, or GND. The timing waveforms show a negative pulse (falling edge) and a positive pulse (rising edge) with parameters t_W , t_{THL} (t_F), and t_{TLH} (t_R).

Test Circuit for 3-State Outputs

SWITCH POSITION

| TEST | SWITCH |
|-------------------|-------------------------|
| t_{PLZ}/t_{PZL} | 6V or $V_{CC} \times 2$ |
| t_{PLH}/t_{PHL} | Open |
| t_{PHZ}/t_{PZH} | GND |

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.
 C_L = Load capacitance includes jig and probe capacitance: See AC CHARACTERISTICS for value.
 R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

| FAMILY | INPUT PULSE REQUIREMENTS | | | | |
|----------|------------------------------------|---------------------|-------|---------------------|---------------------|
| | Amplitude | Rep. Rate | t_W | t_R | t_F |
| 74ALVT16 | 3.0V or V_{CC} whichever is less | $\leq 10\text{MHz}$ | 500ns | $\leq 2.5\text{ns}$ | $\leq 2.5\text{ns}$ |

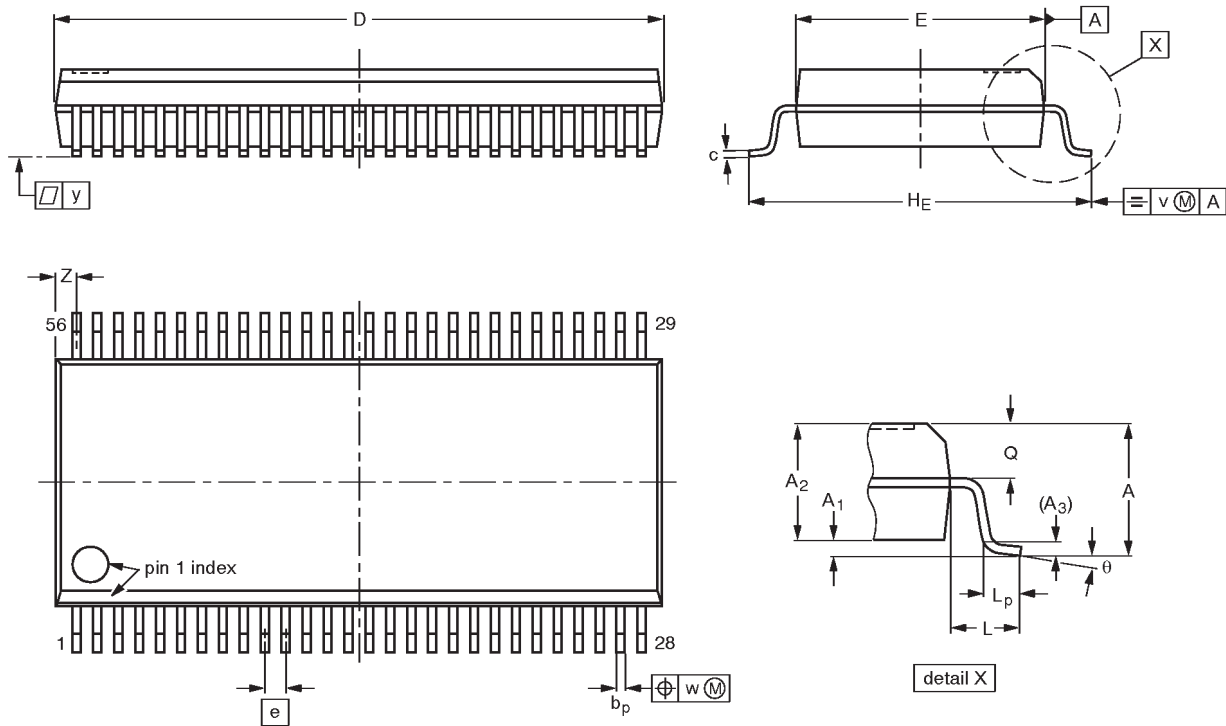
SW00025

2.5V/3.3V ALVT 20-bit bus interface latch (3-State)

74ALVT16841

SSOP56: plastic shrink small outline package; 56 leads; body width 7.5 mm

SOT371-1



DIMENSIONS (mm are the original dimensions)

| UNIT | A max. | A ₁ | A ₂ | A ₃ | b _p | c | D ⁽¹⁾ | E ⁽¹⁾ | e | H _E | L | L _p | Q | v | w | y | Z ⁽¹⁾ | θ |
|------|--------|----------------|----------------|----------------|----------------|--------------|------------------|------------------|-------|----------------|-----|----------------|------------|------|------|-----|------------------|----------|
| mm | 2.8 | 0.4 0.2 | 2.35 2.20 | 0.25 | 0.3 0.2 | 0.22 0.13 | 18.55 18.30 | 7.6 7.4 | 0.635 | 10.4 10.1 | 1.4 | 1.0 0.6 | 1.2 1.0 | 0.25 | 0.18 | 0.1 | 0.85 0.40 | 8° 0° |

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

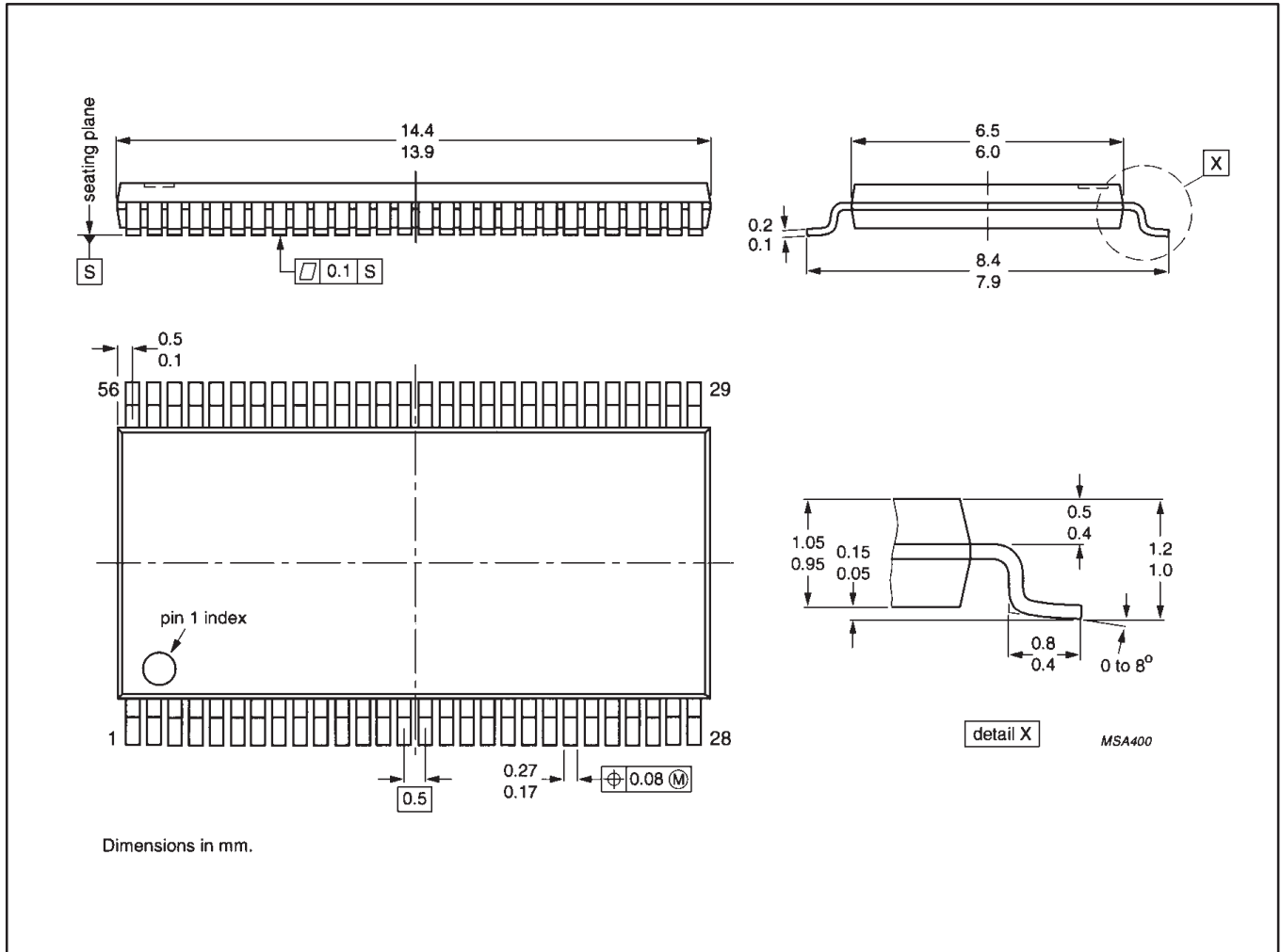
| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|----------|------|--|---------------------|----------------------|
| | IEC | JEDEC | EIAJ | | | |
| SOT371-1 | | MO-118AB | | | | 93-11-02 95-02-04 |

2.5V/3.3V ALVT 20-bit bus interface latch (3-State)

74ALVT16841

TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1mm

SOT364-1



2.5V/3.3V ALVT 20-bit bus interface latch (3-State)

74ALVT16841

Data sheet status

| Data sheet status | Product status | Definition [1] |
|---------------------------|----------------|--|
| Objective specification | Development | This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice. |
| Preliminary specification | Qualification | This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product. |
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

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Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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