Integrated Circuit Systems, Inc.

AV9170

Clock Synchronizer and Multiplier

General Description

The **AV9170** generates an output clock which is synchronized to a given continuous input clock with zero delay (±1ns at 5V V_{DD}). Using ICS's proprietary phase-locked loop (PLL) analog CMOS technology, the **AV9170** is useful for regenerating clocks in high speed systems where skew is a major concern. By the use of the two select pins, multiples or divisions of the input clock can be generated with zero delay (see Tables 2 and 3). The standard versions produce two outputs, where CLK2 is always a divide by two version of CLK1.

The **AV9170** is also useful to recover poor duty cycle clocks. A 50 MHz signal with a 20/80% duty cycle, for example, can be regenerated to the 48/52% typical of the part.
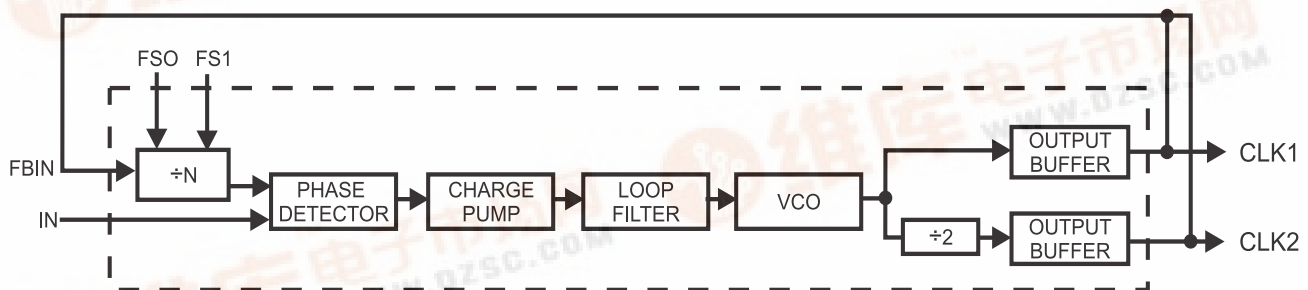
The **AV9170** allows the user to control the PLL feedback, making it possible, with an additional 74F240 octal buffer (or other such device that offers controlled skew outputs), to synchronize up to 8 output clocks with zero delay compared to the input (see Figure 1). Application notes for the **AV9170** are available. Please consult ICS.

Features

- On-chip Phase-Locked Loop for clocks synchronization
- Synchronizes frequencies up to 107 MHz (output) @ 5.0V
- ±1ns skew (max) between input & output clocks @ 5.0V
- Can recover poor duty cycle clocks
- CLK1 to CLK2 skew controlled to within ±1ns @ 5.0V
- 3.0 - 5.5V supply range
- Low power CMOS technology
- Small 8-pin DIP or SOIC package
- On chip loop filter
- **AV9170-01**, **-04** for output clocks 20-107 MHz @ 5.0V, 20 - 66.7 MHz @ 3.3V
- **AV9170-02**, **-05** for output clocks 5-26.75 MHz @ 5.0V, 5 - 16.7 MHz @ 3.3V
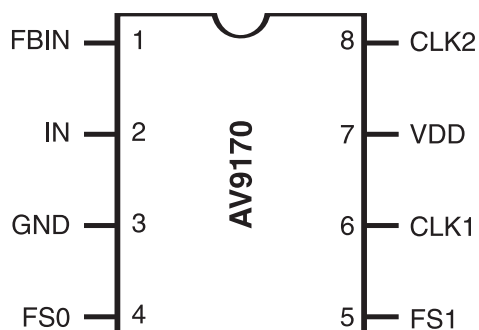
Block Diagram

External Connection to CLK1 or CLK2 (not both)

ICS reserves the right to make changes in the device data identified in this publication

Pin Configuration

8-Pin DIP or SOIC

Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	FBIN	Input	FEEDBACK INPUT
2	IN	Input	INPUT for reference clock
3	GND	—	GROUND
4	FS0	Input	FREQUENCY SELECT 0
5	FS1	Input	FREQUENCY SELECT 1
6	CLK1	Output	CLOCK output 1 (See Tables 1, 2, 3, 4, 5 for values)
7	VDD	—	Power Supply
8	CLK	Output	CLOCK output 2 (See Tables 1, 2, 3, 4, 5 for values)

Using the AV9170

The **AV9170** has the following characteristics:

1. Rising edges at IN and FBIN are lined up. Falling edges are not synchronized.

2. The relationship between the frequencies at FBIN and IN with CLK1 feedback is shown in Table 1 below.

Functionality (Table 1:)

FS1	FS0	f_{FBIN} (-01, -02)	f_{FBIN} (-04, -05)
0	0	$2 \cdot f_{IN}$	$3 \cdot f_{IN}$
0	1	$4 \cdot f_{IN}$	$5 \cdot f_{IN}$
1	0	f_{IN}	$6 \cdot f_{IN}$
1	1	$8 \cdot f_{IN}$	$10 \cdot f_{IN}$

3. The frequency of CLK2 is half the CLK1 frequency.

4. The CLK1 frequency ranges are:

		$V_{DD}=5V$	$V_{DD}=3.3V$
AV9170-01, -04	$20 < f_{CLK1} <$	107 MHz*	< 66.7
AV9170-02, -05	$5 < f_{CLK1} <$	26.75 MHz*	< 16.7

The **AV9170** will only operate correctly within these frequency ranges.

Eliminate High Speed Clock Routing Problems

The **AV9170** makes it possible to route lower speed clocks over long distances on the PC board and to place an **AV9170** next to the device requiring a higher speed clock. The multiplied output can then be used to produce a phase locked, higher speed output clock.

Compensate for Propagation Delays

Including an **AV9170** in a timing loop allows the use of PALs, gate arrays, etc., with loose timing specifications. The **AV9170** compensates for the delay through the PAL and synchronizes the output to the input reference clock.
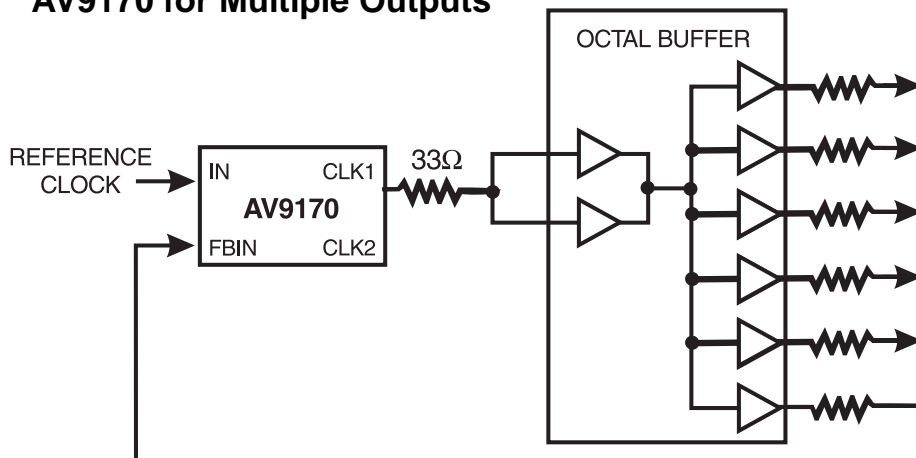
Operating Frequency Range

The **AV9170** is offered in versions optimized for operation in two frequency ranges. The -01 and -04 cover high frequencies, 20 to 100 MHz.* The -02 and -05 operate from 5 to 25 MHz.* The **AV9170** can be supplied with custom multiplication factors and operating ranges. Consult ICS for details.

3.3V VDD Operation

The **AV9170** does operate at both 5.0V and 3.3V system conditions. Please note the Electrical Characteristic specifications at 3.3V include a limited output frequency (66.6 MHz max.) and a wider skew of FBIN to CLK1. For 3.3V±5% (3.15V min.), this skew is -5.0 to 0 ns. At 3.3V±10% (3.0V min.), the skew is widened to -8 ns to 0 ns and should be accounted for in system design.

*At 3.3V, the maximum CLK1 frequency is 66.7 MHz for -01, -04 and 16.7 MHz for -02, -05.

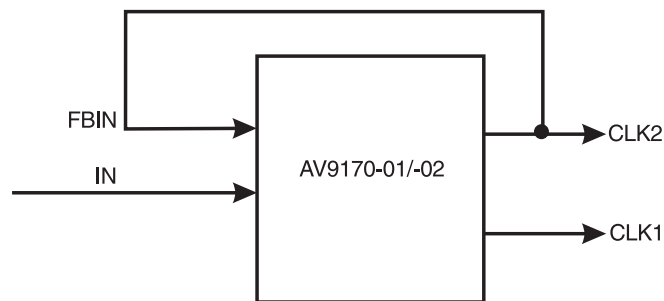## Figure 1: Application of AV9170 for Multiple Outputs

Using CLK2 Feedback

Connecting CLK2 to FBIN as shown in Figure 2 will cause all of the rising edges to be aligned (Figure 4).

Using CLK1 Feedback

With CLK1 connected to FBIN as shown in Figure 3, the input and CLK1 output will be aligned on the rising edge, but CLK2 can be either rising or falling (Figure 5). Consult ICS if the CLK1 frequency is desired to be higher than 107 MHz.

Figure 2:

For CLK2 frequencies 10 - 53.5 MHz* (-01)

For CLK2 frequencies 2.5 - 13.37 MHz (-02)

*Maximum 33.3 MHz @ 3.3V (-01), 8.33 MHz @ 3.3V (-02)

Figure 3:

For CLK1 frequencies 20 - 107 MHz† (-01)

For CLK1 frequencies 5 - 26.75 MHz (-02)

†Maximum 66.7 MHz @ 3.3V (-01), 16.7 MHz @ 3.3V (-02)

**Table 2:
Functionality Table for AV9170-01, -02 with CLK2 Feedback**

FS1	FS0	CLK1	CLK2
0	0	INx4	INx2
0	1	INx8	INx4
1	0	INx2	IN
1	1	INx16	INx8

**Table 3:
Functionality Table for AV9170-01, -02 with CLK1 Feedback**

FS1	FS0	CLK1	CLK2
0	0	INx2	IN
0	1	INx4	INx2
1	0	IN	IN÷2
1	1	INx8	INx4

**Figure 4:
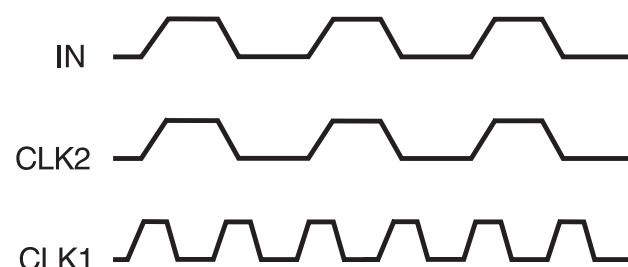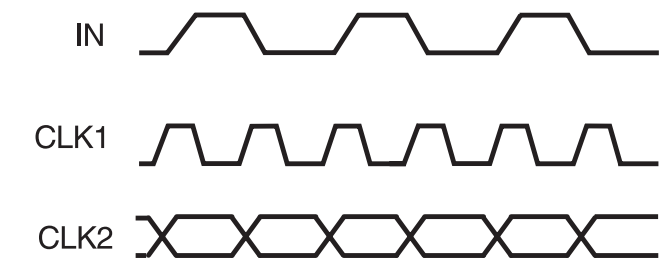Input and Output Clock Waveforms with CLK2 Connected to FBIN**

**Figure 5:
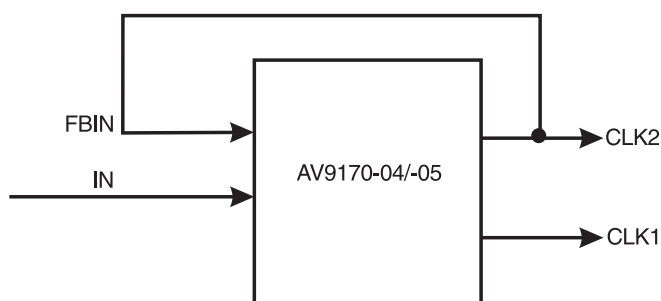Input and Output Clock Waveforms with CLK1 Connected to FBIN**

Using CLK2 Feedback

Connecting CLK2 to FBIN as shown in Figure 6 will cause all of the rising edges to be aligned (Figure 8).

Using CLK1 Feedback

With CLK1 connected to FBIN as shown in Figure 7, the input and CLK1 output will be aligned on the rising edge, but CLK2 can be either rising or falling (Figure 9).

Figure 6:

For CLK2 frequencies 10 - 53 MHz* (-04)

For CLK2 frequencies 2.5 - 13.37 MHz (-05)

*Maximum 33.3 MHz @ 3.3V (-04), 8.33 MHz @ 3.3V (-05)

Figure 7:

For CLK1 frequencies 20 - 107 MHz† (-04)

For CLK1 frequencies 5 - 26.75 MHz (-05)

†Maximum 66.7 MHz @ 3.3V (-04), 16.7 MHz @ 3.3V (-05)

Table 4:
Functionality Table for AV9170-04, -05 with CLK2 Feedback

FS1	FS0	CLK1	CLK2
0	0	INx6	INx3
0	1	INx10	INx5
1	0	INx12	INx6
1	1	INx20	INx10

Table 5:
Functionality Table for AV9170-04, -05 with CLK1 Feedback

FS1	FS0	CLK1	CLK2
0	0	INx3	INx1.5
0	1	INx5	INx2.5
1	0	INx6	INx3
1	1	INx10	INx5

Figure 8:
Input and Output Clock Waveforms with CLK2 Connected to FBIN

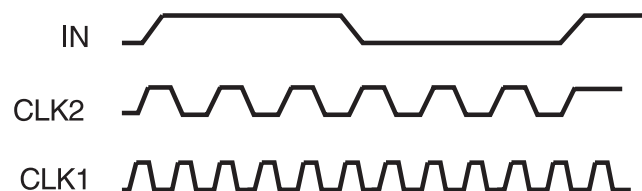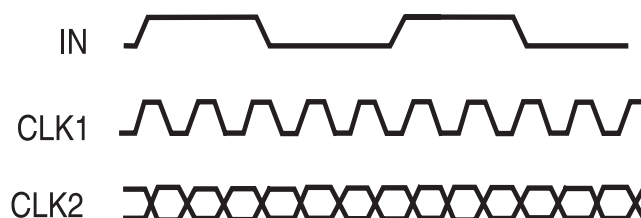### Figure 9:
Input and Output Clock Waveforms with CLK1 Connected to FBIN

Absolute Maximum Ratings

V_{DD} (referenced to GND). . . . . 7.0 V

Operating Temperature under Bias . . . . 0°C to +70°C

Storage Temperature . . . . −65°C to +150°C

Voltage on I/O pins referenced to GND . . . . . GND − 0.5 V to V_{DD} + 0.5 V

Power Dissipation . . . . 0.5 watts

Stresses above those listed under *Absolute Maximum Ratings* above may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics at 5V

V_{DD} = +5V ± 5%, T_A = 0°C to 70°C, unless otherwise stated

DC / CHARACTERISTICS						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	VIL	VDD = 5V	—	—	0.8	V
Input High Voltage	VIH	VDD = 5V	2.0	—	—	V
Input Low Current	IIL	VIN = 0V	−1.5	–5	—	µA
Input High Current	IIH	VIN = VDD	—	—	5	µA
Output Low Voltage	*VOL	IOL = 8mA	—	—	0.4	V
Output High Voltage	*VOH1	IOH = -1mA, VDD = 5.0V	VDD -.4V	—	—	V
Output High Voltage	*VOH2	IOH = -4mA, VDD = 5.0V	VDD -.8V	—	—	V
Output High Voltage	*VOH3	IOH = -8mA,	2.4	—	—	V
Supply Current	IDD1	Unloaded, 100 MHZ (-01, -04)	—	30	50	mA
Supply Current	IDD2	Unloaded, 25 MHZ (-02, -05)	—	13	20	mA

*Parameter guaranteed by design and characterization. Not 100% tested in production.

Notes:
1. It may be possible to operate the AV9170 outside of these ranges. Consult ICS for your specific application.
2. All AC Specifications are measured with a 50Ω transmission line, load terminated with 50Ω to 1.4V.
3. Duty cycle measured at 1.4V.
4. Skew measured at 1.4V on rising edges. Positive sign indicates the first signal precedes the second signal.

Electrical Characteristics at 5V

V_{DD} = +5V ±5%, T_A = 0°C to 70°C, unless otherwise stated

A/C CHARACTERISTICS						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Clock Rise Time	ICLKr*		—	—	10	ns
Input Clock Fall Time	ICLKf*		—	—	10	ns
Output Rise time, 0.8 to 2.0V	tr1*	15pF load.	—	0.6	2	ns
Rise time, 20% to 80% VDD	tr2*	15pF load.	—	1.2	3	ns
Output Fall time, 2.0 to 0.8V	tf1*	15pF load.	—	0.4	2	ns
Fall time, 80% to 20% VDD	tf2*	15pF load.	—	0.9	2	ns
Output Duty Cycle, AV9170-01	dt1*	15pF load. Note 2, 3	40	48/52	60	%
Output Duty Cycle, AV9170-02	dt2*	15pF load. Note 2, 3	45	49/51	55	%
Jitter, 1 sigma	T1s*		—	125	300	ps
Jitter, absolute	Tabs1*	For CLK1 > 10 MHz (-01, -04) For CLK1 > 2.5 MHz (-02, -05)	–500	—	500	ps
Jitter, absolute	Tabs2*	For CLK1 < 10 MHz (-01, -04) For CLK1 < 2.5 MHz (-02, -05)	—	—	2	%
Input Frequency	fi1	Note 1, AV9170-01, -04	8	—	107	MHz
Input Frequency	fi2	AV9170-02, -05	2	—	26.75	MHz
Output Frequency CLK1	fo1	AV9170-01, -04	20	—	107	MHz
Output Frequency CLK1	fo2	AV9170-02, -05	5	—	26.75	MHz
FBIN to IN skew	Tskew1*	Note 2, 4; 15pF load Input rise time < 5ns	–1	–0.3	1	ns
FBIN to IN skew	Tskew2*	Note 2, 4; 15pF load Input rise time < 10ns	–2	–0.3	2	ns
CLK1 to CLK2 skew	Tskew3*	Note 2, 4	–1	0.4	1	ns

*Parameter guaranteed by design and characterization. Not 100% tested in production.

Notes:
1. It may be possible to operate the AV9170 outside of these ranges. Consult ICS for your specific application.
2. All AC Specifications are measured with a 50Ω transmission line, load terminated with 50Ω to 1.4V.
3. Duty cycle measured at 1.4V.
4. Skew measured at 1.4V on rising edges. Positive sign indicates the first signal precedes the second signal.

Electrical Characteristics at 3.3V

V_{DD} = +3.3V ±5%, T_A = 0°C to 70°C, unless otherwise stated

DC / CHARACTERISTICS						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	VIL	VDD = 3.3V	—	—	0.2 VDD	V
Input High Voltage	VIH	VDD = 3.3V	0.7 VDD	—	—	V
Input Low Current	IIL	VIN = 0V	–7	–4	—	µA
Input High Current	IIH	VIN = VDD	—	—	5	µA
Output Low Voltage	*VOL	IOL = 6mA	—	—	0.4	V
Output High Voltage	*VOH1	IOH = -1mA, VDD = 3.3V	VDD -.4V	—	—	V
Output High Voltage	*VOH2	IOH = -3mA, VDD = 3.3V	VDD -.8V	—	—	V
Output High Voltage	*VOH3	IOH = -6mA,	2.4	—	—	V
Supply Current	IDD1	Unloaded, 66.7 MHZ (-01, -04)	—	17	30	mA
Supply Current	IDD2	Unloaded, 16.7 MHZ (-02, -05)	—	7	15	mA

*Parameter guaranteed by design and characterization. Not 100% tested in production.

Notes:
1. It may be possible to operate the AV9170 outside of these ranges. Consult ICS for your specific application.
2. All AC Specifications are measured with a 50Ω transmission line, load terminated with 50Ω to 1.4V.
3. Duty cycle measured at 1.4V.
4. Skew measured at 1.4V on rising edges. Positive sign indicates the first signal precedes the second signal.

Electrical Characteristics at 3.3V

V_{DD} = +3.3V ±5%, T_A = 0°C to 70°C, unless otherwise stated

A/C CHARACTERISTICS						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Clock Rise Time	ICLKr*		—	—	10	ns
Input Clock Fall Time	ICLKf*		—	—	10	ns
Output Rise time, 0.8 to 2.0V	tr1*	15pF load.	—	1.1	2	ns
Rise time, 20% to 80% VDD	tr2*	15pF load.	—	1.8	4	ns
Output Fall time, 2.0 to 0.8V	tf1*	15pF load.	—	0.8	2	ns
Fall time, 80% to 20% VDD	tf2*	15pF load.	—	1.2	3	ns
Output Duty Cycle, AV9170-01, -04	dt1*	15pF load. Note 2, 3	40	52	60	%
Output Duty Cycle, AV9170-02, -05	dt2*	15pF load. Note 2, 3	45	51	55	%
Jitter, 1 sigma	T1s*		—	150	300	ps
Jitter, absolute	Tabs1*	For CLK1 > 10 MHz (-01, -04) For CLK1 > 2.5 MHz (-02, -05)	–500	—	500	ps
Jitter, absolute	Tabs2*	For CLK1 < 10 MHz (-01, -04) For CLK1 < 2.5 MHz (-02, -05)	–2	—	2	%
Input Frequency	fi1	AV9170-01, -04	7	—	66.7	MHz
Input Frequency	fi2	AV9170-02, -05	2	—	16.7	MHz
Output Frequency CLK1	fo1	AV9170-01, -04	20	—	66.7	MHz
Output Frequency CLK1	fo2	AV9170-02, -05	5	—	16.7	MHz
FBIN to IN skew	Tskew1*	Note 2, 4; 15pF load 3.0 ≤ VDD ≤ 3.7	–8.0	–2.0	0	ns
FBIN to IN skew	Tskew2*	Note 2, 4; 15pF load 3.0 ≤ VDD ≤ 3.7	–5.0	–2.0	0	ns
CLK1 to CLK2 skew	Tskew3*	Note 2, 4; 15pF load	–2.0	–0.9	0	ns

*Parameter guaranteed by design and characterization. Not 100% tested in production.

Notes:
1. It may be possible to operate the AV9170 outside of these ranges. Consult ICS for your specific application.
2. All AC Specifications are measured with a 50Ω transmission line, load terminated with 50Ω to 1.4V.
3. Duty cycle measured at 1.4V.
4. Skew measured at 1.4V on rising edges. Positive sign indicates the first signal precedes the second signal.
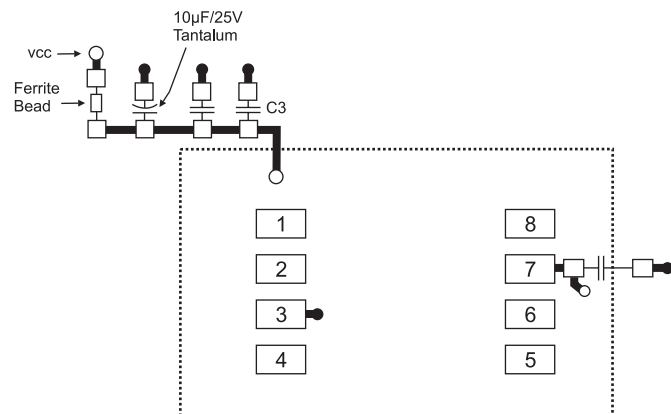
General Layout Precautions:

1) Use a ground plane on the top layer of the PCB in all areas not used by traces.
2) Make all power traces and vias as wide as possible to lower inductance.

Notes:

1) All clock outputs should have series terminating resistor. Not shown in all places to improve readibility of diagram.
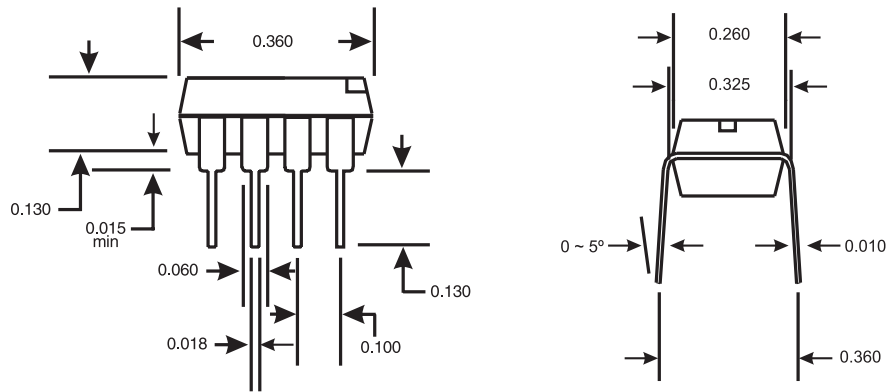
Connections to VDD:

Best
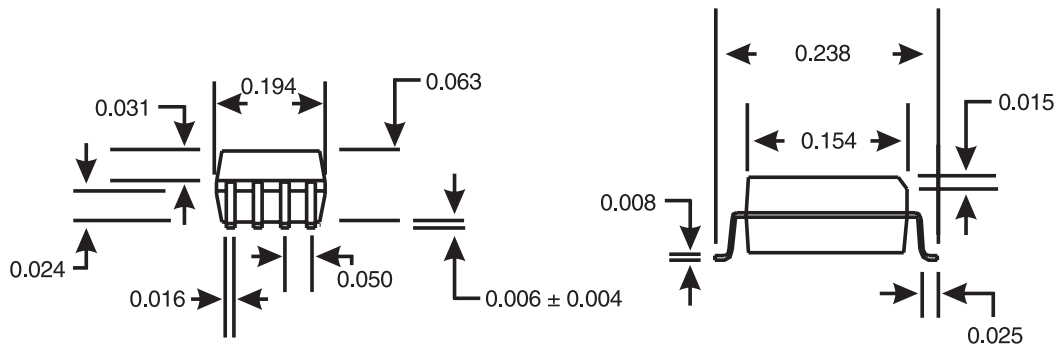
Okay

Avoid

Avoid

● = Ground Plane Connection

○ = Power Plane Conncetion

□ = Solder Pads

⬡ = Clock Load

8-Pin DIP PACKAGE

8-Pin SOIC PACKAGE

Ordering Information

AV9170-xxCN8 (8 Lead Plastic DIP [300 mils])

AV9170-xxCS8 (8 Lead SOIC [150 mils])

Example:

ICS XXXX - PPP M X#W

Lead Count & Package Width
  Lead Count = 1, 2 or 3 digits
  W = 0.3" SOIC or 0.6" DIP; None = Standard Width

Package Type
  N = DIP (Plastic)
  S = SOIC

Pattern Number (2 or 3 digit number for parts with ROM code patterns)

Device Type (consists of 3 or 4 digit numbers)

Prefix
  ICS = Standard Device; AV = ICS (West Coast)

For the SOIC package, the AV9170-01 is marked AV70-1 and the AV9170-02 is marked AV70-2.