Integrated Circuit Systems, Inc.

AV9173-15

Video Genlock PLL

General Description

The **AV9173-15** provides the analog circuit blocks required for implementing a video genlock dot (pixel) clock generator. It contains a phase detector, charge pump, loop filter, and voltage-controlled oscillator (VCO). By grouping these critical analog blocks into one IC and utilizing external digital functions, performance and design flexibility are optimized as are development time and system cost.

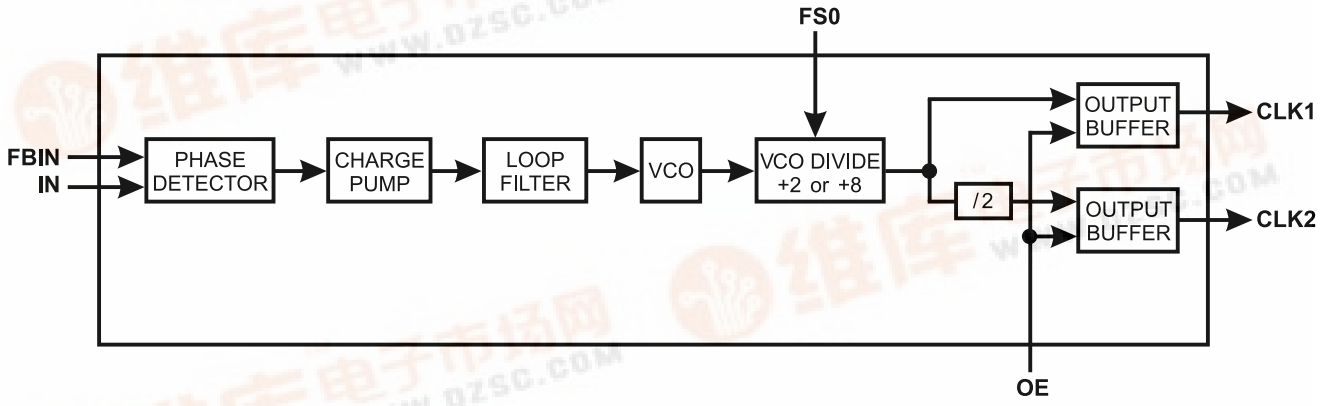
When used with an external clock divider, the **AV9173-15** forms a Phase-Locked Loop configured as a frequency synthesizer. The **AV9173-15** is designed to accept video horizontal synchronization (h-sync) pulses and produce a video dot clock. A separated, negative-going sync input reference pulse is required at pin 2 (IN).

The **AV9173-15** is also suited for other clock recovery applications in such areas as data communications.

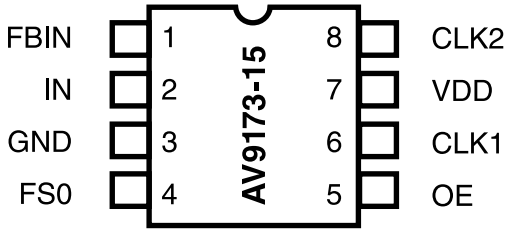
Features

- Phase-detector/VCO circuit block
- Ideal for genlock system
- Reference clock range 12 kHz to 1 MHz (see specification of output clock range)
- Output clock range 0.625 to 37.5 MHz for CLK1, depending on input conditions (see Table 1) on page 2.
- Provides h-sync capability with CLK1 outputs 15 to 37.5 MHz for 15 kHz input
- On-chip loop filter
- Single 5 volt power supply
- Low power CMOS technology
- Small 8-pin DIP or SOIC package

Block Diagram



Pin Configuration



8-Pin DIP or SOIC

Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	FBIN	Input	Feedback Input
2	IN	Input	Input for reference sync pulse
3	GND	—	Ground
4	FS0	Input	Internal VCO divider select input
5	OE	Input	Output Enable
6	CLK1	Output	Clock Output 1
7	VDD	—	Power Supply (+5V)
8	CLK2	Output	Clock Output 2 (Divided-by-2 from Clock 1)

Table 1: Allowable Input Frequency to Output Frequency (Outputs in MHz)

f_{IN} (kHz)	f_{OUT} for FS = 0 (MHz)		f_{OUT} for FS = 1 (MHz)	
	CLK1 Output	CLK2 Output	CLK1 Output	CLK2 Output
$12 \le f_{IN} \le 14$ kHz	22.0 to 37.5	11.0 to 18.75	5.5 to 9.375	2.75 to 4.6875
$14 < f_{IN} \le 17$ kHz	15 to 37.5	7.5 to 18.75	3.75 to 9.375	1.875 to 4.6875
$17 < f_{IN} \le 30$ kHz	12.5 to 37.5	6.25 to 18.75	3.125 to 9.375	1.5625 to 4.6875
$30 < f_{IN} \le 35$ kHz	7.5 to 37.5	3.75 to 18.75	1.875 to 9.375	0.9375 to 4.6875
$35 < f_{IN} \le 1000$ kHz	5.0 to 37.5	2.5 to 18.75	1.25 to 9.375	0.625 to 4.6875

Using the AV9173-15

Most video sources, such as video cameras, are asynchronous, free-running devices. To digitize video or synchronize one video source to another free-running reference video source, a video “genlock” (generator lock) circuit is required. The **AV9173-15** integrates the analog blocks which make the task much easier.

In the complete video genlock circuit, the primary function of the **AV9173-15** is to provide the analog circuitry required to generate the video dot clock within a PLL. This application is illustrated in Figure 1. The input reference signal for this circuit is the horizontal synchronization (h-sync) signal. If a composite video reference source is being used, the h-sync pulses must be separated from the composite signal. A video sync separator circuit, such as the National Semiconductor LM1881, can be used for this purpose.

The clock feedback divider shown in Figure 1 is a digital divider used within the PLL to multiply the reference frequency. Its divide ratio establishes how many video dot clock cycles occur per h-sync pulse. For example, if 880 pixel clocks are desired per h-sync pulse, then the divider ratio is set to 880. Hence, together the h-sync frequency and external divider ratio establish the dot clock frequency:

$f_{OUT} = f_{IN} \bullet N$ where N is external divide ratio

Both **AV9173-15** input pins IN and FBIN respond only to negative-going clock edges of the input signal. The h-sync signal must be constant frequency in the 12 kHz to 1MHz range and stable (low clock jitter) for creation of a stable output clock.

The output hook-up of the **AV9173-15** is dictated by the desired dot clock frequency. The primary consideration is the internal VCO which operates over a frequency range of 10 MHz to 75 MHz. Because of the selectable VCO output divider and the additional divider on output CLK2, four distinct output frequency ranges can be achieved. The following Table lists these ranges and the corresponding device configuration.

FS0 State	Output Used	Frequency Range
0	CLK1	5 - 37.5 MHz
0	CLK2	2.5 - 18.75 MHz
1	CLK1	1.25 - 9.375 MHz
1	CLK2	0.625 - 4.6875 MHz

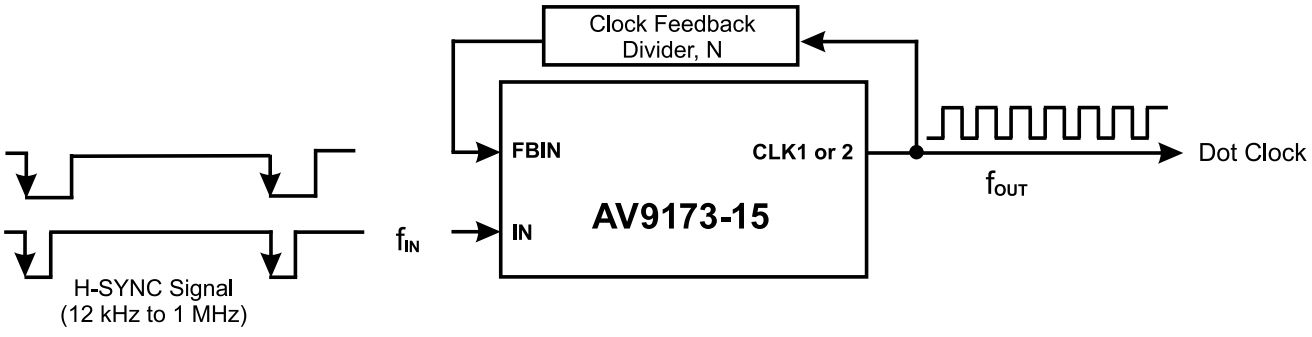
Note that both outputs, CLK1 and CLK2, are available during operation even though only one is fed back via the external clock divider.

Pin 5, OE, tristates both CLK1 and CLK2 upon logic low input. This feature can be used to revert dot clock control to the system clock when not in genlock mode (hence, when in genlock mode the system dot clock must be tristated).

When unused, inputs FS0 and OE must be tied to either GND (logic low) or VDD (logic high).

For further discussion of VCO/PLL operation as it applies to the **AV9173-15**, please refer to the AV9170 application note. The AV9170 is a similar device with fixed feedback dividers for skew control applications.

Figure 1: Typical Application of AV9173-15 in a Video Genlock System



Absolute Maximum Ratings

V_{DD} (referenced to GND) . . . . . 7.0 V
Operating Temperature under Bias . . . . . 0°C to +70°C
Storage Temperature . . . . . – 65°C to +150°C
Voltage on I/O pins referenced to GND . . . . . GND – 0.5 V to V_{DD} + 0.5 V
Power Dissipation . . . . . 0.5 watts

Stresses above those listed under *Absolute Maximum Ratings* above may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristic

V_{DD} = +5V ±5%, T_A = 0°C to 70°C, unless otherwise stated

DC CHARACTERISTICS						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V_{IL}	V_{DD} = 5V	—	—	0.8	V
Input High Voltage	V_{IH}	V_{DD} = 5V	2.0	—	—	V
Input Low Current	I_{IL}	V_{IN} = 0V	-5	—	—	µA
Input High Current	I_{IH}	V_{IN} = V_{DD}	-5	—	5	µA
Output Low Voltage[1]	V_{OL}	I_{OL} = 8mA	—	—	0.4	V
Output High Voltage[1]	V_{OH1}	I_{OH} = -1mA, V_{DD} = 5.0V	V_{DD} -.4V	—	—	V
Output High Voltage[1]	V_{OH2}	I_{OH} = -4mA, V_{DD} = 5.0V	V_{DD} -.8V	—	—	V
Output High Voltage[1]	V_{OH3}	I_{OH} = -8mA	2.4	—	—	V
Supply Current	I_{DD}	Unloaded, 50 MHZ	—	20	50	mA

Notes:

1. Parameter is guaranteed by design and characterization. Not 100% tested in production.

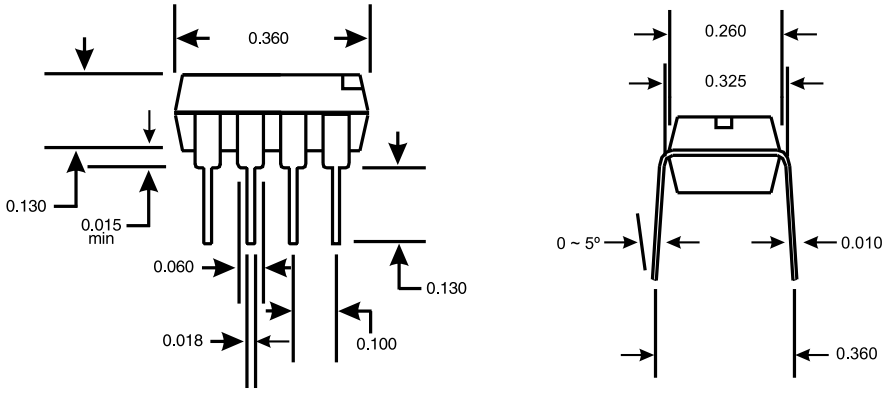
Electrical Characteristics

V_{DD} = +5V ±5%, T_A = 0°C to 70°C, unless otherwise stated

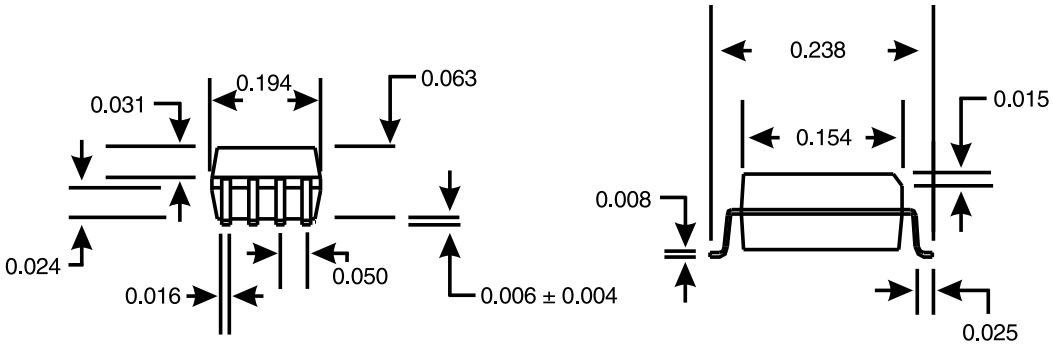
AC CHARACTERISTICS						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Clock Rise Time[1]	ICLKr		—	—	10	ns
Input Clock Fall Time[1]	ICLKf		—	—	10	ns
Output Rise Time[1]	t_{r1}	15pF load; 0.8 to 2.0V	—	0.6	1.5	ns
Rise time[1]	t_{r2}	15pF load; 20% to 80% V_{DD}	—	1.3	3.0	ns
Output Fall time[1]	t_{f1}	15pF load; 2.0 to 0.8V	—	0.6	1.5	ns
Fall time[1]	t_{f2}	15pF load; 80% to 20% V_{DD}	—	0.7	2.0	ns
Output Duty Cycle[1]	d_t	15pF load, V_{TH} =1.4V	40	47	55	%
Jitter,[1] 1 sigma	T_{1s1}	CLK1 freq.≥ 12.5 MHz	—	120	250	ps
Jitter,[1] 1 sigma	T_{1s2}	CLK1 freq.≥12.5 MHz	—	—	1	%
Jitter,[1] 1 absolute	T_{abs1}	CLK1 freq.< 12.5 MHz	-400	±250	400	ps
Jitter,[1] 1 absolute	T_{abs2}	CLK1 freq.< 12.5 MHz	—	—	2	%
Line-to-line jitter,[1] absolute[2]	TL_{abs}		—	±4	—	ns
Input Frequency,[1] IN or FBIN	f_{i1}	f_{VCO} 10 to 75 MHz	12.0	—	1000	kHz
CLK1 Frequency[3]	f_{CLK1}	12 ≤ f_i ≤ 14 kHz	22.0	—	37.5	MHz
		14 < f_i ≤ 17 kHz	15.0	—	37.5	MHz
		17 < f_i ≤ 30 kHz	12.5	—	37.5	MHz
		30 < f_i ≤ 35 kHz	7.5	—	37.5	MHz
		35 < f_i ≤ 1000 kHz	5.0	—	37.5	MHz

Notes:

1. Parameter is guaranteed by design and characterization. Not 100% tested in production.
2. Input Reference Frequency = 25 kHz, Output Frequency = 25 MHz. Jitter measured between adjacent vertical pixels.
3. CLK1 frequency applies for FS = 0. For FS = 1 condition, divide allowable CLK1 range by the factor of 4.



8-Pin DIP PACKAGE



8-Pin SOIC PACKAGE

Ordering Information

AV9173-15CN08 - or - AV9173-15CS08

Example:

XXX XXXX - PPP M X#W

Lead Count & Package Width
Lead Count = 1, 2 or 3 digits
W = 0.3" SOIC or 0.6" DIP; None = Standard Width

Package Type
N = DIP (Plastic)
S = SOIC

Pattern Number (2 or 3 digit number for parts with ROM code patterns)

Device Type (consists of 3 or 4 digit numbers)

Prefix
ICS, AV = Standard Device