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Integrated Circuit Systems, Inc.

ICS853031

LOW SKEW, 1-TO-9 DIFFERENTIAL-TO-2.5V/3.3V LVPECL/ECL FANOUT BUFFER

GENERAL DESCRIPTION

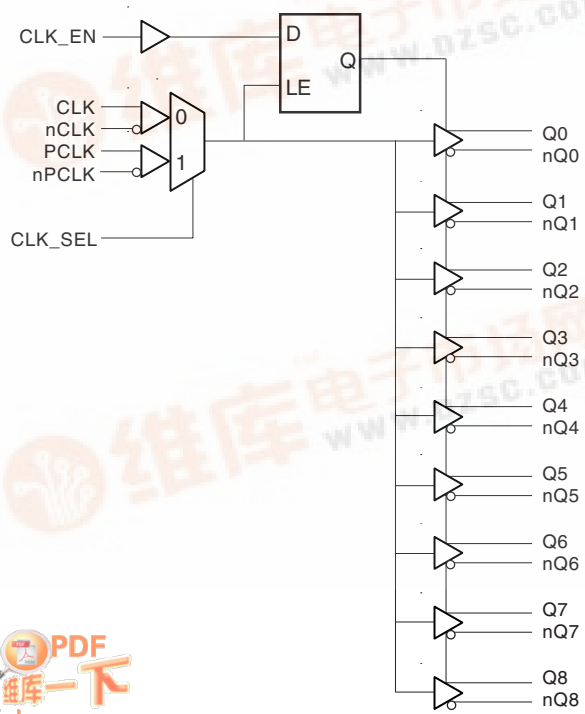
The ICS853031 is a low skew, high performance 1-to-9 Differential-to-2.5V/3.3V LVPECL/ECL Fanout Buffer and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The ICS853031 has two selectable clock inputs. The CLK, nCLK pair can accept most standard differential input levels. The PCLK, nPCLK pair can accept LVPECL, LVDS, CML, or SSTL input levels. The clock enable is internally synchronized to eliminate runt pulses on the outputs during asynchronous assertion/deassertion of the clock enable pin.

Guaranteed output skew and part-to-part skew characteristics make the ICS853031 ideal for high performance workstation and server applications.

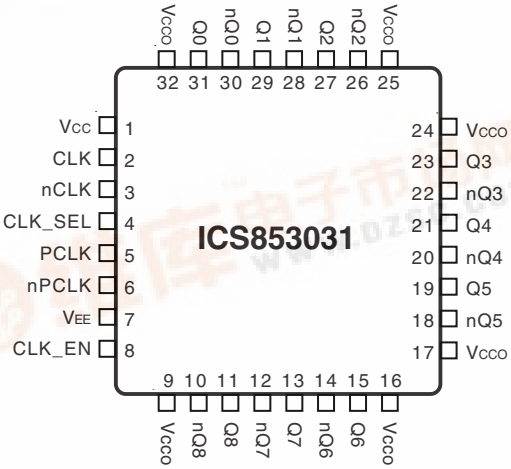
FEATURES

- 9 differential 2.5V/3.3V LVPECL/ECL outputs
- Selectable differential CLK, nCLK or LVPECL clock inputs
- CLK, nCLK pair can accept the following differential input levels: LVPECL, LVDS, LVHSTL, HCSL, SSTL,
- PCLK, nPCLK supports the following input types: LVPECL, LVDS, CML, SSTL
- Output frequency: 1.6GHz (typical)
- Translates any single ended input signal (LVCMOS, LVTTL, GTL) to 3.3V LVPECL levels with resistor bias on nCLK or nPCLK inputs
- Output skew: 20ps (typical)
- Part-to-part skew: 75ps (typical)
- Propagation delay: 875ps (typical)
- LVPECL mode operating voltage supply range: V_{CC} = 2.375V to 3.465V, V_{EE} = 0V
- ECL mode operating voltage supply range: V_{CC} = 0V, V_{EE} = -2.375V to -3.465V
- -40°C to 85°C ambient operating temperature
- Lead-Free package available
- Pin compatible with ICS8531-01

BLOCK DIAGRAM



PIN ASSIGNMENT



32-Lead LQFP
7mm x 7mm x 1.4mm package body
Y package
Top View

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TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	V_{CC}	Power		Core supply pin.
2	CLK	Input	Pulldown	Non-inverting differential clock input.
3	nCLK	Input	Pullup	Inverting differential clock input.
4	CLK_SEL	Input	Pulldown	Clock Select input. When HIGH, selects PCLK, nPCLK inputs. When LOW, selects CLK, nCLK. LVTTL / LVCMOS interface levels.
5	PCLK	Input	Pulldown	Non-inverting differential LVPECL clock input.
6	nPCLK	Input	Pullup	Inverting differential LVPECL clock input.
7	V_{EE}	Power		Negative supply pin.
8	CLK_EN	Input	Pullup	Synchronizing clock enable. When HIGH, clock outputs follow clock input. When LOW, Q outputs are forced low, nQ outputs are forced high. LVTTL / LVCMOS interface levels.
9, 16, 17, 24, 25, 32	V_{CCO}	Power		Output supply pins.
10, 11	nQ8, Q8	Output		Differential output pair. LVPECL interface level.
12, 13	nQ7, Q7	Output		Differential output pair. LVPECL interface level.
14, 15	nQ6, Q6	Output		Differential output pair. LVPECL interface level.
18, 19	nQ5, Q5	Output		Differential output pair. LVPECL interface level.
20, 21	nQ4, Q4	Output		Differential output pair. LVPECL interface level.
22, 23	nQ3 Q3	Output		Differential output pair. LVPECL interface level.
26, 27	nQ2, Q2	Output		Differential output pair. LVPECL interface level.
28, 29	nQ1, Q1	Output		Differential output pair. LVPECL interface level.
30, 31	nQ0, Q0	Output		Differential output pair. LVPECL interface level.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$R_{PULLDOWN}$	Input Pulldown Resistor			50		KΩ
R_{PULLUP}	Input Pullup Resistor			50		KΩ

TABLE 3A. CONTROL INPUT FUNCTION TABLE

Inputs			Outputs	
CLK_EN	**CLK_SEL**	**Selected Sourced**	**Q0:Q8**	**nQ0:nQ8**
0	0	CLK, nCLK	Disabled; LOW	Disabled; HIGH
0	1	PCLK, nPCLK	Disabled; LOW	Disabled; HIGH
1	0	CLK, nCLK	Enabled	Enabled
1	1	PCLK, nPCLK	Enabled	Enabled

After CLK_EN switches, the clock outputs are disabled or enabled following a rising and falling input clock edge as shown in Figure 1.
In the active mode, the state of the outputs are a function of the CLK, nCLK and PCLK, nPCLK inputs as described in Table 3B.

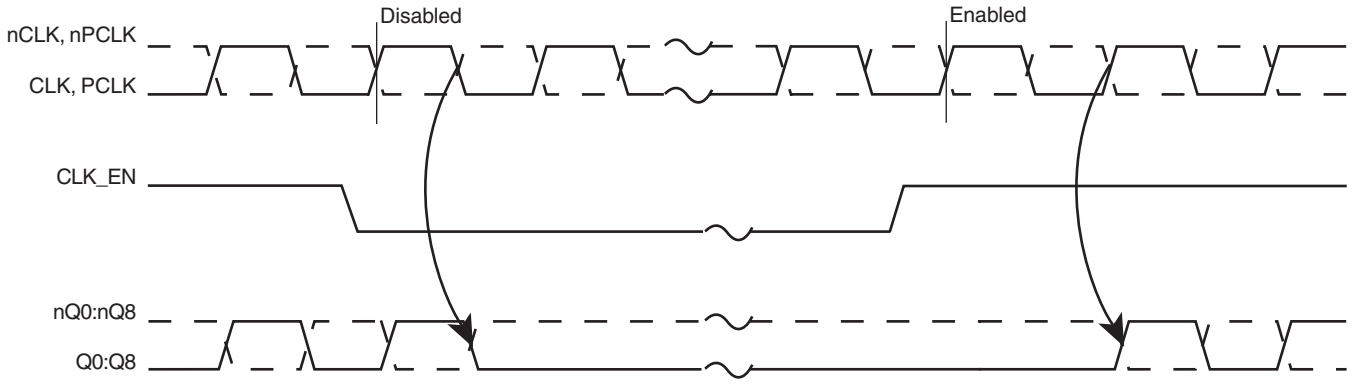


FIGURE 1. CLK_EN TIMING DIAGRAM

TABLE 3B. CLOCK INPUT FUNCTION TABLE

Inputs		Outputs		Input to Output Mode	Polarity
CLK or PCLK	**nCLK or nPCLK**	**Q0:Q8**	**nQ0:nQ8**		
0	1	LOW	HIGH	Differential to Differential	Non Inverting
1	0	HIGH	LOW	Differential to Differential	Non Inverting
0	Biased; NOTE 1	LOW	HIGH	Single Ended to Differential	Non Inverting
1	Biased; NOTE 1	HIGH	LOW	Single Ended to Differential	Non Inverting
Biased; NOTE 1	0	HIGH	LOW	Single Ended to Differential	Inverting
Biased; NOTE 1	1	LOW	HIGH	Single Ended to Differential	Inverting

NOTE 1: Please refer to the Application Information section, "Wiring the Differential Input to Accept Single Ended Levels".

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	4.6V
Negative Supply Voltage, V_{EE}	-4.6V
Inputs, V_I	-0.5V to V_{CC} + 0.5V
Outputs, I_O	
Continuous Current	50mA
Surge Current	100mA
Operating Temperature Range, TA	-40°C to +85°C
Storage Temperature, T_{STG}	-65°C to 150°C
Package Thermal Impedance, θ_{JA} (Junction-to-Ambient)	47.9°C/W (0 lfpm)

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, V_{CC} = 2.375 TO 3.465V; V_{EE} = 0V

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		2.375	3.3	3.465	V
V_{CCO}	Output Supply Voltage		2.375	3.3	3.465	V
I_{EE}	Power Supply Current				77	mA

TABLE 4B. LVCMOS/LVTTL DC CHARACTERISTICS, V_{CC} = 2.375 TO 3.465V; V_{EE} = 0V

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	CLK_EN, CLK_SEL			2		3.465	V
V_{IL}	CLK_EN, CLK_SEL			-0.3		0.8	V
I_{IH}	Input High Current	CLK_EN	V_{CC} = V_{IN} = 3.465V or 2.625V			10	µA
		CLK_SEL	V_{CC} = V_{IN} = 3.465V or 2.625V			150	µA
I_{IL}	Input Low Current	CLK_EN	V_{IN} = 0V, V_{CC} = 3.465V or 2.625V	-150			µA
		CLK_SEL	V_{IN} = 0V, V_{CC} = 3.465V or 2.625V	-50			µA

TABLE 4C. DIFFERENTIAL DC CHARACTERISTICS (CLK, nCLK), V_{CC} = 2.375 TO 3.465V; V_{EE} = 0V

Symbol	Parameter		-40°C			25°C			85°C			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{IH}	Input High Current	CLK			150			150			150	µA
		nCLK			10			10			10	µA
I_{IL}	Input Low Current	CLK	-50			-50			-50			µA
		nCLK	-150			-150			-150			µA
V_{PP}	Peak-to-Peak Input Voltage		0.15		1.3	0.15		1.3	0.15		1.3	V
V_{CMR}	Input High Voltage Common Mode Range; NOTE 1, 2		V_{EE} + 0.7		V_{CC} - 0.85	V_{EE} + 0.7		V_{CC} - 0.85	V_{EE} + 0.7		V_{CC} - 0.85	V

NOTE 1: For single ended applications, the maximum input voltage for CLK and nCLK is V_{CC} + 0.3V.
NOTE 2: Common mode voltage is defined as V_{IH}.

TABLE 4D. LVPECL DC CHARACTERISTICS (PCLK, nPCLK), V_{CC} = 3.3V; V_{EE} = 0V

Symbol	Parameter		-40°C			25°C			85°C			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output High Voltage; NOTE 1		2.175	2.275	2.38	2.225	2.295	2.37	2.22	2.295	2.365	V
V_{OL}	Output Low Voltage; NOTE 1		1.405	1.545	1.68	1.425	1.52	1.615	1.44	1.535	1.63	V
V_{PP}	Peak-to-Peak Input Voltage		0.15	0.8	1.3	0.15	0.8	1.3	0.15	0.8	1.3	V
V_{CMR}	Input High Voltage Common Mode Range; NOTE 2, 3		1.2		V_{CC}	1.2		V_{CC}	1.2		V_{CC}	V
I_{IH}	Input High Current	PCLK			150			150			150	µA
		nPCLK			10			10			10	µA
I_{IL}	Input Low Current	PCLK	-50			-50			-50			µA
		nPCLK	-150			-150			-150			µA

Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary ± 0.165V.
NOTE 1: Outputs terminated with 50Ω to V_{CCO} - 2V.
NOTE 2: Common mode voltage is defined as V_{IH}.
NOTE 3: For single-ended applications, the maximum input voltage for PCLK, nPCLK is V_{CC} + 0.3V.

TABLE 4E. LVPECL DC CHARACTERISTICS (PCLK, nPCLK), V_{CC} = 2.5V; V_{EE} = 0V

Symbol	Parameter		-40°C			25°C			85°C			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output High Voltage; NOTE 1		1.375	1.475	1.58	1.425	1.495	1.57	1.42	1.495	1.565	V
V_{OL}	Output Low Voltage; NOTE 1		0.605	0.745	0.88	0.625	0.72	0.815	0.64	0.735	0.83	V
V_{PP}	Peak-to-Peak Input Voltage		0.15	0.8	1.3	0.15	0.8	1.3	0.15	0.8	1.3	V
V_{CMR}	Input High Voltage Common Mode Range; NOTE 2, 3		1.2		V_{CC}	1.2		V_{CC}	1.2		V_{CC}	V
I_{IH}	Input High Current	PCLK			150			150			150	µA
		nPCLK			10			10			10	µA
I_{IL}	Input Low Current	PCLK	-10			-10			-10			µA
		nPCLK	-150			-150			-150			µA

Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary ± 0.125V.
NOTE 1: Outputs terminated with 50Ω to V_{CCO} - 2V.
NOTE 2: Common mode voltage is defined as V_{IH}.
NOTE 3: For single-ended applications, the maximum input voltage for PCLK, nPCLK is V_{CC} + 0.3V.

TABLE 4F. ECL DC CHARACTERISTICS (PCLK, nPCLK), V_{CC} = 0V; V_{EE} = -2.375V TO -3.465V

Symbol	Parameter		-40°C			25°C			85°C			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output High Voltage; NOTE 1		-1.125	-1.025	-0.92	-1.075	-1.005	-0.93	-1.08	-1.005	-0.935	V
V_{OL}	Output Low Voltage; NOTE 1		-1.895	-1.755	-1.62	-1.875	-1.78	-1.685	-1.86	-1.765	-1.67	V
V_{PP}	Peak-to-Peak Input Voltage		0.15	0.8	1.3	0.15	0.8	1.3	0.15	0.8	1.3	V
V_{CMR}	Input High Voltage Common Mode Range; NOTE 2, 3		V_{EE}+1.2		0	V_{EE}+1.2		0	V_{EE}+1.2		0	V
I_{IH}	Input High Current	PCLK			150			150			150	µA
		nPCLK			10			10			10	µA
I_{IL}	Input Low Current	PCLK	-10			-10			-10			µA
		nPCLK	-150			-150			-150			µA

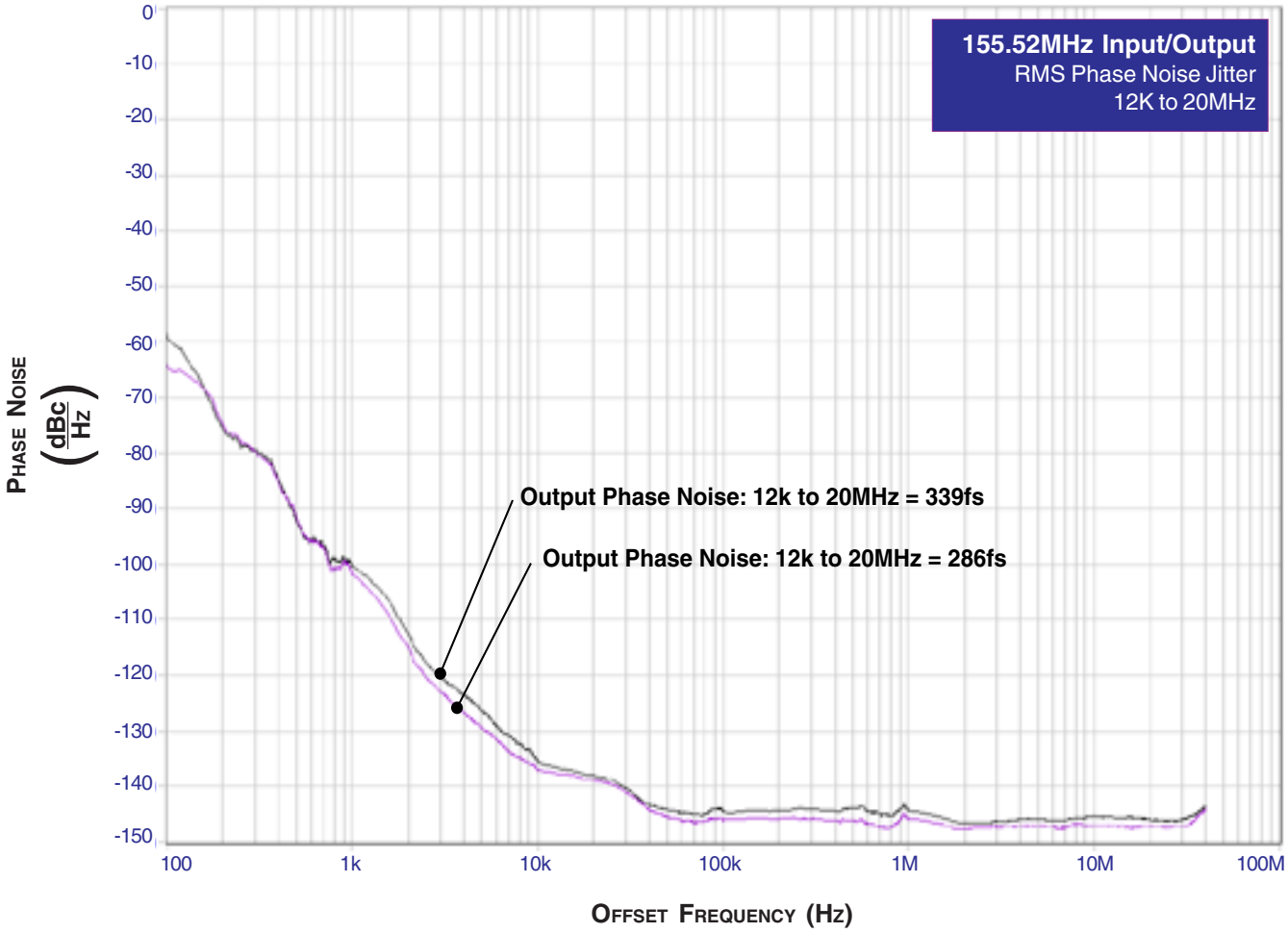
NOTE 1: Outputs terminated with 50Ω to V_{CCO} - 2V.
NOTE 2: Common mode voltage is defined as V_{IH}.
NOTE 3: For single-ended applications, the maximum input voltage for PCLK, nPCLK is V_{CC} + 0.3V.

TABLE 5. AC CHARACTERISTICS, V_{CC} = 0V; V_{EE} = -2.375V TO -3.465V OR V_{CC} = 2.375 TO 3.465V; V_{EE} = 0V

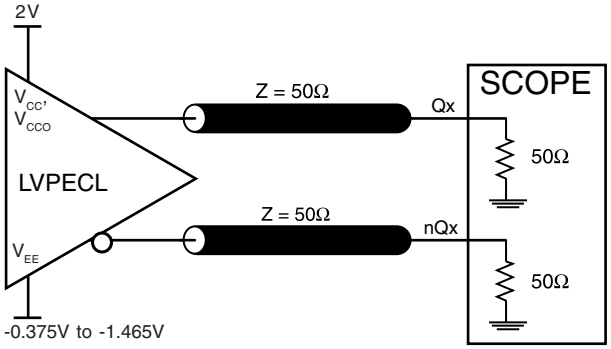
Symbol	Parameter		-40°C			25°C			85°C			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{MAX}	Output Frequency			>1.6			>1.6			>1.6		GHz
t_{PD}	Propagation Delay; NOTE 1	PCLK, nPCLK	750	825	900	785	875	965	825	925	1025	ps
		CLK, nCLK	820	920	1020	860	960	1060	910	1010	1110	ps
*t*sk(o)	Output Skew; NOTE 2, 4			20	55		20	55		25	55	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4			60	150		75	175		75	200	ps
t_R/t_F	Output Rise/Fall Time	20% to 80%	100	215	400	100	225	400	100	215	350	ps
odc	Output Duty Cycle	f ≤ 266MHz	48		52	48		52	48		52	%
		266MHz < f ≤ 500MHz	46		54	46		54	46		54	%

All parameters measured at ≤ 500MHz unless otherwise noted.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

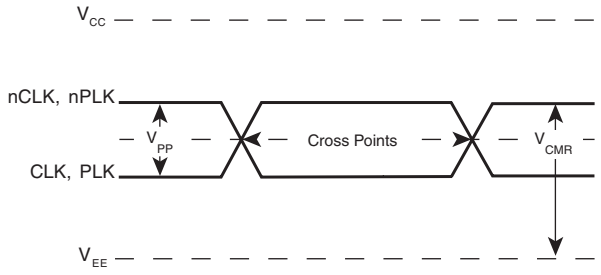
TYPICAL PHASE NOISE



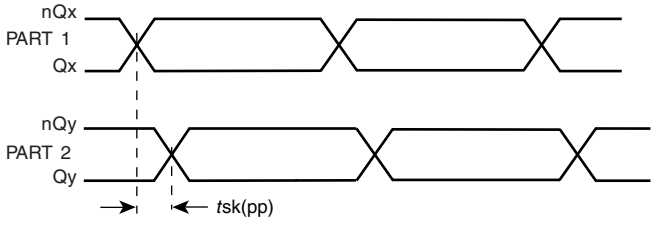
PARAMETER MEASUREMENT INFORMATION



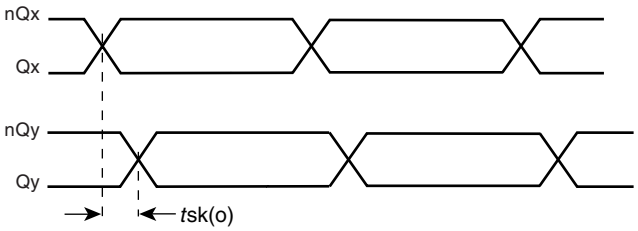
OUTPUT LOAD AC TEST CIRCUIT



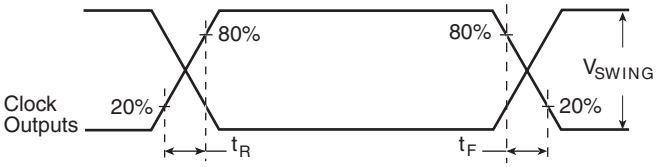
DIFFERENTIAL INPUT LEVEL



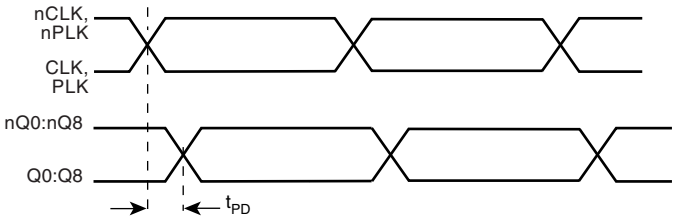
PART-TO-PART SKEW



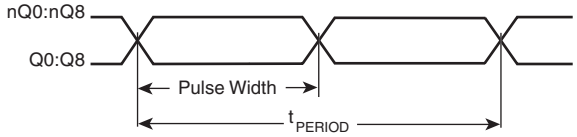
OUTPUT SKEW



OUTPUT RISE/FALL TIME



PROPAGATION DELAY



$$odc = \frac{t_{PW}}{t_{PERIOD}}$$

OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD

APPLICATION INFORMATION

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 2 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF $\simeq V_{CC}/2$ is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{CC} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

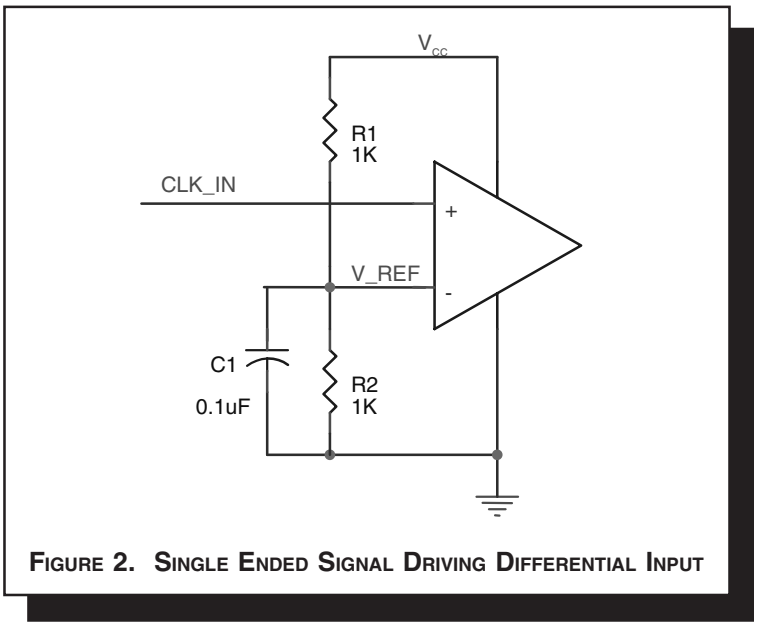


FIGURE 2. SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT

TERMINATION FOR 3.3V LVPECL OUTPUTS

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 3A and 3B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

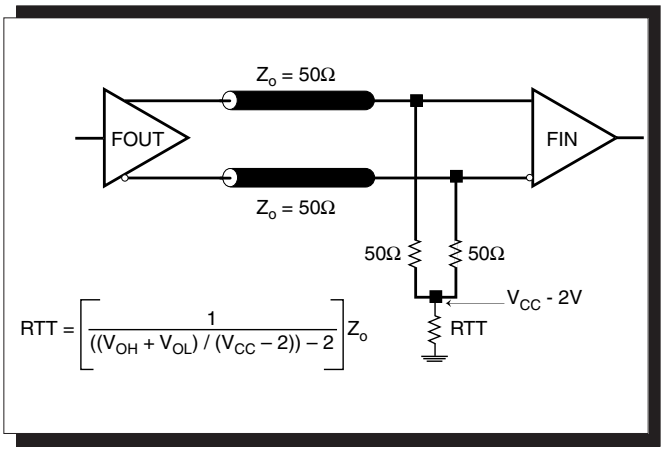


FIGURE 3A. LVPECL OUTPUT TERMINATION

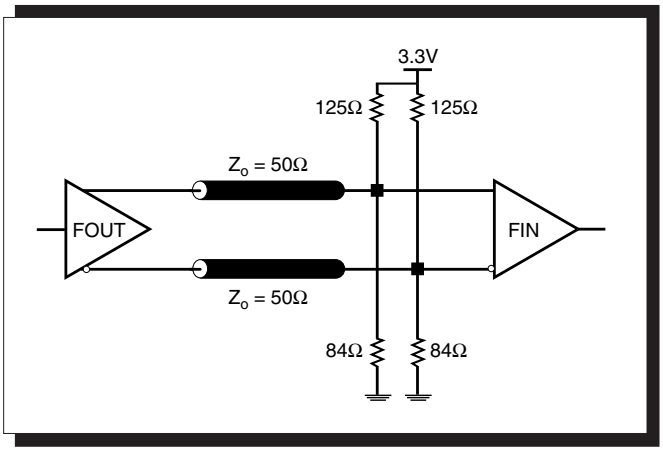


FIGURE 3B. LVPECL OUTPUT TERMINATION

TERMINATION FOR 2.5V LVPECL OUTPUT

Figure 4A and *Figure 4B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{CC} - 2V. For V_{CC} = 2.5V, the V_{CC} - 2V is very close to ground level. The R3 in Figure 4B can be eliminated and the termination is shown in *Figure 4C.*

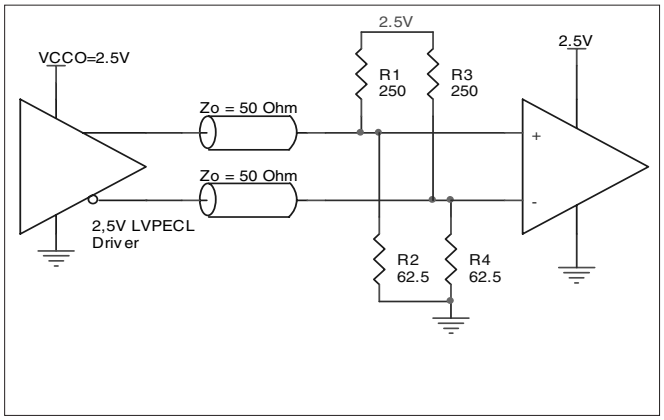


FIGURE 4A. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

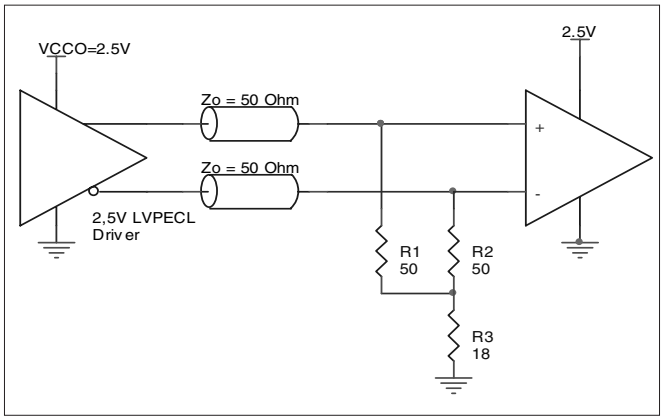


FIGURE 4B. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

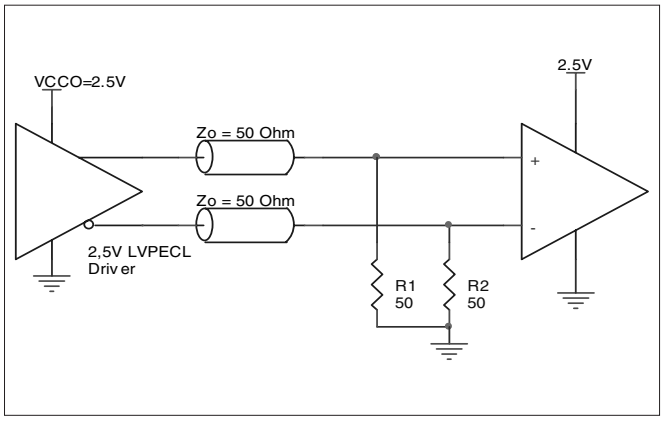


FIGURE 4C. 2.5V LVPECL TERMINATION EXAMPLE

DIFFERENTIAL CLOCK INPUT INTERFACE

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. Figures 5A to 5E show interface examples for the HiPerClockS CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example in *Figure 5A,* the input termination applies for ICS HiPerClockS LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

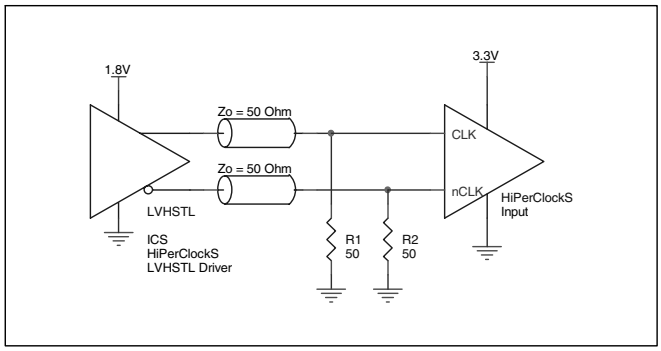


FIGURE 5A. HIPERCLOCKS CLK/NCLK INPUT DRIVEN BY ICS HIPERCLOCKS LVHSTL DRIVER

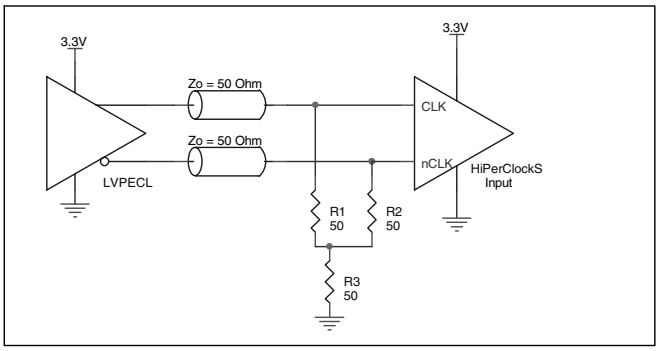


FIGURE 5B. HIPERCLOCKS CLK/NCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER

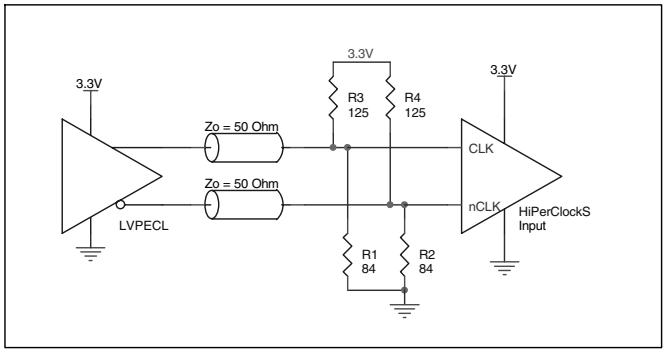


FIGURE 5C. HIPERCLOCKS CLK/NCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER

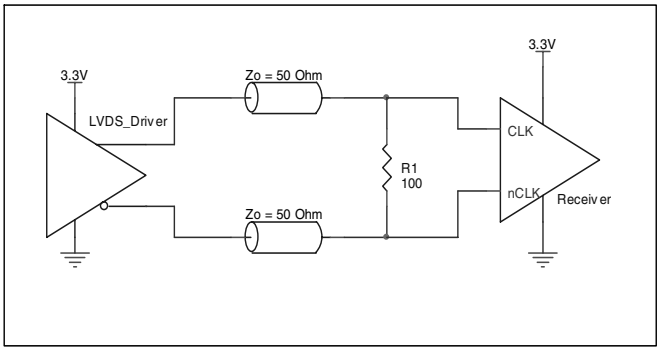


FIGURE 5D. HIPERCLOCKS CLK/NCLK INPUT DRIVEN BY 3.3V LVDS DRIVER

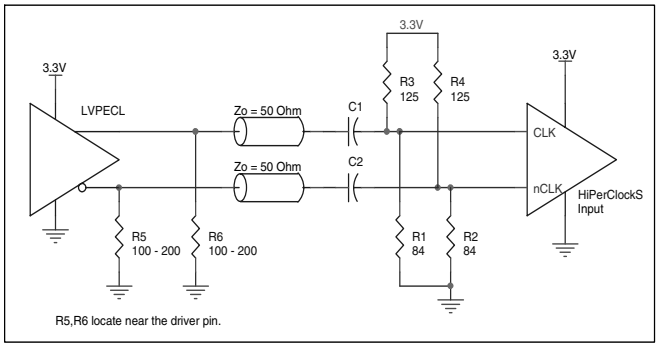


FIGURE 5E. HIPERCLOCKS CLK/NCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER WITH AC COUPLE

LVPECL CLOCK INPUT INTERFACE

The PCLK /nPCLK accepts LVPECL, CML, SSTL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 6A to 6E* show interface examples for the HiPerClockS PCLK/nPCLK input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

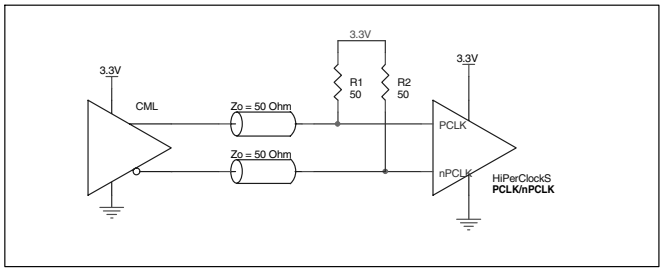


FIGURE 6A. HIPERCLOCKS PCLK/NPCLK INPUT DRIVEN BY A CML DRIVER

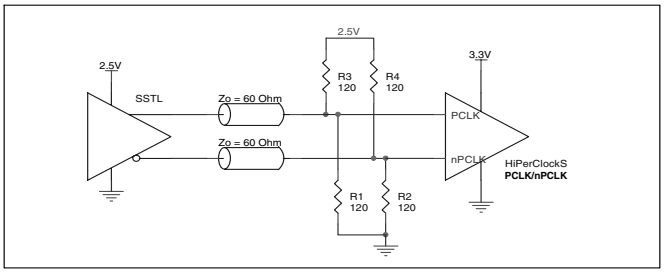


FIGURE 6B. HIPERCLOCKS PCLK/NPCLK INPUT DRIVEN BY AN SSTL DRIVER

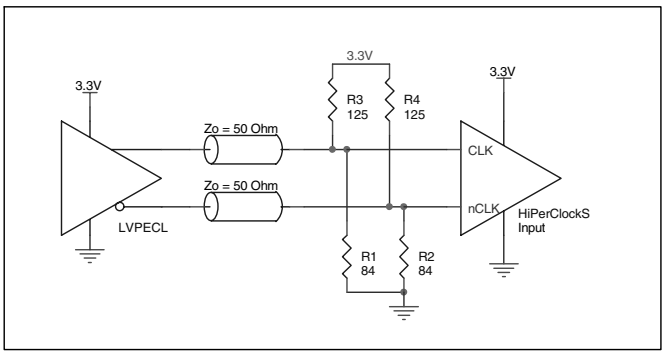


FIGURE 6C. HIPERCLOCKS PCLK/NPCLK INPUT DRIVEN BY A 3.3V LVPECL DRIVER

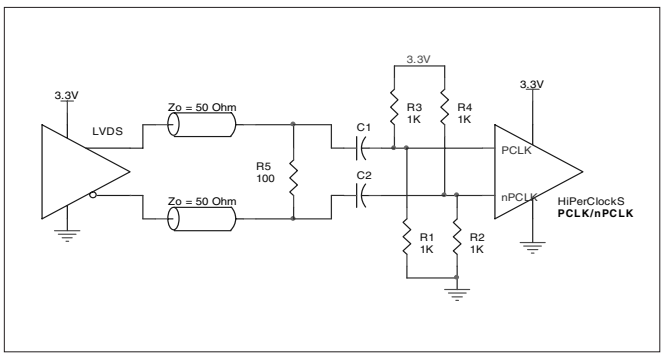


FIGURE 6D. HIPERCLOCKS PCLK/NPCLK INPUT DRIVEN BY A 3.3V LVDS DRIVER

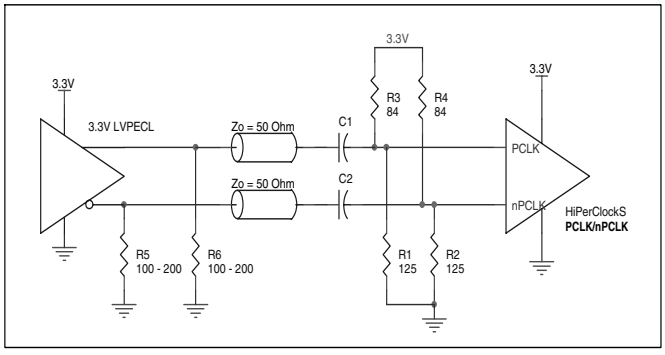


FIGURE 6E. HIPERCLOCKS PCLK/NPCLK INPUT DRIVEN BY A 3.3V LVPECL DRIVER WITH AC COUPLE

APPLICATION SCHEMATIC EXAMPLE

Figure 7 shows an example of ICS853031 application schematic. In this example, the device is operated at V_{CC}=3.3V. The decoupling capacitor should be located as close as possible to the power pin. The input is driven by a 3.3V LVPECL driver. Only two terminations examples are shown in this schematic. For more termination approaches, please refer to the LVPECL Termination Application Note.

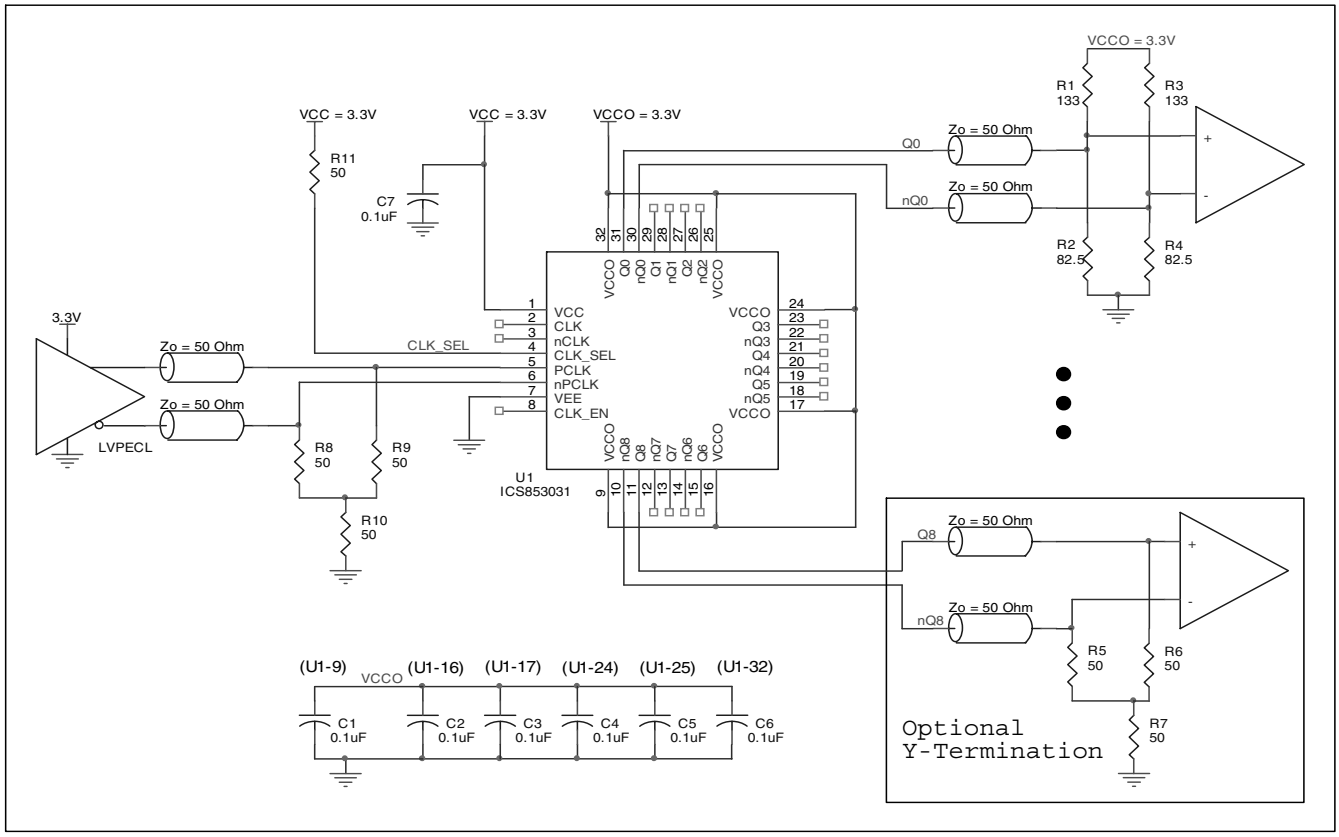


FIGURE 7. ICS853031 SCHEMATIC EXAMPLE

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS853031.
Equations and example calculations are also provided.

1. Power Dissipation.
The total power dissipation for the ICS853031 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.3V ± 5% = 3.465V, which gives worst case results.
NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power $(core)_{MAX} = V_{CC\_MAX} * I_{EE\_MAX}$ = 3.465V * 77mA = **266.8mW**
- Power $(outputs)_{MAX}$ = **30.2mW/Loaded Output pair**
  If all outputs are loaded, the total power is 9 * 30.94mW = **278.5mW**

Total Power$_{\_MAX}$ (3.465V, with all outputs switching) = 266.8mW + 278.5mW = **545.3mW**

2. Junction Temperature.
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 42.1°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:
85°C + 0.545W * 42.1°C/W = 108°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 6. THERMAL RESISTANCE θ_{JA} FOR 32-PIN LQFP FORCED CONVECTION

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	67.8°C/W	55.9°C/W	50.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 8.*

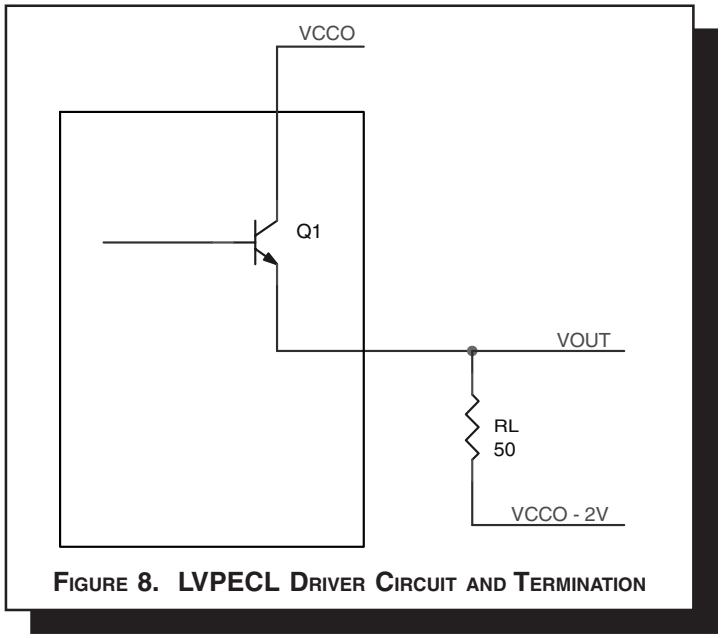


FIGURE 8. LVPECL DRIVER CIRCUIT AND TERMINATION

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CCO} - 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CCO\_MAX} - 0.935V}$

  $(V_{CCO\_MAX} - V_{OH\_MAX}) = \mathbf{0.935V}$

- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CCO\_MAX} - 1.67V}$

  $(V_{CCO\_MAX} - V_{OL\_MAX}) = \mathbf{1.67V}$

Pd_H is power dissipation when the output drives high.
Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) =$
$[(2V - 0.935V)/50\Omega] * 0.935V =$ **19.92mW**

$Pd\_L = [(V_{OL\_MAX} – (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) =$
$[(2V - 1.67V)/50\Omega] * 1.67V =$ **11.2mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **30.94mW**

RELIABILITY INFORMATION

TABLE 7. θ_{JA} VS. AIR FLOW TABLE FOR 32 LEAD LQFP

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	67.8°C/W	55.9°C/W	50.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS853031 is: 394

PACKAGE OUTLINE AND DIMENSIONS - Y SUFFIX FOR 32 LEAD LQFP

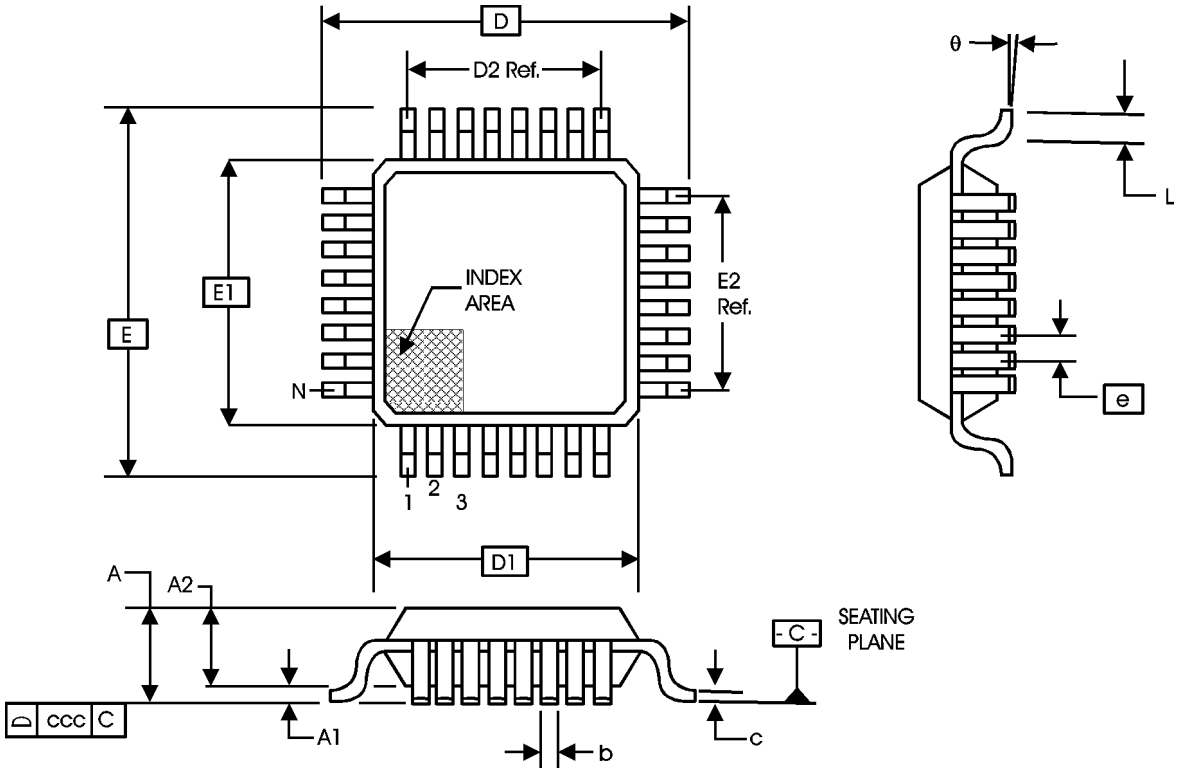


TABLE 8. PACKAGE DIMENSIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	BBA		
	MINIMUM	NOMINAL	MAXIMUM
N		32	
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
c	0.09	--	0.20
D		9.00 BASIC	
D1		7.00 BASIC	
D2		5.60 Ref.	
E		9.00 BASIC	
E1		7.00 BASIC	
E2		5.60 Ref.	
e		0.80 BASIC	
L	0.45	0.60	0.75
θ	0°	--	7°
ccc	--	--	0.10

Reference Document: JEDEC Publication 95, MS-026

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Count	Temperature
ICS853031AY	ICS853031AY	32 Lead LQFP	250 per tray	-40°C to 85°C
ICS853031AYT	ICS853031AY	32 Lead LQFP on Tape and Reel	1000	-40°C to 85°C
ICS853031AYLF	ICS853031AYL	32 Lead "Lead-Free" LQFP	250 per tray	-40°C to 85°C
ICS853031AYLFT	ICS853031AYL	32 Lead "Lead-Free" LQFP on Tape and Reel	1000	-40°C to 85°C

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REVISION HISTORY SHEET				
Rev	**Table**	**Page**	**Description of Change**	**Date**
B	T4B	4	LVCMOS Table - changed I_{IL} (CLK_SEL) from -10µA min. to -50µA min.	9/10/03
	T4C	4	Differential Table - change I_{IL} (CLK) from -10µA min. to -50µA min.	
	T4D	5	3.3V LVPECL Table - change V_{OH} @ 85° to 2.22V min. and 2.295V typical from 2.295V min. and 2.33V typical. Changed I_{IL} (PCLK) from -10µA min. to -50µA min.	
	T4E	5	2.5V LVPECL Table - change V_{OH} @ 85° to 1.42V min. and 1.495V typical from 1.495V min. and 1.53V typical.	
	T4F	6	ECL Table - change V_{OH} @ 85° to -1.08V min. and -1.005V typical from -1.005V min. and -0.97V typical.	
		9	Revised LVPECL Output Termination drawings.	
		12	Revised Figure 6D.	
B		13	Added Schematic Layout	8/19/04
B	2	T1	Pin Description Table - changed nCLK & nPCLK Type to Pullup (only).	9/16/04
	4	T4B	LVCMOS Table - added 2.625V in Test Conditions.	
	5	T4D & E	LVPECL DC Characteristics Tables - corrected Note 3.	
	6	T4F	ECL DC Characteristics Tables - corrected Note 3.	
	18	T9	Ordering Information Table - added Lead-Free part number.	