OKI semiconductor

MSM6222B-01

DOT MATRIX LCD CONTROLLER WITH 16 DOT COMMON DRIVER AND 40 DOT SEGMENT DRIVER

GENERAL DESCRIPTION

The OKI MSM6222B-01GS is a dot matrix LCD controller which is fabricated by low power CMOS silicon gate technology. In combination with 4-bit/8-bit microcontroller, character display on the dot matrix character type LCD can be effected. This LSI consists of 16 dot COMMON driver, 40 dot SEGMENT driver, DISPLAY RAM, character generator RAM, character generator ROM and control circuit.
Max. 80 characters' display can be controlled by MSM6222B-01GS by using together with the MSM5259GS.

The OKI MSM6222B-01GS has the same performance as HD44780. There is, however, slight differences between these two devices as described in the table on NEXT PAGE.

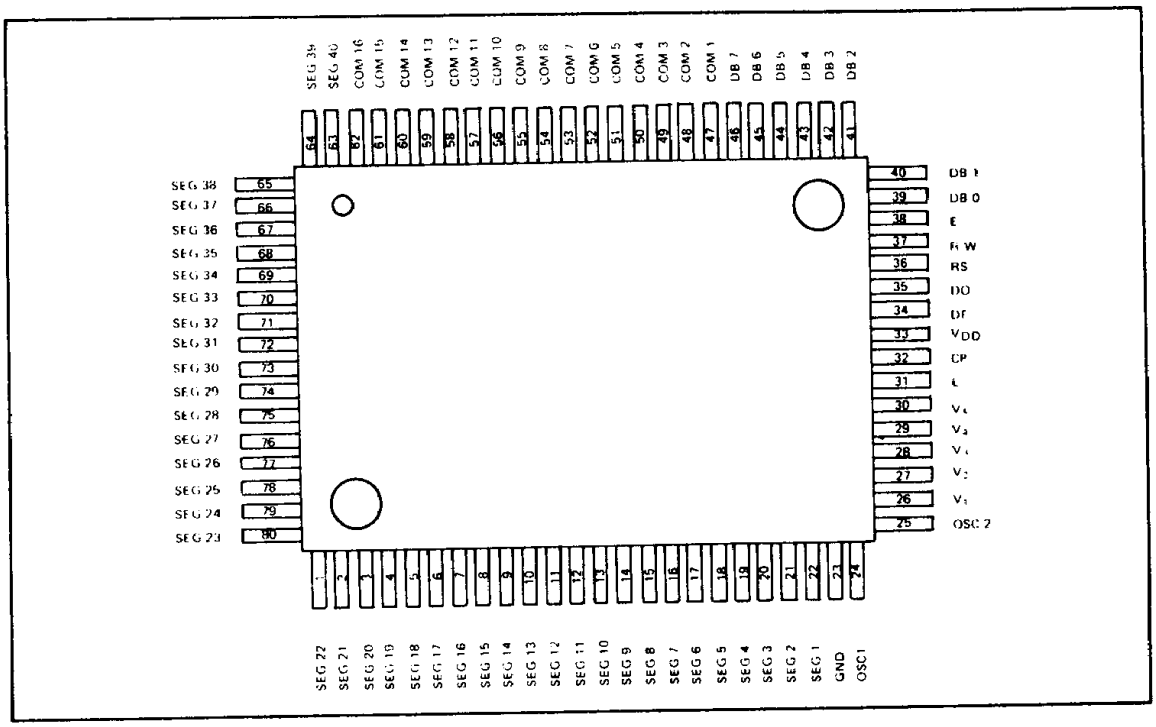
MSM6222B has ROM area for character code that can be programmed by custom mask. -01GS is the standard version with 160 characters, with small letter font 5 X 7, and 32 characters, with capital letter font 5 X 10, in this ROM area.

FEATURES

- Easy interface with an 8-bit or 4-bit microcontroller.
- Dot matrix LCD controller/driver for small letter font (5 X 7 dots) or capital letter font (5 X 10 dots).
- Automatic power ON reset.
- COMMON signal drivers (16) and SEGMENT signal drivers (40).
- Control up to 80 characters when used in combination with MSM5259GS.
- Character generator ROM for 160 characters with small letter font (5 X 7 dots) and 32 characters with capital letter font (5 X 10 dots).
- Character patterns can be programmable by CG RAM. (Small letter font: 8 kinds, 5 X 8 dots, Capital letter font: 4 kinds, 5 X 11 dots).
- Oscillation circuit for external register or ceramic resonator.
- 1/8 duty (1 line; 5 X 7 dots + cursor), 1/11 duty (1 line; 5 X 10 dots + cursor), or 1/16 duty (2 lines; 5 X 7 dots + cursor), selectable.
- Clear display even in case of 1/5 bias, 3.0V LCD driving voltage.
- 80 pin plastic QFP (QFP80-P-1420-L)
- 80 pin -VI plastic QFP (QFP80-P-1420-VIL)

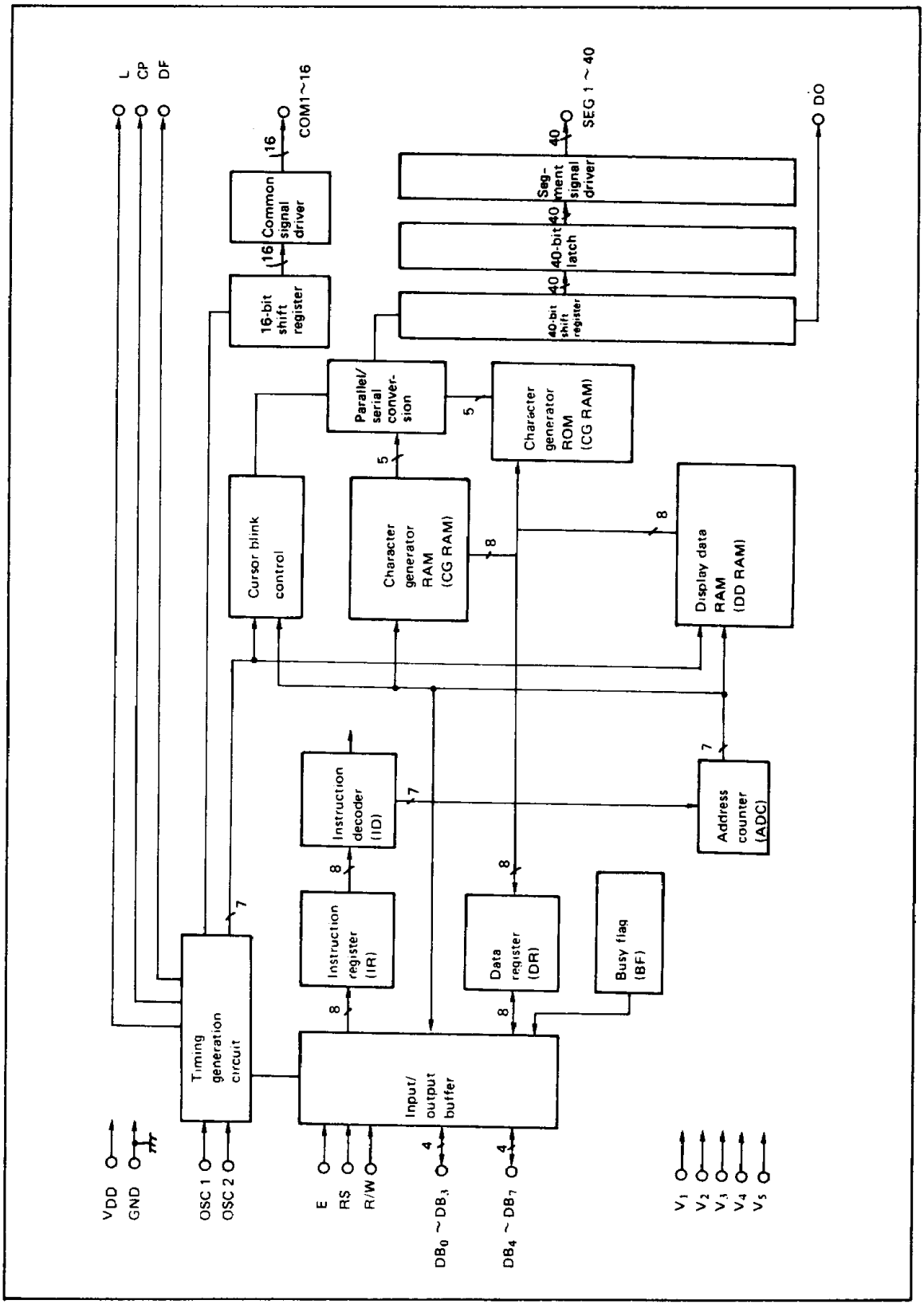
PIN CONFIGURATION

(Top View)



Item	HD44780	MSM6222B-01GS
LCD driving voltage 1/4 bias 1/5 bias	 3.0 ~ 11.0 (V) 4.6 ~ 11.0 (V)	 3.0 ~ 8.0 (V) 3.0 ~ 8.0 (V)
Bus interface speed with CPU	1 MHz (1000 ns)	1.5 MHz (667 ns) Signal rising/falling time is quite fast. So, the conduction between lines of the PCB and the cable assignment are very important.
The increment and decrement of the address counter in writing/reading the data to/from the CGRAM/DDRAM.	The address counter is incremented or decremented 6 μ sec (when f_{OSC} = 250 KHZ) after the busy condition is released. (Period of busy condition is 40 μs) So, the data cannot be written into/read out from the RAM for 6 μsec after the busy condition was over.	The address counter is incremented or decremented during the busy condition. So, data can be written into/read out from the RAM immediately after the busy condition was over.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATING

Parameter	Symbol	Condition	Limits	Unit	Applicable pin
Supply voltage	V_{DD}	T_a = 25°C	−0.3 ~ +7.0	V	V_{DD} − GND
Supply voltage for LCD displaying	V_1, V_2, V_3 V_4, V_5	T_a = 25°C	V_{DD} − 9.0 ~ V_{DD} + 0.3	V	V_1, V_2, V_3 V_4, V_5
Input voltage	V_{IN}	T_a = 25°C	−0.3 ~ V_{DD} + 0.3	V	R/W, RS, E, DB_0 ~ DB_7 OSC1
Permissible loss	P_D	—	500	mW	—
Storage temperature	T_{stg}	—	−55 ~ +125	°C	—
Operating temperature	T_{opr}	—	−20 ~ +75	°C	—

OPERATING RANGE

Parameter	Symbol	Condition	Limits	Unit	Applicable pin
Supply voltage	V_{DD}	–	4.5 ~ 5.5	V	V_{DD}
LCD driving voltage	V_{DD}−V_5 (3) (V_{LCD})	1/4 bias (1)	3.0 ~ 8.0	V	V_{DD}, V_5
		1/5 bias (2)	3.0 ~ 8.0	V	
Operating temperature	T_{opr}	–	−20 ~ +75	°C	–

(1) This voltage should be applied to $V_{DD} - V_5$.
Voltage applicable to V_1, V_2, V_3 and V_4 are as follows.

(2) $V_1 = V_{DD} - 1/4\ (V_{DD} - V_5)$
$V_2 = V_3 = V_{DD} - 1/2\ (V_{DD} - V_5)$
$V_4 = V_{DD} - 3/4\ (V_{DD} - V_5)$

(3) $V_1 = V_{DD} - 1/5\ (V_{DD} - V_5)$
$V_2 = V_{DD} - 2/5\ (V_{DD} - V_5)$
$V_3 = V_{DD} - 3/5\ (V_{DD} - V_5)$
$V_4 = V_{DD} - 4/5\ (V_{DD} - V_5)$

DC CHARACTERISTICS

(V_{DD} = 4.5 ~ 5.5V, T_a = −20 ~ +75°C)

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit	Applicable pin
"H" input voltage	V_{IH1}	–	2.2	–	V_{DD}	V	R/W, RS, E, DB_0 ~ DB_7
"L" input voltage	V_{IL1}	–	−0.3	–	0.6	V	
"H" input voltage	V_{IH2}	–	V_{DD} − 1.0	–	V_{DD}	V	OSC1
"L" input voltage	V_{IL2}	–	−0.3	–	1.0	V	
"H" output voltage	V_{OH1}	I_O = −0.205mA	2.4	–		V	DB_0 ~ DB_7
"L" output voltage	V_{OL1}	I_O = 1.2mA	–	–	0.4	V	
"H" output voltage	V_{OH2}	I_O = −40μA	0.9V_{DD}	–		V	DO, CP, L, DC, OSC2
"L" output voltage	V_{OL2}	I_O = 40μA	–	–	0.1V_{DD}	V	
COM voltage drop	V_C	I_O = ± 50μA Note 1	–	–	2.9	V	COM_1 ~ COM_{16}
SEG voltage drop	V_S	I_O = ± 50μA Note 1	–	–	3.8	V	SEG_1 ~ SEG_{40}
Input leak current	I_{IL}	V_{IN} = 0V	–	–	−1	μA	E
		V_{IN} = V_{DD}	–	–	1	μA	
"L" input current	I_{IL}	V_{DD} = 5.0V V_{IN} = 0V	−50	−125	−250	μA	R/W, RS
						μA	DB_0 ~ DB_7
"H" input current	I_{IH}	V_{IN} = V_{DD}	–	–	2	μA	

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit	Applicable pin
Current consumption (1)	I_{DD_1}	V_{DD} = 5.0V E = L level registor oscillator = 270KHz R/W, RS, and DB_0 to DB_7 are open. Output terminals are all no load. See Note 2.	–	0.35	0.6	mA	V_{DD}
Current consumption (2)	I_{DD2}	V_{DD} = 5V, ceramic oscillator. f_{OSC} = 250 KHz. E is in "L" level. R/W, RS, and DB_0 to DB_7 are open. Output terminals are all no load. See Note 2.	–	0.55	0.8	mA	V_{DD}
R_f clock oscillation frequency	f_{OSC}	R_f = 91 KΩ± 2% Note 3	175	300	350	KHz	OSC1 OSC2
Clock input frequency	f_{IN}	OSC 2 is open. Input from OSC1	125	250	350	KHz	OSC1
Input clock duty	f_{Duty}	Note 4	45	50	55	%	OSC1
Input clock rise time	t_{fr}	Note 5	–	–	0.2	μS	OSC1
Input clock fall time	t_{ff}	Note 5	–	–	0.2	μS	OSC1
Ceramic filter oscillation frequency	f_{OSC}	Rf = 500 kΩ $C_1 = C_2$ = 200 PF, Rd = 30 kΩ, and ceramic filter CSB250A. See Note 6.	245	250	255	KHz	OSC1 OSC2
LCD driving bias input voltage	V_{LCD}	Refer to the interface LCD.	3.0		8.0	V	$V_{DD} - V_5$ potential

(Note 1) Applied to the voltage drop (V_C) occuring from terminals V_{DD}, V_1, V_4, and V_5 to each COMMON terminal (COM1 to COM16) when 50 μA is flown in or out to and from all COM and SEG terminals, and also to voltage drop (V_S) occurring from terminals V_{DD}, V_2, V_3, and V_5 to each SEG terminal (SEG1 to SEG40).

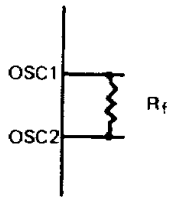
When output level is at V_{DD}, V_1, or V_2 level, 50 μA is flown out, while 50 μA is flown in when the output level is at V_3, V_4 or V_5 level.

This occurs when 5V or −3V is input to V_{DD}, V_1, and V_3 or to V_2, V_4, and V_5, respectively.

(Note 2) Applied to the current value flown in terminal V_{DD} when power is input as follows:

V_{DD} = 5V, GND = 0V, V_1 = 3.4V, V_2 = 1.8V, V_3 = 0.2V, V_4 = −1.4V, and V_2 = −3V.

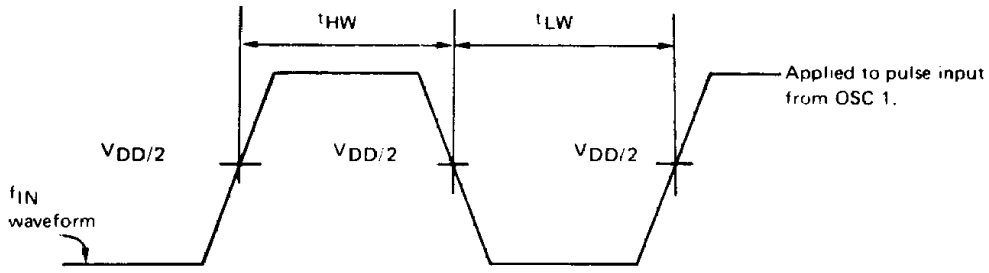
(Note 3)



R_f = 91 KΩ ± 2%

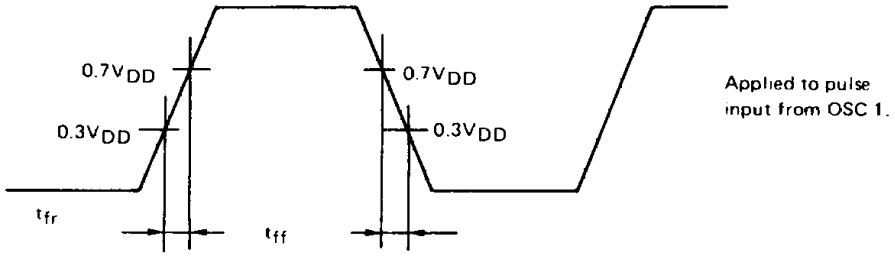
Minimum wiring is recommended between OSC 1 and R_f and between OSC 2 and R_f.

(Note 4)

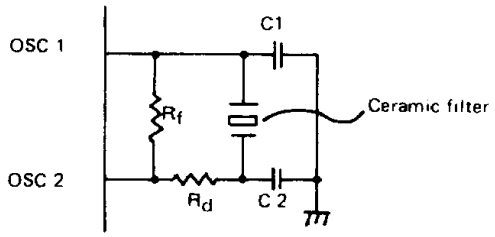


$f_{Duty} = t_{HW}/(t_{HW} + t_{LW}) \times 100$ (%)

(Note 5)



(Note 6)



Ceramic filter : CSB250D (MURATA SEISAKUSHO Works)
Rf : 510KΩ ± 10%
C1 = C2 : 200pF ± 10%
Rd : 30KΩ ± 5%

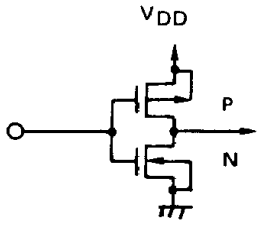
Please inform us when you use this circuit

(Note) Input the voltage listed in the table below to $V_1 - V_5$:

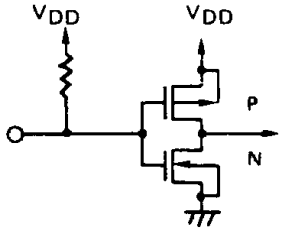
N (LCD line number) / Terminal	1-line mode	2-line mode
V_1	$V_{DD} - \frac{VLCD}{4}$	$V_{DD} - \frac{VLCD}{5}$
V_2	$V_{DD} - \frac{VLCD}{2}$	$V_{DD} - \frac{2VLCD}{5}$
V_3	$V_{DD} - \frac{VLCD}{2}$	$V_{DD} - \frac{3VLCD}{5}$
V_4	$V_{DD} - \frac{3VLCD}{4}$	$V_{DD} - \frac{4VLCD}{5}$
V_5	$V_{DD} - V_{LCD}$	$V_{DD} - V_{LCD}$

V_{LCD} is the LCD driving voltage. (For "N (LCD line number), refer to the initial set of the instruction code.)

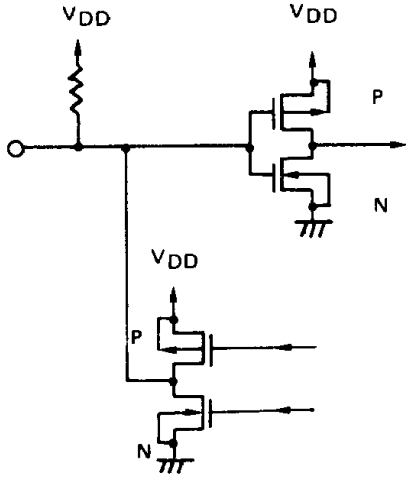
INPUT/OUTPUT CIRCUIT



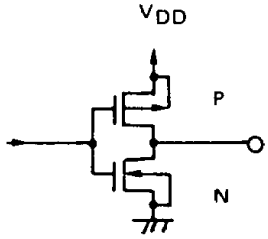
Applied to terminal E.



Applied to terminals R/W and RS.



Applied to $DB_0 - DB_7$.



Applied to DO, CP, L, and DF.

PIN DESCRIPTION

Pin Name	Function
R/W	Read/write selection input terminal. "H": Read, and "L": Write
RS	Register selection input terminal. "H": Data register, and "L": Instruction register
E	Input terminal for data input/output between CPU and MSM6222B-01GS and for instruction register activation.
$DB_0 \sim DB_7$	Input/output terminal for data send/receive between CPU and MSM6222B-01GS
OSC1, OSC2	Clock oscillating terminal required for internal operation upon receipt of the LCD drive signal and CPU instruction.
$COM_1 \sim COM_{16}$	LCD COMMON signal output terminal.
$SEG1 \sim SEG_{40}$	LCD SEGMENT signal output terminal.
DO	Output terminal to be connected to MSM5259GS to expand the number of characters to be displayed.
CP	Clock output terminal used when DO terminal data output shifts the inside of MSM5259GS.
L	Clock output terminal for the serially transfered data to be latched to MSM5259GS.
DF	The alternating signal (DF, display frequency) output pin.
V_{DD}	Power supply pin.
GND	Ground pin.
$V_1 \sim V_5$	Bias voltage input pin to drive the LCD.

FUNCTIONAL DESCRIPTION

1. Instruction Register (IR) and Data Register (DR)

These two registers are selected by the register selector (RS) terminal.
The DR is selected when the "H" level is input and IR when the "L" level is input.
The IR is used to store the address code and instruction code of the display data RAM (DD RAM) or character generator RAM (CG RAM).
The IR can be written into, but not be read out by the microcontroller (or CPU).
The DR is used to write into/read out the data to/from the DD RAM or CGRAM.
The data written to DR by the CPU is automatically written to the DD RAM or CG RAM as an internal operation.

When an address code is written to IR, the data (of the specified address) is automatically transferred from the DD RAM or CG RAM to the DR. By having the CPU subsequently read the DR (from the DR data), it is possible to verify DD RAM or CG RAM data.
After the writing of DR by the CPU, the DD RAM or CG RAM of the next address is selected to be ready for the next CPU writing.
Likewise, after the reading out of DR by the CPU, DD RAM or CG RAM data is read out by the DR to be ready for the next CPU reading.
Write/read to and from both registers is carried out by the READ/WRITE (R/W) terminal.

Table 1 Register and R/W terminals function table

R/W	RS	Function
L	L	IR write
H	L	Read of busy flag (BF) and address counter (ADC)
L	H	DR write
H	H	DR read

2. Busy Flag (BF)

When the busy flgag output is at "H", it indicates that the MSM6222B-01GS is engaged in internal operation.
When the busy flag is at "H" level, any new instruction is ignored.
When R/W = "H" and RS = "L", the busy flag is output from DB7.
New instruction should be input when BF is "L" level.
When the busy flag is set to "H", the output code of the address counter (ADC) cannot be fixed.

3. Address Counter (ADC)

The address counter (ADC) allocates the address for the DD RAM and CG RAM write/read and also for the cursor display.
When the instruction code for a DD RAM address or CG RAM address setting is input to IR, after deciding whether it is DD RAM or CG RAM, the address code is transferred from IR to ADC. After writing (reading) the display data to (from) the DD RAM or CG RAM, the ADC increments (decrements) by 1 as its internal operation.
The data of the ADC is output to DB0 – DB6 under the conditions that R/W = "H", RS = L, and BF = "L".

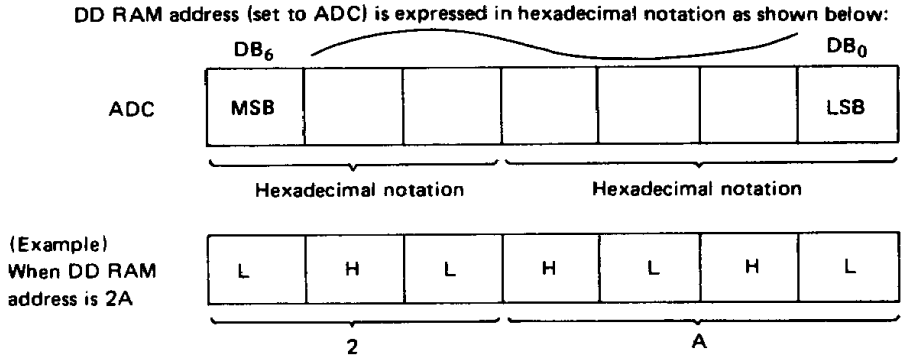
4. Timing Generator Circuit

This circuit is used to generate timing signals to activate internal operations upon receipt of CPU instruction and also from such internal circuits as the DD RAM, CG RAM, and CG ROM.
It is so designed that the internal operation caused by accessing from the CPU will not interfere with the internal operation caused by LCD display. Consequently, when data is written from the CPU to DD RAM no ill effect, e.g., flickering occurs in other than the display area where the data is written.
In addition, the circuit generates the transfer signal to MSM5259GS for display character expansion.

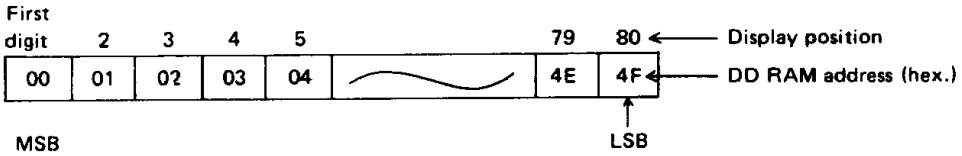
5. Display Data RAM (DD RAM)

This RAM is used to store display data of 8-bit character codes (see Table 2).
DD RAM address corresponds to the display position of the LCD. The coordination between the two is described in the following.

DD RAM address (set to ADC) is expressed in hexadecimal notation as shown below:



(1) Coordination between address and display position in the 1-line display mode



- When the MSM6222B-01GS is used alone, 8 characters max. can be displayed from the first digit to the eighth digit.

First digit	2	3	4	5	6	7	8
00	01	02	03	04	05	06	07

When the display is shifted by instruction, the coordination between the LCD display position and the DD RAM address changes as shown below:

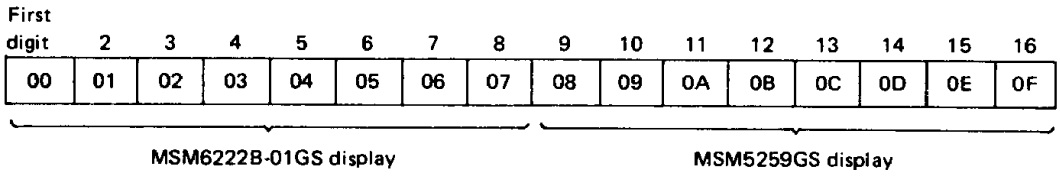
(Display shifted to right)

First digit	2	3	4	5	6	7	8
4F	00	01	02	03	04	05	06

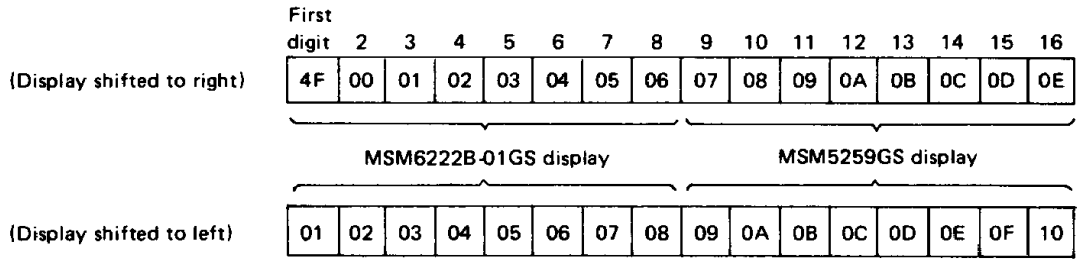
(Display shifted to left)

First digit	2	3	4	5	6	7	8
01	02	03	04	05	06	07	08

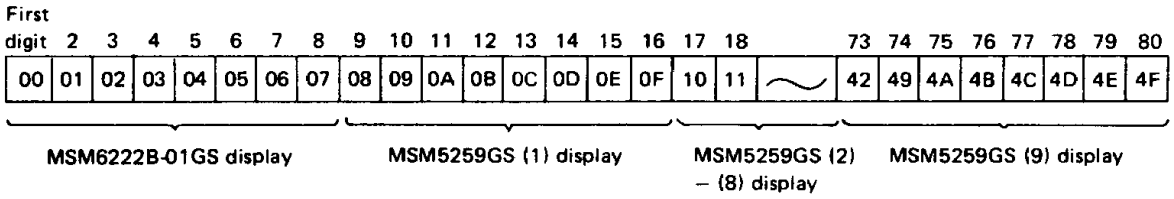
- When the MSM6222GS is used with one MSM5259GS, 16 characters max. can be displayed from the first digit to the sixteenth digit as shown below:



When the display is shifted by instruction, the coordination between the LCD display and DD RAM address changes as shown below:



- Since the MSM6222B-01GS has a DD RAM capacity for 80 characters, max. 9 pieces of MSM5259GS can be connected to MSM6222B-01GS so that 80 characters can be displayed.



(2) Coordination between address and display position in the 2-line display mode

	First digit	2	3	4	5		39	40 ← Display position
First line	00	01	02	03	04		26	27 ← DD RAM address (hex.)
Second line	40	41	42	43	44		66	67 ←

(Note) Note that the last address of the first line is not consecutive to the head address of the second line.

- When MSM6222B-01GS is ued alone, 16 characters (8 characters x 2 lines) max. can be displayed from the first digit to the eight digit.

	First digit	2	3	4	5	6	7	8
First line	00	01	02	03	04	05	06	07
Second line	40	41	42	43	44	45	46	47

When the display is shifted by instruction, the coordination between the LCD display position and the DD RAM address changes as shown below:

(Display shifted to right)

	First digit	2	3	4	5	6	7	8
First line	27	00	01	02	03	04	05	06
Second line	67	40	41	42	43	44	45	46

(Display shifted to left)

	First digit	2	3	4	5	6	7	8
First line	01	02	03	04	05	06	07	08
Second line	41	42	43	44	45	46	47	48

- When the MSM6222B-01GS is used with one MSM5259GS, 32 characters (16 characters x 2 lines) max. can be displayed from the first digit to the sixteenth digit.

	First digit	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
First line	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
Second line	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F

MSM6222B-01GS display　　MSM5259GS display

When the display is shifted by instruction, the coordination between the LCD display position and the DD RAM address changes as shown below:

(Display shifted to right)

	First digit	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
First line	27	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E
Second line	67	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E

MSM6222B-01GS display | MSM5259GS display

(Display shifted to left)

	First digit	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
First line	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10
Second line	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50

MSM6222B-01GS display | MSM5259GS display

- Since the MSM6222B-01GS has a DD RAM capacity for 80 characters, max. 4 pieces of MSM5259GS can be connected to the MSM6222B-01GS in the 2-line display mode.

	First digit	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18		33	34	35	36	37	38	39	40
First line	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11		20	21	22	23	24	25	26	27
Second line	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51		60	61	62	63	64	65	66	67

MSM6222B-01GS display | MSM5259GS (1) display | MSM5259GS (2) ~ (3) display | MSM5259 (4) display

6. Character Generator ROM (CG ROM)

The CG ROM is used to generate 5 X 7 dot (160 kinds) character patterns or 5 X 10 dot (32 kinds) character patterns from an 8-bit DD RAM character code signal.

The coordination between 8-bit character codes and character patterns is shown in Table 2.

When the 8-bit character code of a CG ROM is written to the DD RAM, the character pattern of the CG ROM corresponding to the code is displayed on the LCD display position corresponding to the DD RAM address.

Table 2 Table of correspondence for character codes and characters (character pattern)

Upper 4 BIT / Lower 4 BIT	MSB 0000	0010	0011	0100	0101	0110	0111	1010	1011	1100	1101	1110	1111
0000 LSB	CG RAM (1)		0	@	P	\	p					α	
0001	(2)	!	1	A	Q	a	q					ä	
0010	(3)	"	2	B	R	b	r					β	
0011	(4)	#	3	C	S	c	s					ε	
0100	(5)	$	4	D	T	d	t					μ	
0101	(6)	%	5	E	U	e	u					σ	
0110	(7)	&	6	F	V	f	v					ρ	
0111	(8)	'	7	G	W	g	w						
1000	(1)	(	8	H	X	h	x					√	
1001	(2)	)	9	I	Y	i	y						
1010	(3)	*	:	J	Z	j	z						
1011	(4)	+	;	K	[	k	{						
1100	(5)	,	<	L	¥	l	|						
1101	(9)	-	=	M	]	m	}						
1110	(7)	.	>	N	^	n	→						
1111	(8)	/	?	O	_	o	←						

7. Character Generator RAM (CG RAM)

The CG RAM is used to display user's original character patterns other than the CG ROM.

The CG RAM has the capacity (64 bytes = 512 bits) to write 8 kinds for 5 X 7 dots and 4 kinds for 5 X 10 dots.

When displaying character patterns stored in the CG RAM, write 8-bit character codes (00–07 or 02 to 0F; hex.) on the left side as shown in Table 2. It is then possible to output the character pattern to the LCD display position corresponding to the DD RAM address.

The following is a description on how to write and read character patterns to and from the CG RAM.

(1) When the character pattern is 5 X 7 dots (See Table 3-1).

- **A method to write character pattern into CG RAM by CPU:**

  Three bits of CG RAM address 0–2 correspond to the line position of the character pattern.

  First, set increment or decrement by the CPU, and then input the CG RAM address.

  After this, write character pattern codes into CG RAM through $DB_0 \sim DB_7$ line by line.

  DB_0 to DB_7 correspond to CG RAM data 0–7 in Table 3-1.

  It is displayed when "H" is set as input data and is not display when "L" is set as input data.

  Since the ADC is automatically incremented or decremented by 1 after the writing of data to the CG RAM, it is not necessary to set the CG RAM address again.

  The line, the CG RAM address 0–2 of which are all "H" ("7" in hexadecimal notation), is the cursor position. It is ORed with the cursor at the cursor position and displayed to LCD.

  For this reason, it is necessary to set all input data that become cursor positions to "L".

  Although CG RAM data 0–4 bit are output to the LCD as display data, CG RAM data bit 5–7 are not. The latter can be written and read to and from the RAM, it is therefore allowed to be used as data RAM.

  Accordingly, it is necessary to set all input data which become cursor positions to "H".

  0–4 bit of CG RAM data are output to the LCD as the display data, however, 5–7 bit of CG RAM data are not. But it can be used as RAM because data can be written/read into/from it.

- **A method to display the CG RAM character pattern to the LCD:**

  The CG RAM is selected when 4-upper order bits MSB of the character code are all "L".

  As character code bit 3 is invalid, the display of "O" in Table 3-1, is selected by character code "00" (hex.) or "08" (hex.).

  When the 8-bit character code of the CG RAM is written to the DD RAM, the character pattern of the CG RAM is displayed on the LCD display position corresponding to the DD RAM address. (DD RAM data, bit 0–2 correspond to CG RAM address, bit 3–5.)

(2) When character pattern is 5 x 10 dots (See Table 3-2)

- **A method to write character pattern into the CG RAM by the CPU**

  Four bits of CG RAM address, bit 0–3, correspond to the line position of the character pattern.

  First, set increment or decrement by the CPU, and then input the address of the CG RAM.

  After this, write the character pattern code into the CG RAM, line by line from DB_0–DB_7.

  DB_0 to DB_7 correspond to CG RAM data, bit 0–7, in Table 3-2.

  It is displayed when "H" is set as the input data, while it is not displayed when "L" is set as the input data.

  As the ADC is automatically incremented or decremented by 1 after the writing of data to the CG RAM, it is not necessary to set the CG RAM address again.

  The line in which the CG RAM address 0 to 3 is "A" (hex) is ORed with cursor at the cursor position and displayed on the LCD.

  When the CG RAM data, bit 0–4, CG RAM address, bit 0–3, is "0" ~ "A", it is displayed on the LCD as the display data. When the CG RAM data, bit of 5–7, and CG RAM, bit data is 0–4 and CG RAM address data is "B" ~ "F", it is not output to the LCD.

  But in this case, CG RAM can be used as RAM and it can be written into/read out. So, it can be used as the data RAM.

- **A method to display the CG RAM character pattern to the LCD:**

  The CG RAM is selected when 4-upper order bits MSB of the character code are all "L".

  As MSB and LSB of character code LSD are invalid, the display of "year" 年 in Kanji character is selected by character codes "00", "01", "08", and "09" (hex.) as in Table 3-2.

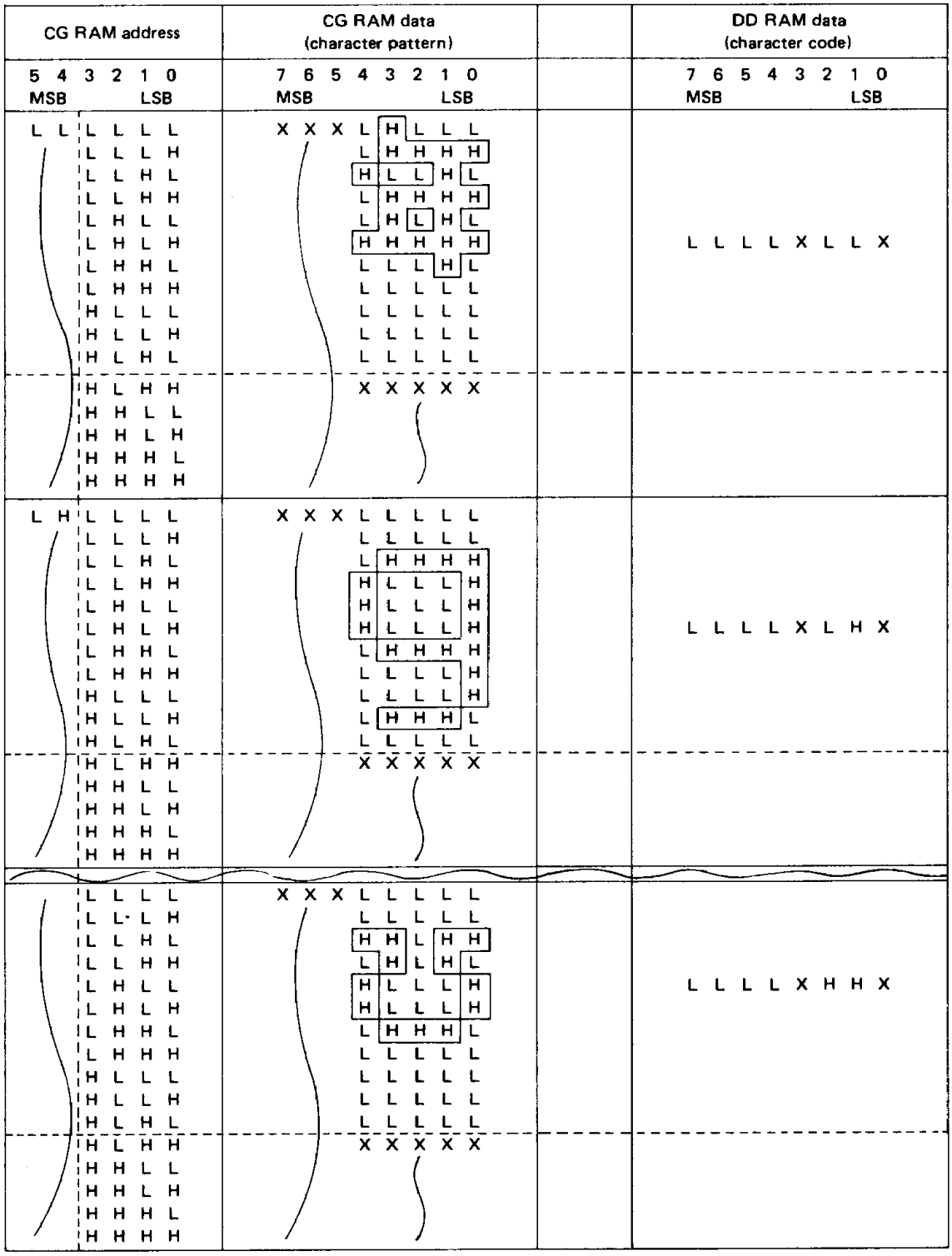
  When the CG RAM character code is written to the DD RAM, the CG RAM character pattern is displayed on the LCD display position corresponding to the DD RAM address.

  (DD RAM data bit 1, 2 correspond to CG RAM address bit 4, 5.)

CG RAM address	CG RAM data (character pattern)		DD RAM data (character code)
5 4 3 2 1 0 MSB LSB	7 6 5 4 3 2 1 0 MSB LSB		7 6 5 4 3 2 1 0 MSB LSB
L L L L L L L L H L H L L H H H L L H L H H H L H H H L L H L L L	X X X L H H H L H L L L H H L L L H H L L L H H L L L H H L L L H L H H H L L L L L L X X X H L L L H		L L L L X L L L
L L H L H L L H H H L L H L H H H L H H H	H L L H L H L H L L H H L L L H L H L L H L L H L H L L L H L L L L L		L L L L X L L H
H H H L L L L L H L H L L H H H L L H L H H H L H H H	X X X L H H H L L L H L L L L H L L L L H L L L L H L L L L H L L L H H H L L L L L L		L L L L X H H H

X: Irrespective of H/L

Table 3-1 Relation between CG RAM data (character pattern) vs. CG RAM address and DD RAM data vs. character pattern when the caracter pattern is 5 X 7 dots. Above example indicate "OKI".

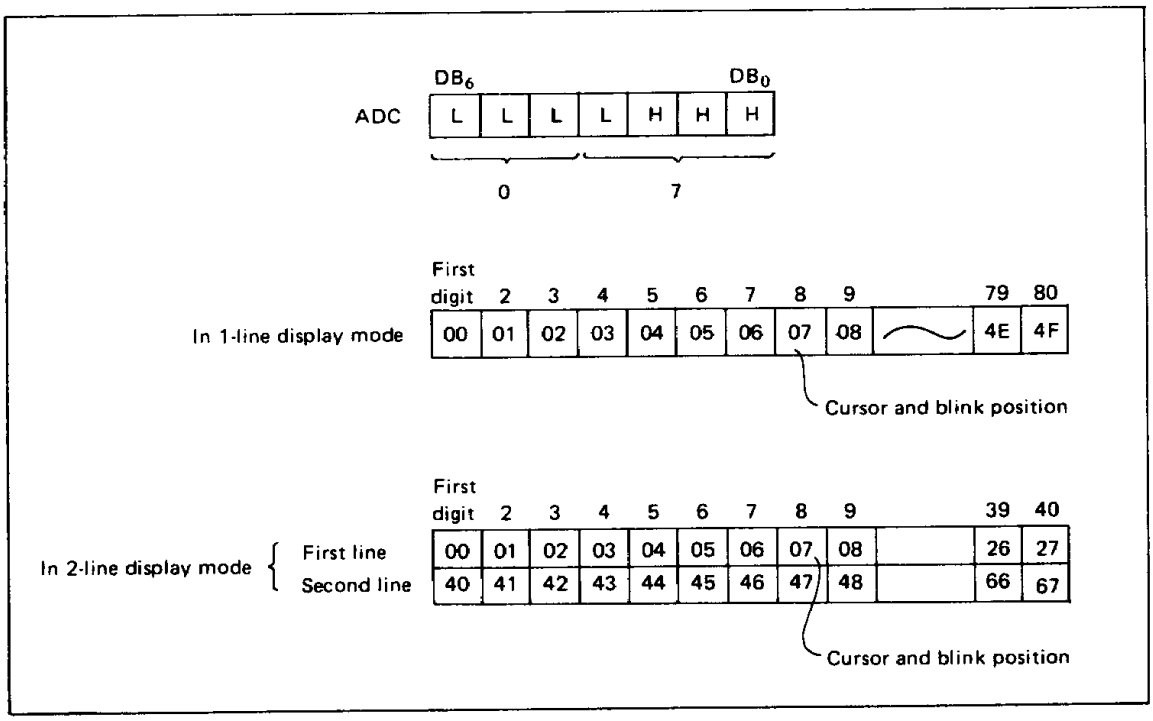


X: Irrespective of H/L

Table 3-2 Relation between CG RAM dada (character pattern) example vs. CG RAM address and DD RAM data vs. character pattern when the character pattern is 5 X 10 dots. Above examples indicate 年 , g, v respectively.

8. Cursor/Blink Control Circuit:

This is a circuit that generates the LCD cursor and blink.
This circuit is under the control of the CPU program.
The display of the cursor and blink on the LCD is made at a position corresponding to the DD RAM address set to the ADC.
The figure below shows an example of the curson/blink position when the value of ADC is set at "07" (hex.).



(Note) The cursor and blink are displayed even when the CG RAM address is set to ADC.
For this reason, it is necessary to inhibit the cursor and blink display while the CG RAM address is set to the ADC.

9. LCD Display Circuit (COM 1 to 16, SEG 1 to 40, L, CP, DO, and DF):

As the MSM6222B-01GS provides the COM signal outputs (16 pcs.) and the SEG signal outputs (40 pcs.), it can display 8 characters (1-line display) or 16 characters (2-line display) as a unit.
The SEG1 ~ SEG40 are used to display 8 digit display on the LCD. To expand the display, an MSM5259GS is used.
The MSM5259GS, 40 dot segement driver, is used for expansion of the SEG signal output.
Interface with the MSM5259GS is made through data output terminal (DO), clock output terminal (CP), latch output terminal (L), and display frequency terminal (DF). The character pattern data is serially transferred to MSM5259GS through DO and CP. When the data of 72 characters 360-bit (= 5-bit/ch. x 72 ch. = 1-line display) or 32 characters 160-bit (5-bit/ch. x 32 ch. = 2-line display) is output, the latch pulse is also output through terminal L. By this latch pulse, the data transferred serially to MSM5259GS is latched to be used as display data. The display frequency signal (DF) required when LCD is displayed is also synchronously output from DF terminal with this latch pulse.

10. Built-in Reset Circuit

The MSM6222B-01GS is automatically initialized when the power is turned on.
During initialization, the busy flag (BF) holds "H" and does not accept instructions (other than the busy flag read).
The busy flag goes to "H" for 15 ms after V_{DD} reaches 4.5V or more.
During initialization, the MSM6222B-01GS executes the following instructions:

- Display clear
- Data length of interface with CPU: 8 bits (8B/4B = H)
- LCD: 1-line display (N = L)
- Character font: 5 x 7 dots (F = L)
- ADC: Increment (I/D = H)
- No display shift (SH = L)
- Display: Off (DI = L)
- Cursor: Off (C = L)
- No blink (B = L)

When the built-in reset circuit is used, it is required to satisfy the following power supply conditions. As the built-in reset circuit does not operate normally unless these power supply conditions are met; initialize the MSM6222B-01GS by instruction through the CPU (refer to initialize instruction).
When a battery is used as supply voltage source, it is required to initialize the instruction.

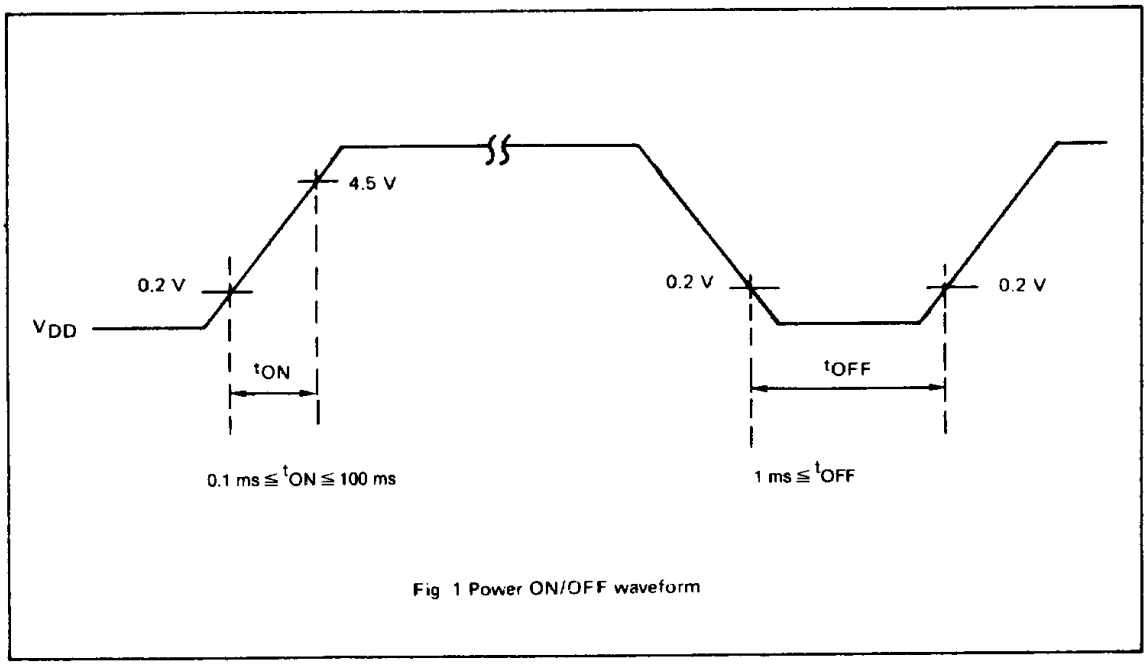


Fig 1 Power ON/OFF waveform

11. Data Bus with CPU

The data bus with CPU is available either once for 8 bits or twice for 4 bits allowing the MSM6222B-01GS to be interfaced with either an 8-bit or 4-bit CPU.

(1) When the interface data length is 8 bits

Data buses DB0 to DB7 (8 pcs.) are all used and data input/output is carried out simultaneously.

(2) When the interface data length is 4 bits

The 8-bit data input/output is carried out in two steps by using only 4-high order bits of data buses DB4 to DB7 (4 pcs.).

The first time data input/output is made for 4-high order bits (DB4 to DB7 when the interfaces data length is 8 bits) and the second time data input/output is made for 4-low order bits (DB0 to DB3 when the interface data length is 8 bits). Even when the data input/output can be completely made through 4-high order bits, be sure to make another input/output of 4-low order bits. (Example: Busy flag Read)
Since the data input/output is carried out in two steps but as one execution, no normal data transfer is executed from the next input/output if accessed only once.

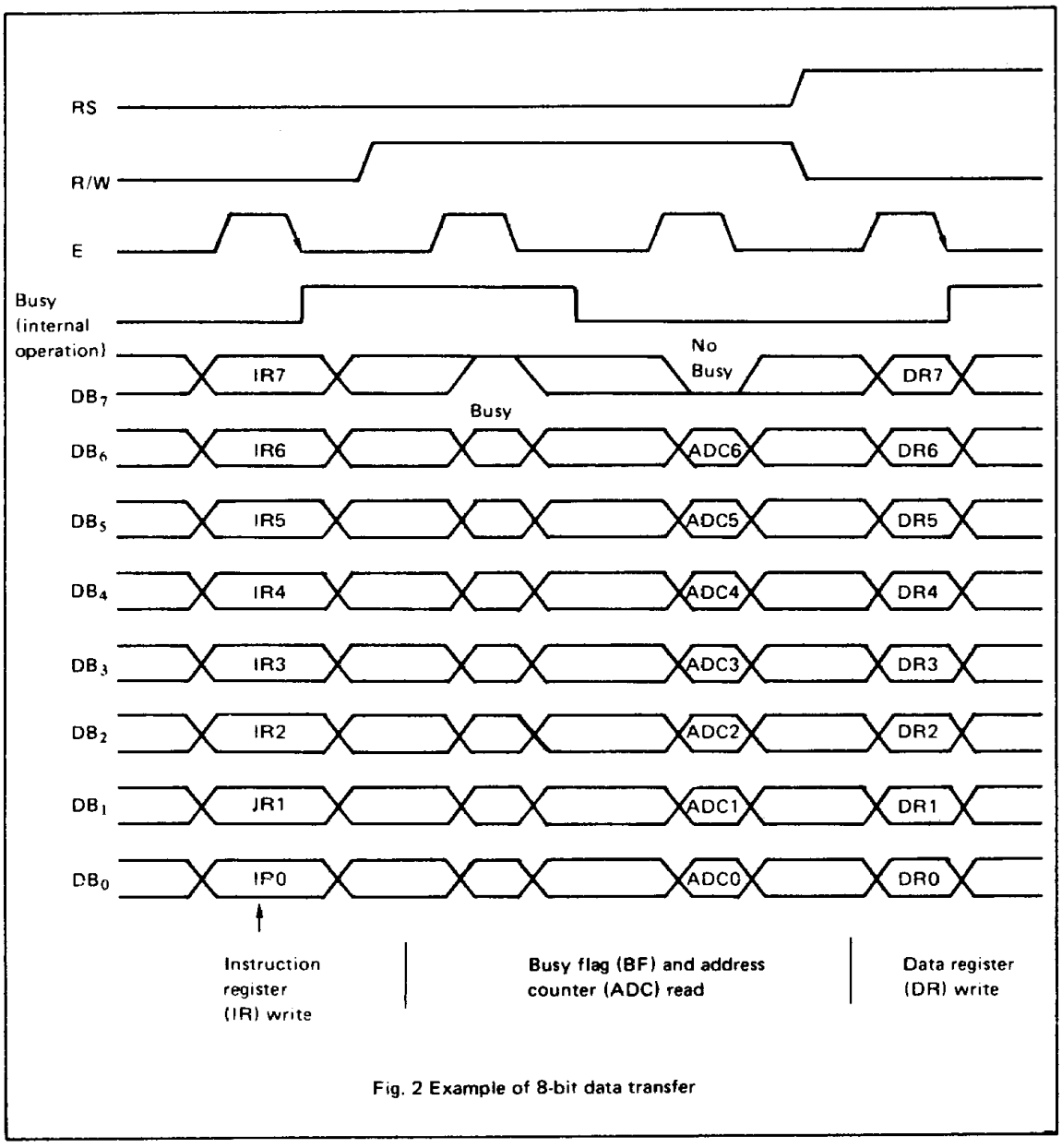


Fig. 2 Example of 8-bit data transfer

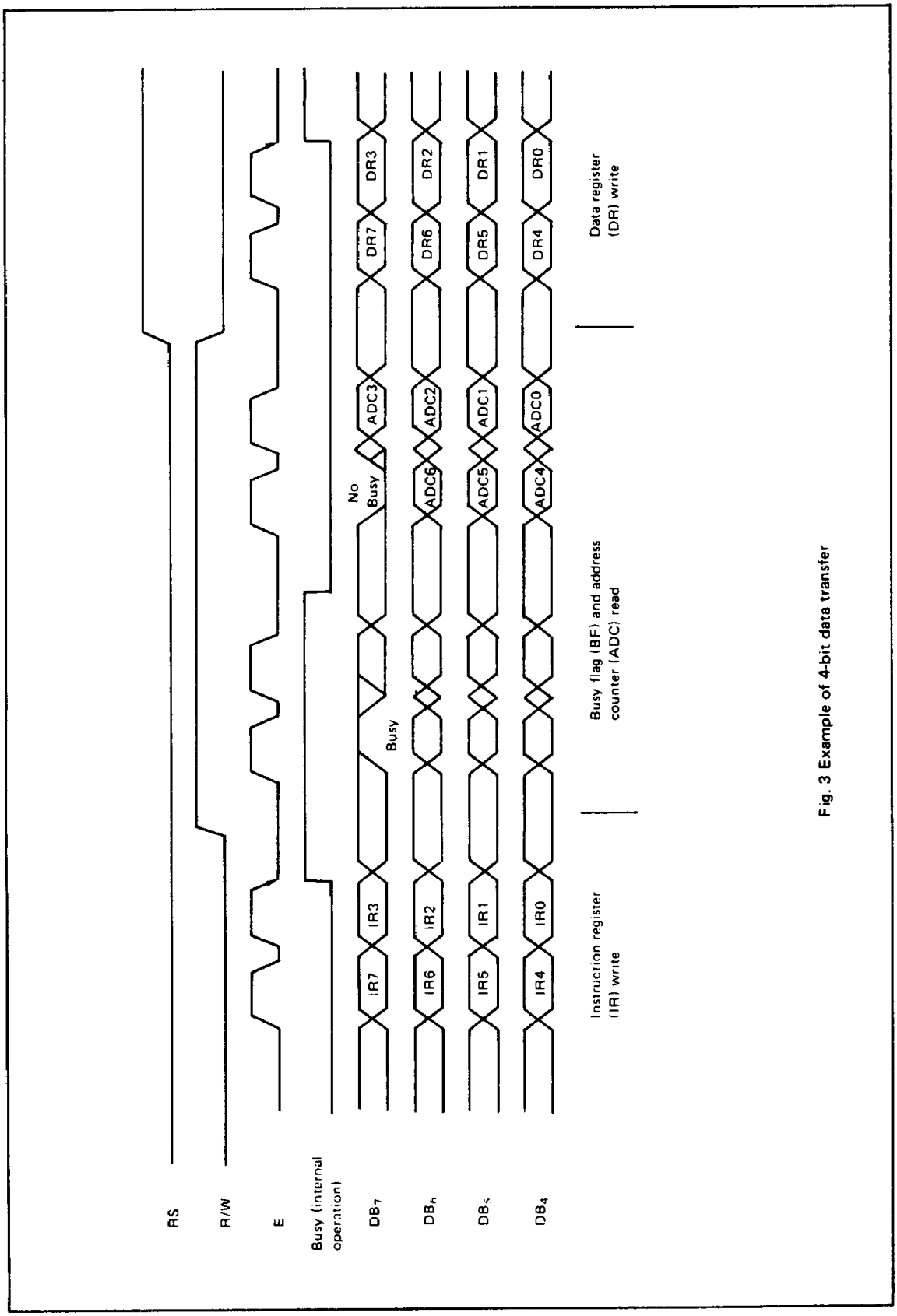


Fig. 3 Example of 4-bit data transfer

12. Instruction Code

The instruction code is defined as the signal through which the MSM6222B-01GS is accessed by the CPU. CPU.

The MSM6222B-01GS begins operation upon receipt of the instruction code input.

As the internal processing operation of MSM6222B-01GS is started with a timing that does not affect the LCD display, the busy status continues longer than the CPU cycle time.

Under the busy status (when the busy flag is set to "H"), the MSM6222B-01GS does not execute any instructions other than the busy flag read.

Therefore, the CPU has to verify that the busy flag is set to "L" prior to the input of the instruction code.

(1) Display clear:

	R/W	RS	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Instruction code	L	L	L	L	L	L	L	L	L	H

When this instruction is executed, the LCD display is cleared.

When the cursor and blink are in display, the blinking position moves to the left end of the LCD (the left end of the first line in the 2-line display mode).

(Note) All DD RAM data goes to "20" (hex.), while the address counter (ADC) goes to "00" (hex.). The execution time, when the OSC oscillation frequency is 250 KHz is 1.64 ms (max.).

(2) Cursor home

	R/W	RS	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Instruction code	L	L	L	L	L	L	L	L	H	X

X: Irrespective of H/L

When this instruction is executed, the blinking position moves to the left end of the LCD (to the left end of the first line in the 2-line display mode) when the cursor and blink are being displayed.

When the display is in shift, the display returns to its original position before shifting.

(Note) The address counter (ADC) goes to "00" (hex.). The execution time, when the OSC oscillation frequency is 250 KHz, is 1.64 ms (max.).

(3) Shift mode set

	R/W	RS	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Instruction code	L	L	L	L	L	L	L	H	I/D	SH

① When the I/D is set, the 8-bit character code is written or read to and from the DD RAM, the cursor and blink shift to the right by 1 character position (I/D = H; increment) or to the left by 1 character position (I/D = L; decrement).

The address counter is incremented (I/D = H) or decremented (I/D = L) by 1 at this time.

Even after the character pattern code is written or read to and from the CG RAM, the address counter (ADC) is incremented (I/D = H) or decremented (I/D = L) by 1.

② When SH = H is set, the character code is written to the DD RAM, and then the cursor and blink stop and the entire display shifts to the left (I/D = H) or to the right (I/D = L) by 1 character position.

When the character is read from the DD RAM when SH = H is set, or when the character pattern data is written or read to or from the CG RAM when SH = H is set, the entire display does not shift, but normal write/read is performed (the entire display does not shift, but the cursor and blink shift to the right (I/D = H) or to the left (I/D = L) by 1 character position.

When SH = L is set, the display does not shift, but normal write/read is performed.

The execution time when the OSC oscillation frequency is 250 KHz is 40 μs.

(4) Display mode set

	R/W	RS	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Instruction code	L	L	L	L	L	L	H	DI	C	B

① The DI bit controls whether the character pattern is displayed or extinguished.
When DI is "H", this bit makes the LCD display the character pattern.
When DI is "L", this bit distinguishes the LCD character pattern. The cursor and blink are also cancelled at this time.
(**Note**) Different from the display clear, the character code is absolutely not rewritten.

② The cursor goes off when C = L and it is displayed when DI = H and C = H.

③ The blink is cancelled when B = L and it is executed when DI = H and B = H.
In the blink mode, all dots (including the cursor), displaying character pattern, and cursor are displayed alternately at 409.6 ms (in 5 X 7 dots character font) or 563.2 ms (in 5 X 10 dots character font) when the OSC oscillation frequency is 250 KHz. The execution time when the OSC oscillation frequency is 250 KHz is 40 μs.

(5) Cursor and display shift

	R/W	RS	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Instruction code	L	L	L	L	L	H	D/C	R/L	X	X

X: Irrespective of H/L

When D/C = L and R/L = L, the cursor and blink position are shifted to the left by 1 character position (ADC is then decremented by 1).
When D/C = L and R/L = H, the cursor and blink position are shifted to the right by 1 character position (ADC is then incremented by 1).
When D/C = H and R/L = L, the entire display is shifted to the left by 1 character position. The cursor and blink positions are also shifted with the display (ADC remains unchanged).
When D/C = H and R/L = H, the entire display is shifted to right by 1 character position. The cursor and blink positions are also shifted with the display (ADC remains unchanged).
In the 2-line display mode, the cursor and blink positions are shifted from the first line to the second line when the cursor is shifted to the right next to the fortieth digit (27; hex.) in the first line. No such shifting is made in other cases.
When shifting the entire display, the display pattern, cursor, and blink positions are in no case shifted between lines (from the first line to the second line or vice versa).
The execution time when the OSC oscillation frequency is 250 KHz is 40 μs.

(6) Initial set

	R/W	RS	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Instruction code	L	L	L	L	H	8B/4B	N	F	X	X

X: Irrespective of L/O

① When 8B/4B = H, the data input/output to and from the CPU is carried out simultaneously by means of 8 bits DB7 to DB0.
When 8B/4B = L, the data input/output to and from the CPU is carried out in two steps through of 4 bits DB7 to DB4.

② The 2-line display mode of the LCD is selected when N = H, while the 1-line display mode is selected when N = L.

③ The 5 X 7 dots character font is selected when F = L, while the 5 X 10 dots character font is selected when F = H and N = L.

This initial set has to be accessed prior to other instructions excepting the busy flag read after powering ON the MSM6222B-01GS.

N	F	Number of display lines	Character font	Duty ratio	Number of biases	Number of COMMON signals
L	L	1-line	5 X 7 dots	1/8	4	8
L	H	1-line	5 X 10 dots	1/11	4	11
H	L	2-line	5 X 7 dots	1/16	5	16
H	H	2-line	5 X 7 dots	1/16	5	16

Generate biases externally and input them to the MSM6222B-01GS (V_{DD}, V1, V2, V3, V4, and V5).
When the number of biases is 4, input the same potential to V2 and V3. The execution time, when the OSC oscillation frequency is 250 KHz, is 40 μs.

(7) CG RAM address set

	R/W	RS	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Instruction code	L	L	L	H	C_5	C_4	C_3	C_2	C_1	C_0

When CG RAM addresses, bit C_5 to C_0 (binary), are set, the CG RAM is specified, until the DD RAM address is set.
Write/read of the character pattern to and from the CPU begins with addresses, bit C_5 to C_0, starting from CG RAM selection.
The execution time, when the OSC oscillation frequency is 250 KHz, is 40 μs.

(8) DD RAM address set

	R/W	RS	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Instruction code	L	L	H	D_6	D_5	D_4	D_3	D_2	D_1	D_0

When the DD RAM addresses D6 to D0 (binary) are selected, the DD RAM is specified until the DD RAM address is set.
Write/read of the character code to and from the CPU begins with addresses D_6 to D_0 starting from DD RAM selection.
In the 1-line display mode (N = H), however, D_6 to D_0 (binary) must be set to one of the values among "00" to "4F" (hex.).

Likewise, in the 2-line mode, D_6 to D_0 (binary) must be set to one of the values among "00" ~ "27" (hex.) or "40" – "67" (hex.).
When any value other than the above is input, it is impossible to make a normal write/read of character codes to and from the DD RAM.
The execution time, when the OSC oscillation frequency is 250 KHz, is 40 μs.

(9) DD RAM and CG RAM data write

	R/W	RS	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Instruction code	L	H	E_7	E_6	E_5	E_4	E_3	E_2	E_1	E_0

When E7 to E0 (binary) codes are written to the DD RAM or CG RAM, the cursor and display move as described in "(5) Cursor and display shift". The execution time, when the OSC oscillation frequency is 250 KHz, is 40 μs.

(10) Busy flag and address counter read

	R/W	RS	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Instruction code	H	L	BF	0_6	0_5	0_4	0_3	0_2	0_1	0_0

The busy flag (BF) is output by this instruction to indicate whether the MSM6222B-01GS is engaged in internal operations (BF = "H") or not (BF = "L").
When BF = "H", no new instruction is accepted. It is therefore necessary to verify BF = "L" before inputting a new instruction.
When BF = "L", a correct address counter value is output. The address counter value must match the DD RAM address or CG RAM address. The decision of whether it is a DD RAM address or CG RAM address is made by the address previously set.
Since the address counter value when BF = "H" is sometimes incremented or decremented by 1 during internal operations, it is not always a correct value.
Execution time is 1 μs.

(11) DD RAM and CG RAM data read

	R/W	RS	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Instruction code	H	H	P_7	P_6	P_5	P_4	P_3	P_2	P_1	P_0

Character codes (bit P_7 to P_0) are read from the DD RAM, while character patterns (P7 to P0) from the CG RAM.
Selection of DD RAM or CG RAM is decided by the address previously set.
After reading those data, the address counter (ADC) is incremented or decremented by 1 as set by the shift mode mentioned in item "(3) shift mode set".
The execution time, when the OSC oscillation frequency is 250 KHz, is 40 μs.

(Note) Conditions for the reading of correct data:

1. When the DD RAM address set or CG RAM address set is input before inputting this instruction.
2. When the cursor/display shift is input before inputting this instruction in case the character code is read.
3. Data after the second reading from RAM when read more than 2 times. Correct data is not output in any other case.

13. Instruction Initialization

(1) When data input/ouput to and from the CPU is carried out by 8 bits (DB0 to DB7):

① ● Turn on the power
② ● Wait for 15 ms or more after V_{DD} has reached 4.5V or more.
③ ● Set 8B/4B at H by initial reset of instruction.
④ ● Wait for 4.1 ms or more.
⑤ ● Set 8B/4B at H by initial reset of instruction.
⑥ ● Wait for 100 μs or more.
⑦ ● Set 8B/4B at H by initial reset of instruction.
⑧ ● Check the busy flag as No Busy.
⑨ ● Set 8B/4B at H. Set LCD line number (N) and character font (F).
(After this, do not change the LCD line number and character font.)
⑩ ● Check No Busy.
⑪ ● Clear the display by setting the display mode.
⑫ ● Check No Busy.
⑬ ● Clear the display.
⑭ ● Check No Busy.
⑮ ● Set the shift mode.
⑯ ● Check No Busy.
⑰ ● Initialization completed.

Example of Instruction Code for Steps ③, ⑤, and ⑦.

R/W	RS	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
L	L	L	L	H	H	X	X	X	X

X: Irrespective of H/L

(2) When data input/output to and from the CPU is carried out by 4 bits (DB4 to DB7):

① ● Turn on the power.
② ● Wait for 15 ms or more after V_{DD} has reached 4.5V or more.
③ ● Set 8B/4B at H by initial reset of instruction.
④ ● Wait for 4.1 ms or more.
⑤ ● Set 8B/4B at H by initial reset of instruction.
⑥ ● Wait for 100 μs or more.
⑦ ● Set 8B/4B at H by initial reset of instruction.
⑧ ● Check the busy flag as No Busy.
⑨ ● Set 8B/4B at L. Set LCD line number (N) and character font (F).
⑩ ● Check No Busy.
⑪ ● Set 8B/4B at L. Set LCD line number (N) and character font (F).
⑫ ● Check No Busy.
⑬ ● Clear the display by setting the display mode.
⑭ ● Check No Busy.
⑮ ● Clear the display.
⑯ ● Check No Busy.
⑰ ● Set the shift mode.
⑱ ● Check No Busy.
⑲ ● Initialization completed.

Example of Instruction Code for Steps ③, ⑤, and ⑦.

R/W	RS	DB_7	DB_6	DB_5	DB_4
L	L	L	L	H	H

Example of Instruction Code for Step ⑨.

R/W	RS	DB_7	DB_6	DB_5	DB_4
L	L	L	L	H	L

LCD DRIVE WAVEFORM

Figures 4, 5 and 6 show the LCD driving waveform consists of COM signal, SEG signal DF signal and L (latch pulse waveform) signal, in the duty of 1/8, 1/11 and 1/16 respectively.

The relation between duty and frame frequency is described in the table below.

Duty	Frame frequency
1/8	78.1 Hz
1/11	56.8 Hz
1/16	78.1 Hz

(Note) The OSC oscillation frequency is assumed to be 250 KHz.

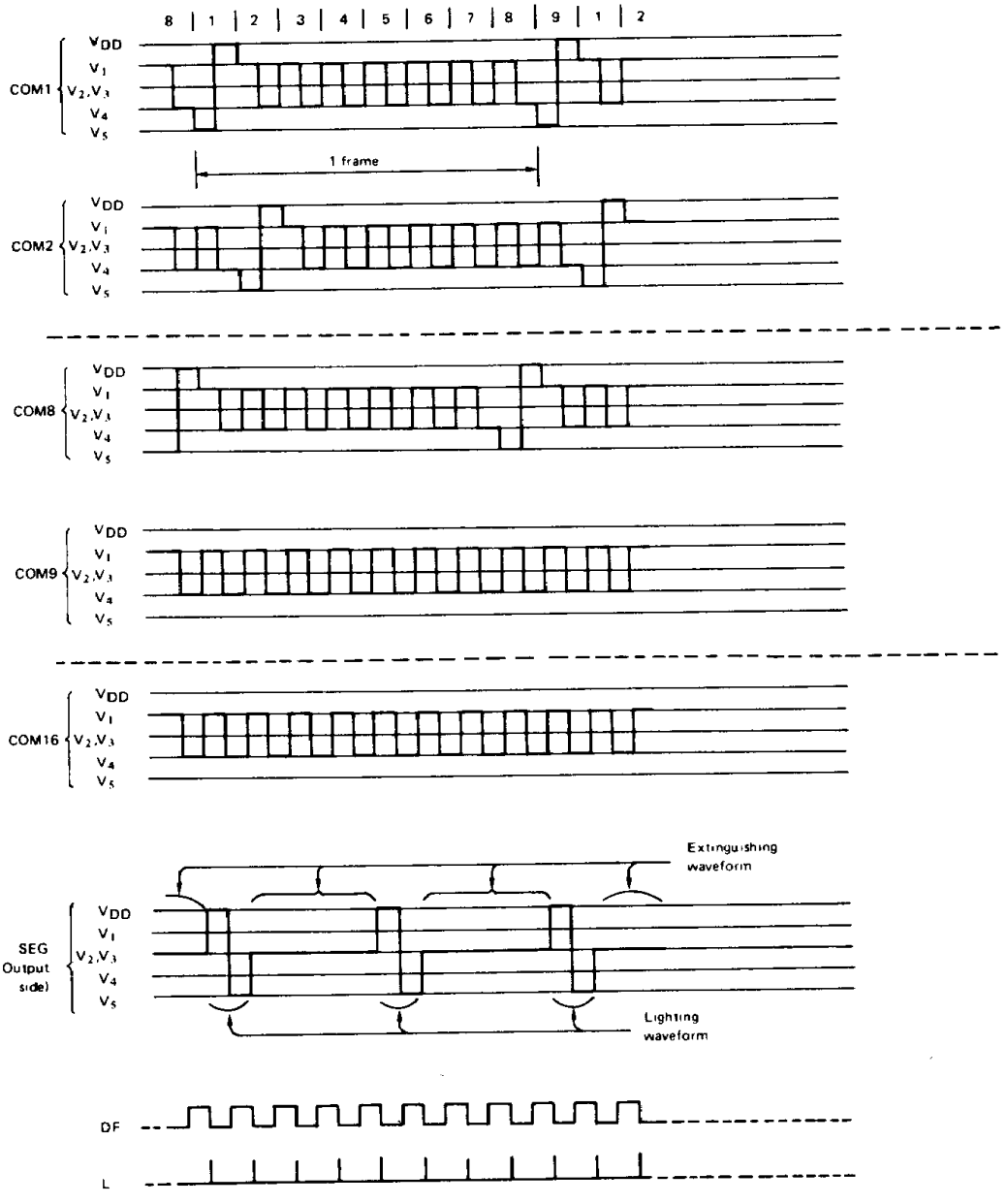


Figure 4 LCD driving waveform at 1/8 duty.

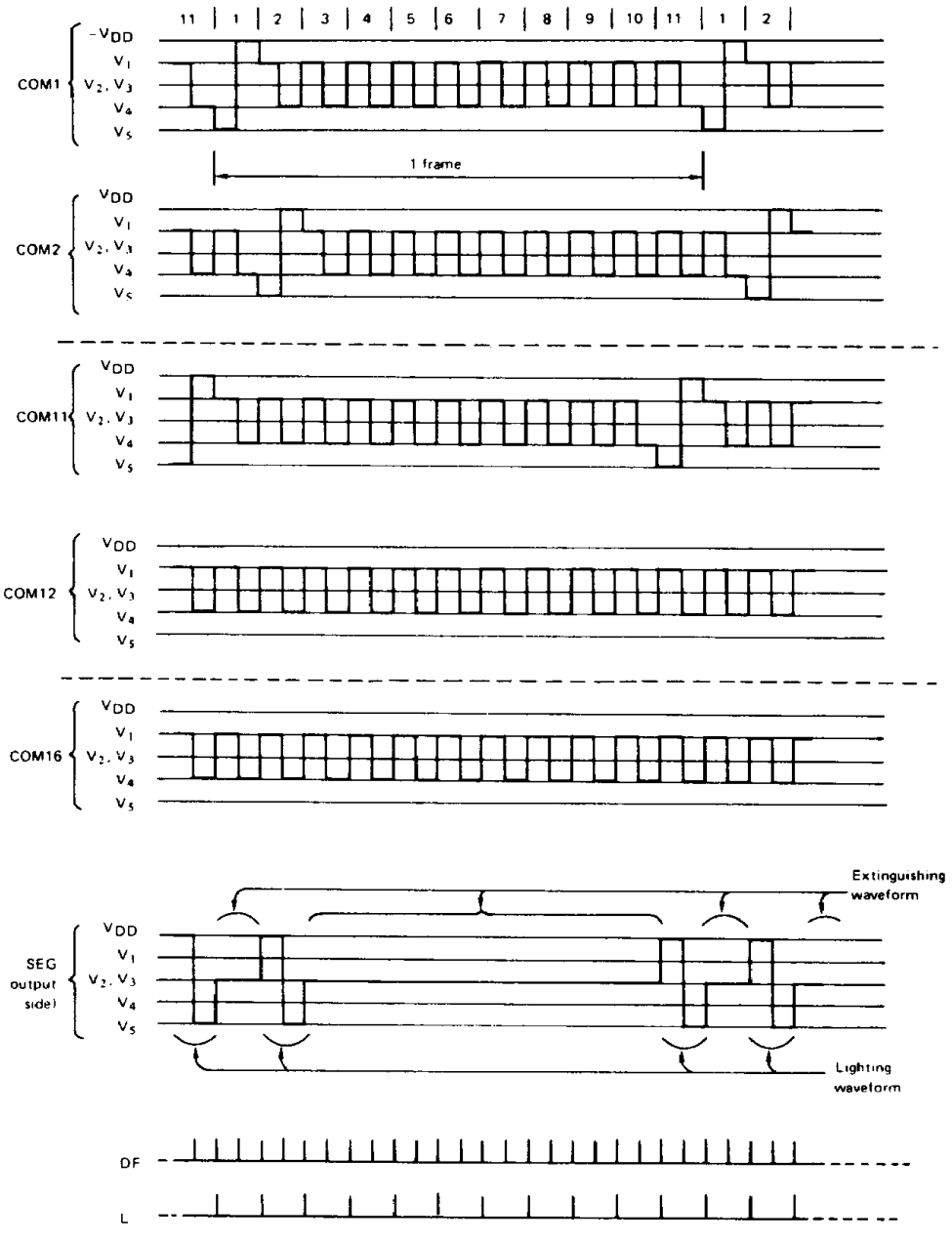


Figure 5 LCD driving waveform at 1/11 duty.

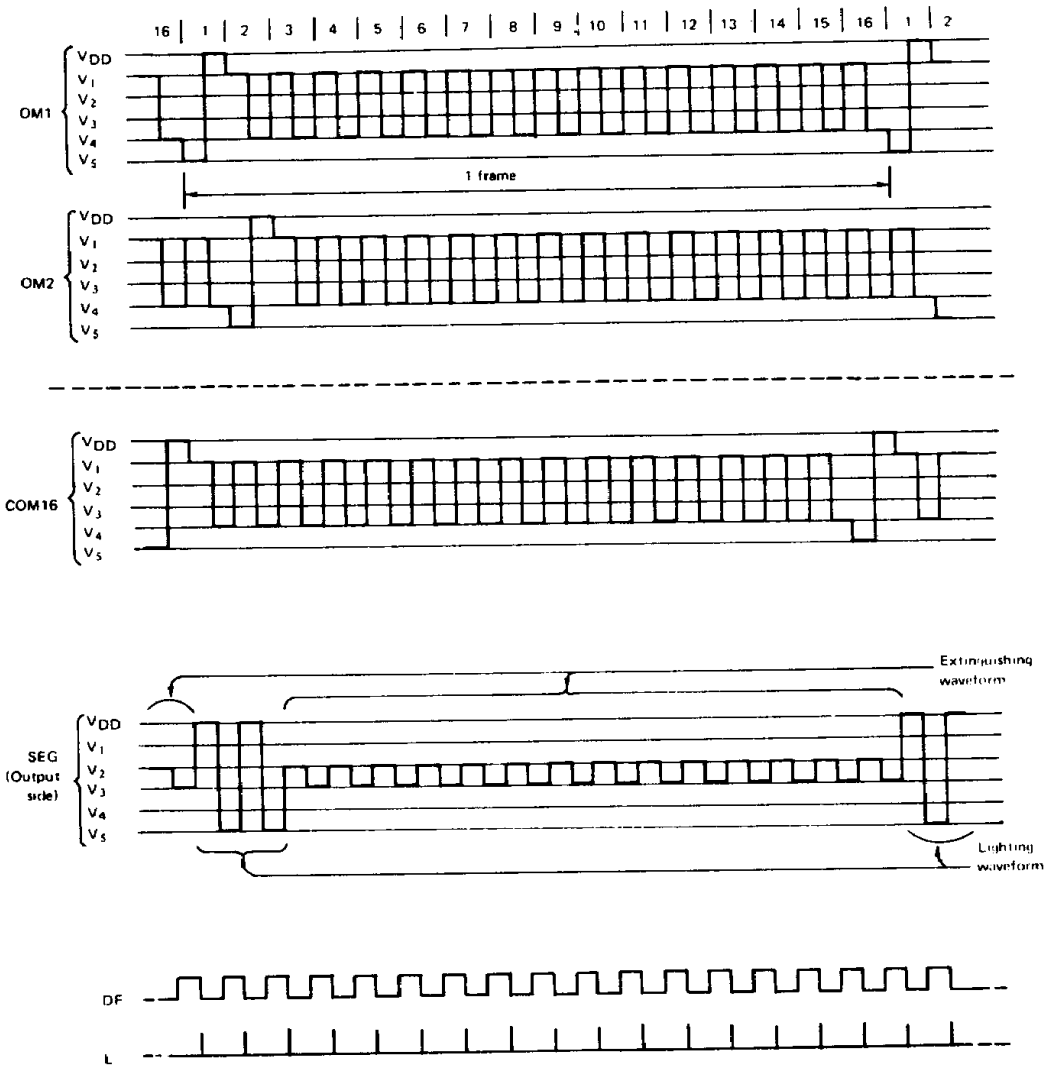


Figure 6 LCD driving waveform at 1/16 duty.

INPUT/OUTPUT TIMING TO AND FROM THE CPU AND OUTPUT TIMING TO MSM5259GS

Table 4, 5 and 6 show input characteristics from the CPU, output characteristics to the CPU and output characteristics to MSM5259GS respectively.

- **Input characteristics from the CPU**

  (V_{DD} = 4.5 ~ 5.5V, T_a = −20 ~ +75°C)

Parameter	Symbol	Limits			Unit
		MIN	TYP	MAX	
R/W and RS set-up time	t_B	140	–	–	nS
E and H pulse width	t_W	280	–	–	nS
R/W and RS holding time	t_A	10	–	–	nS
E rise time	t_r	–	–	25	nS
E fall time	t_f	–	–	25	nS
E and L pulse width	t_L	280	–	–	nS
E cycle time	t_C	667	–	–	nS
DB_0 to DB_7 input data set-up time	t_I	180	–	–	nS
DB_0 to DB_7 input data holding time	t_H	10	–	–	nS

Table 4: Input characteristics from the CPU

- **Output characteristics to the CPU**

  (V_{DD} = 4.5 ~ 5.5V, T_a = −20 ~ +75°C)

Parameter	Symbol	Limits			Unit
		MIN	TYP	MAX	
R/W and RS set-up time	t_B	140	–	–	nS
E and H pulse width	t_W	280	–	–	nS
R/W and RS holding time	t_A	10	–	–	nS
E rise time	t_r	–	–	25	nS
E fall time	t_f	–	–	25	nS
E and L pulse width	t_L	280	–	–	nS
E cycle time	t_C	667	–	–	nS
DB_0 to DB_7 data output delay time	t_D	–	–	220	nS
DB_0 to DB_7 data output holding time	t_O	20	–	–	nS

Table 5: Output characteristics to the CPU

- **Output characteristics to MSM5259GS**
  (V_{DD} = 4.5 ~ 5.5V, T_a = −20 ~ +75°C)

Parameter	Symbol	Limits			Unit
		MIN	TYP	MAX	
CP and H pulse width	t_{HW1}	800	–	–	nS
CP and L pulse width	t_{LW}	800	–	–	nS
DO set-up time	t_S	300	–	–	nS
DO holding time	t_{DH}	300	–	–	nS
L clock set-up time	t_{SU}	500	–	–	nS
L clock holding time	t_{HO}	100	–	–	nS
L and H pulse width	t_{HW2}	800	–	–	nS
DF delay time	t_M	−1000	–	1000	nS

Table 6: Output characteristics to MSM5259GS

Figures 7, 8 and 9 show input timing from the CPU, output timing to the CPU and output timing to MSM5259GS respectively.

- **Input timing from the CPU**

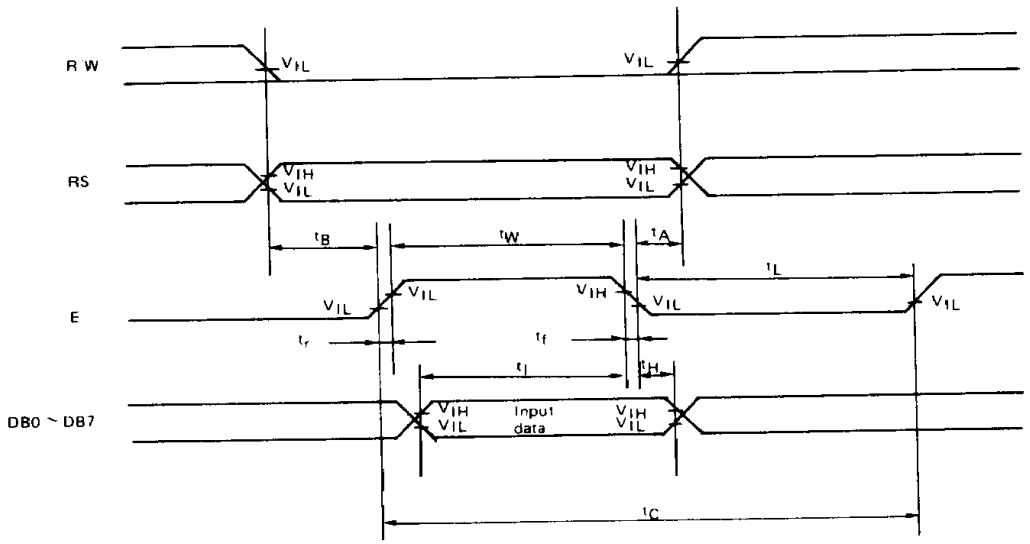


Figure 7

● **Output timing to the CPU**

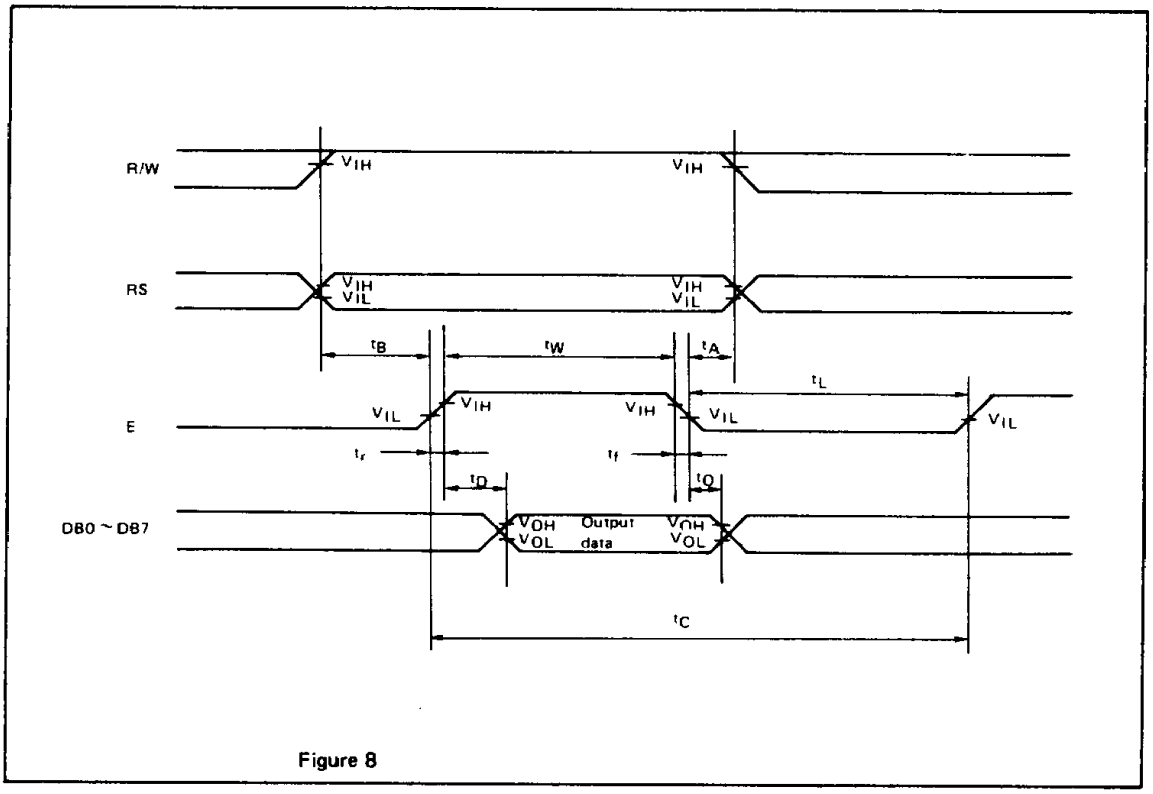


Figure 8

● **Output timing to MSM5259GS**

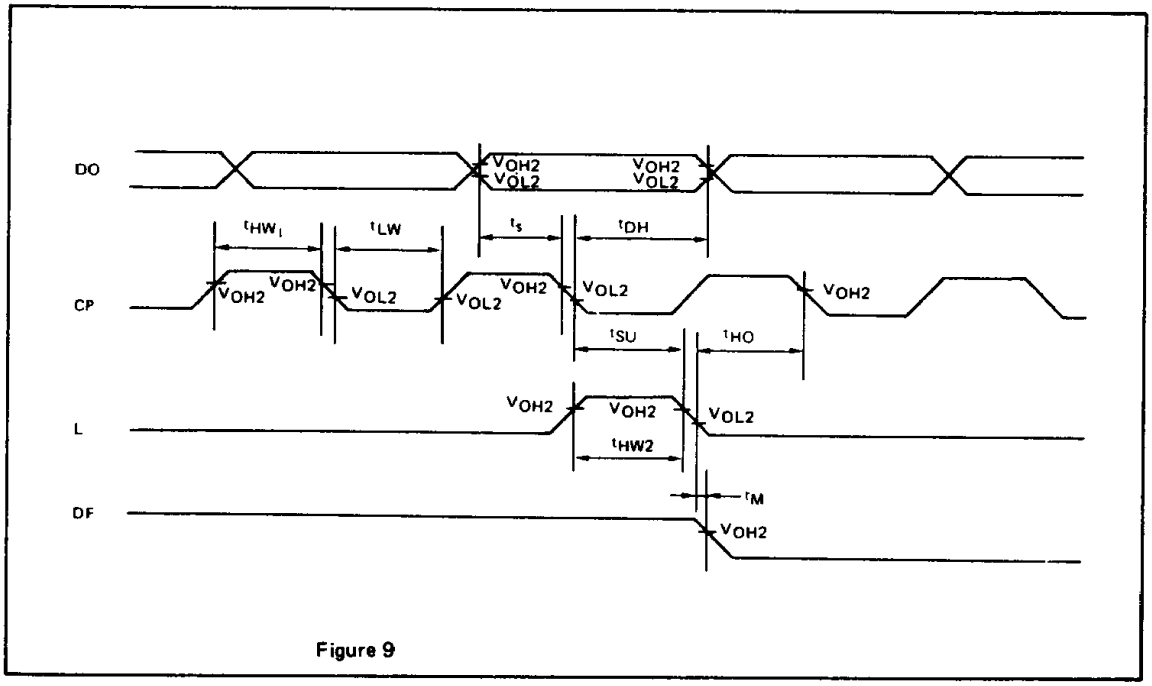


Figure 9

TYPICAL APPLICATION

Interface with LCD and MSM5259GS

Display examples when setting the 5 X 7 dots character font 1-line mode, 5 X 10 dots character font 1-line mode, and 5 X 7 dots character font 2-line mode through instructions are shown in Figures 10, 11, and 12, respectively.

When the 5 X 7 dots character font is set in the 1-line display mode, the COM signals COM9 to COM16 are output for extinguishing.

Likewise, when the 5 X 10 dots character font (1-line is set, the COM signals COM12 to COM16 are output for extinguishing.

The display example shows a combination of 16 characters (32 characters for the 2-line display mode) and the LCD. When the number of MSM5259GSs are increased according to the increase in the number of characters, it is possible to display a maximum of 80 characters.

Besides, it is necessary to generate bias voltage required for LCD operation by splitting resistors outside the IC to input it to MSM6222B-01GS and MSM5259GS.

Examples of these bias voltages are shown in Figures 13, 14, 15, and 16. Basically, this can be done by dividing the voltage of the resistors as shown in Figures 4 and 5. If the value of resistor R is made larger to reduce system power consumption, the LCD operating margin decreases and the LCD drive To prevent this, a by-pass condenser is serially connected to the resistor to lower voltage division impedance caused by the splitting of resistors as shown in Figures 15 and 16.

As the values of R, VR, and C vary according to the LCD size used and V_{LCD} (LCD drive voltage), these values have to be determined through actual experimentation in combination with the LCD. (Example set values:

$R = 3.3 - 10\ K\Omega$, $V_R = 10 - 30\ K\Omega$, and

$C = 0.0022\ \mu F$ to $0.047\ \mu F$)

Figure 17 shows an application circuit for the MSM6222B-01GS and MSM5259GS including a bias circuit.

The bias voltage has to maintain the following potential relation:

$$V_{DD} > V_1 > V_2 \geqq V_3 > V_4 > V_5$$

- In the case of 1-line 16 characters display (5 x 7 dot/font).

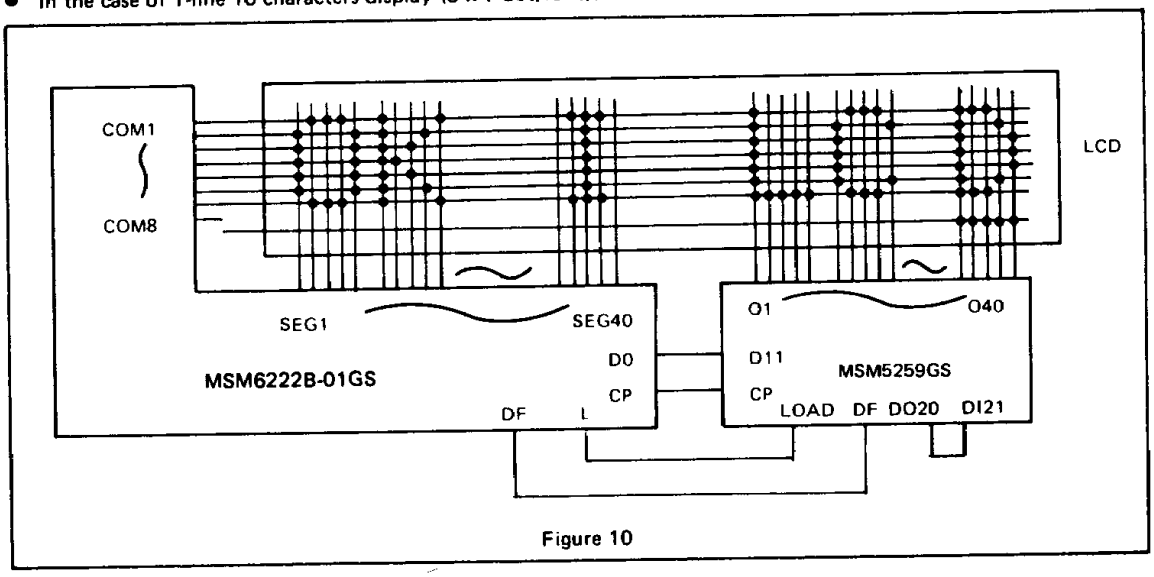


Figure 10

- In the case of 1-line 16 characters display (5 x 10 dot/font)

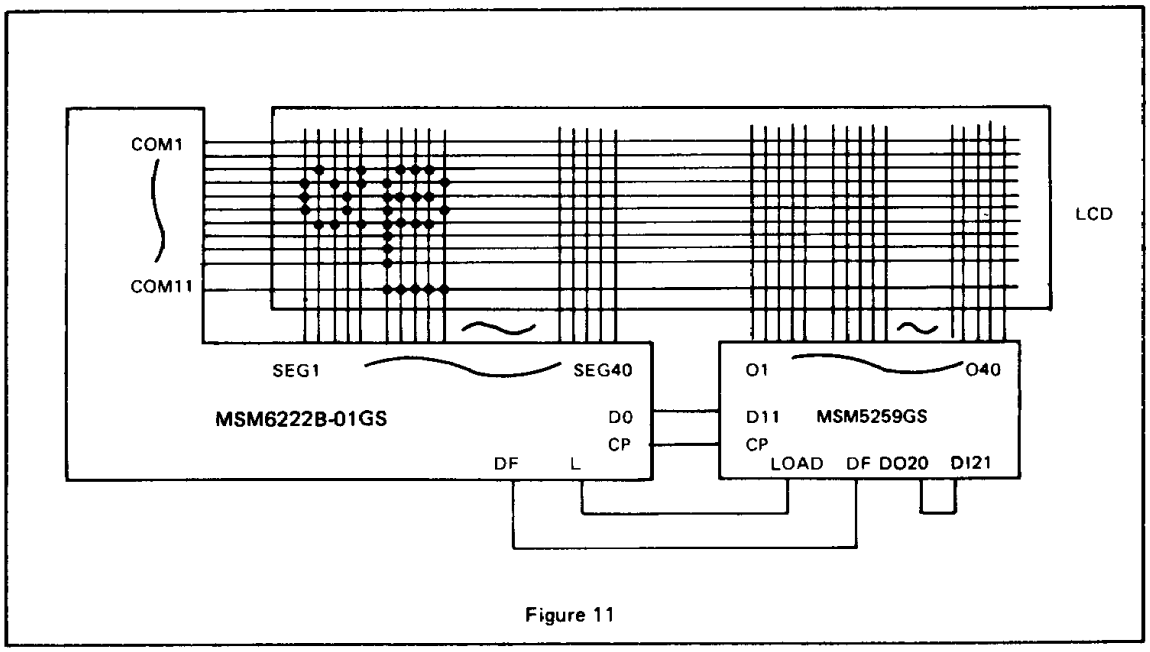


Figure 11

- In the case of 2-lines 16 characters display (5 x 7 dot/font)

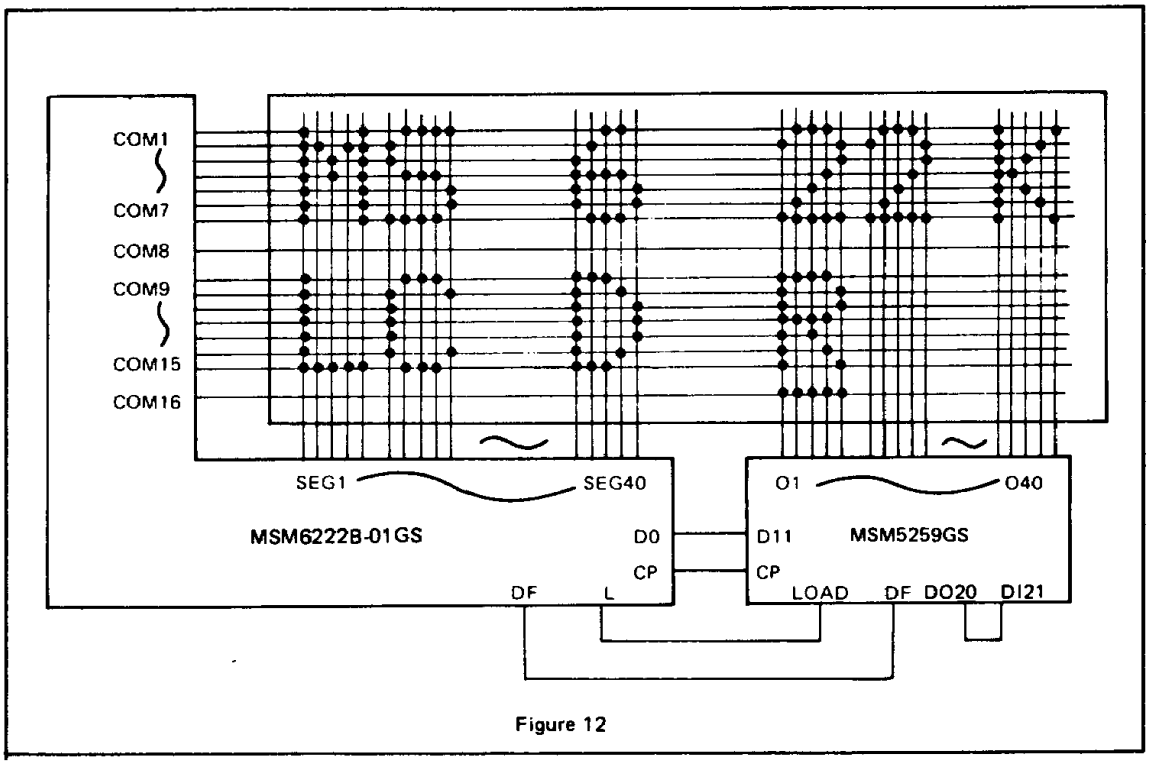


Figure 12

● Bias voltage circuit (1-line display mode)

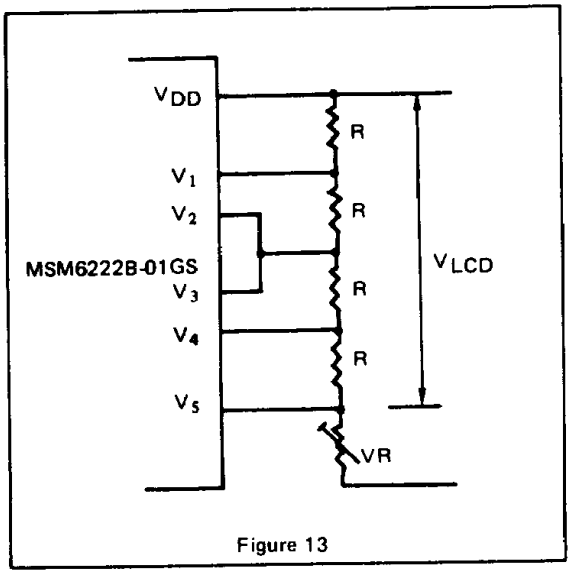


Figure 13

● Bias voltage circuit (2-line display mode)

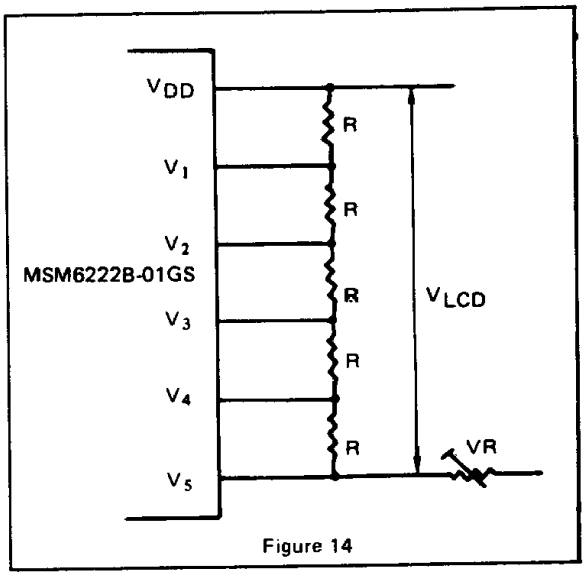


Figure 14

● Bias voltage circuit (1-line display mode)

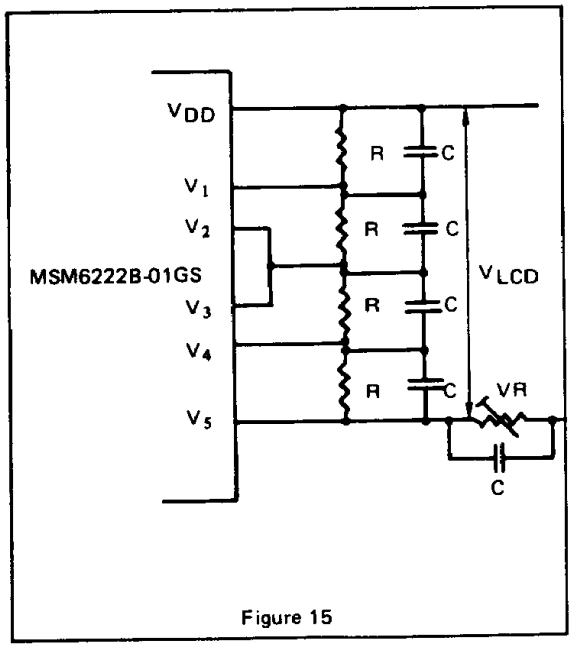


Figure 15

● Bias voltage circuit (2-line display mode)

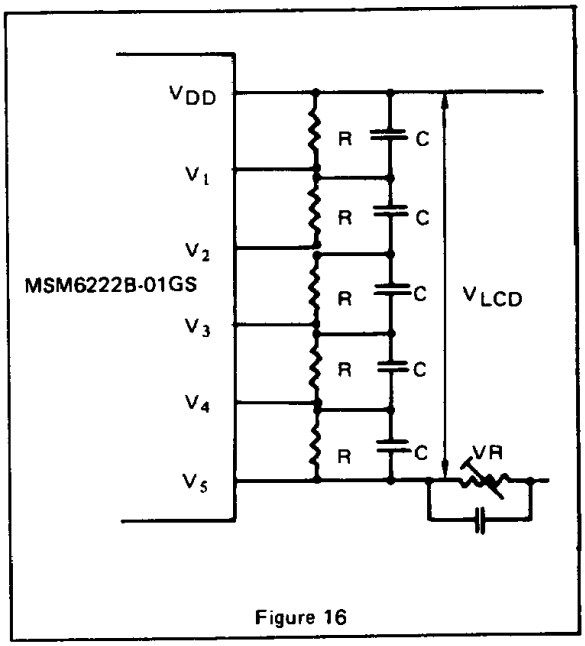


Figure 16

(V_{LCD}: LCD driving voltage)

● Application circuit.

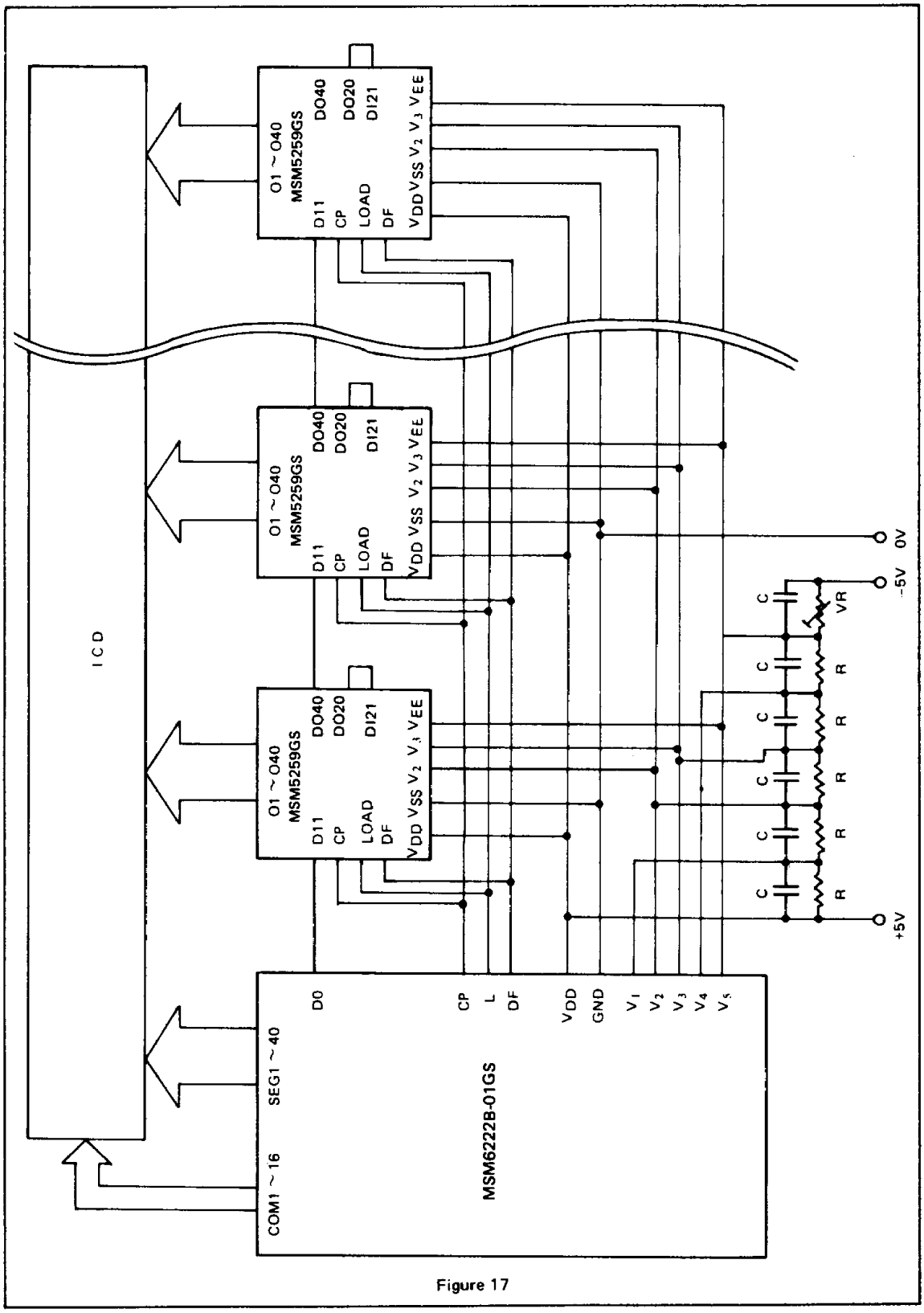


Figure 17