

Thyristors

BT151B series

GENERAL DESCRIPTION

Glass passivated thyristors in a plastic envelope, suitable for surface mounting, intended for use in applications requiring high bidirectional blocking voltage capability and high thermal cycling performance. Typical applications include motor control, industrial and domestic lighting, heating and static switching.

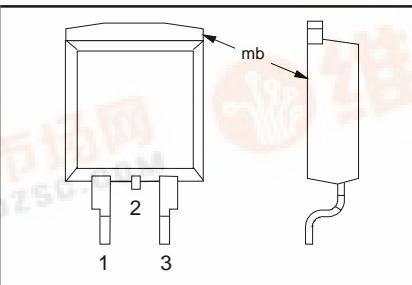
QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | MAX. | UNIT |
|--------------------------|---|-------------|-------------|-------------|------|
| V_{DRM} , V_{RRM} | Repetitive peak off-state voltages | 500R 500 | 650R 650 | 800R 800 | V |
| $I_{T(AV)}$ | Average on-state current | 7.5 | 7.5 | 7.5 | A |
| $I_{T(RMS)}$ | RMS on-state current | 12 | 12 | 12 | A |
| I_{TSM} | Non-repetitive peak on-state current | 100 | 100 | 100 | A |

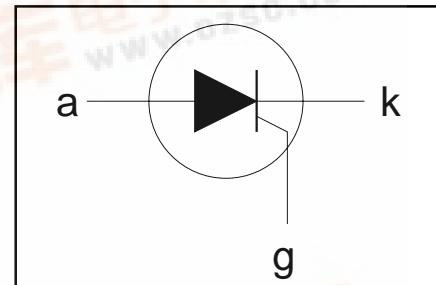
PINNING - SOT404

| PIN | DESCRIPTION |
|-----|-------------|
| 1 | cathode |
| 2 | anode |
| 3 | gate |
| mb | anode |

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | | UNIT |
|-----------------------|--|---|------|---------------------------|---------------------------|--------------|------------------|
| V_{DRM} , V_{RRM} | Repetitive peak off-state voltages | | - | -500R 500 ¹ | -650R 650 ¹ | -800R 800 | V |
| $I_{T(AV)}$ | Average on-state current | half sine wave; $T_{mb} \leq 109^\circ\text{C}$ | - | 7.5 | | | A |
| $I_{T(RMS)}$ | RMS on-state current | all conduction angles | - | 12 | | | A |
| I_{TSM} | Non-repetitive peak on-state current | half sine wave; $T_j = 25^\circ\text{C}$ prior to surge | - | | | | |
| I^2t | I^2t for fusing | $t = 10\text{ ms}$ | - | 100 | | | A |
| dI_T/dt | Repetitive rate of rise of on-state current after triggering | $t = 8.3\text{ ms}$ | - | 110 | | | A |
| I_{GM} | Peak gate current | $t = 10\text{ ms}$ | - | 50 | | | A ² s |
| V_{GM} | Peak gate voltage | $I_{TM} = 20\text{ A}$; $I_G = 50\text{ mA}$; $dI_G/dt = 50\text{ mA}/\mu\text{s}$ | - | 50 | | | A/ μs |
| V_{RGM} | Peak reverse gate voltage | | - | 2 | | | A |
| P_{GM} | Peak gate power | | - | 5 | | | V |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | 5 | | | V |
| T_{stg} | Storage temperature | | - | 5 | | | W |
| T_j | Operating junction temperature | | -40 | 0.5 | 150 | 125 | °C |

¹ Although not recommended, off-state voltages up to 800V may be applied without damage, but the thyristor may switch to the on-state. The rate of rise of current should not exceed 15 A/ μs .

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THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|-----------------------|--|------------------------------|------|------|------|------|
| $R_{th\ j\text{-}mb}$ | Thermal resistance junction to mounting base | | - | - | 1.3 | K/W |
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | minimum footprint, FR4 board | - | 55 | - | K/W |

STATIC CHARACTERISTICS

 $T_j = 25^\circ\text{C}$ unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|------------|---------------------------|---|------|------|------|------|
| I_{GT} | Gate trigger current | $V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$ | - | 2 | 15 | mA |
| I_L | Latching current | $V_D = 12\text{ V}$; $I_{GT} = 0.1\text{ A}$ | - | 10 | 40 | mA |
| I_H | Holding current | $V_D = 12\text{ V}$; $I_{GT} = 0.1\text{ A}$ | - | 7 | 20 | mA |
| V_T | On-state voltage | $I_T = 23\text{ A}$ | - | 1.4 | 1.75 | V |
| V_{GT} | Gate trigger voltage | $V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$ | - | 0.6 | 1.5 | V |
| I_D, I_R | Off-state leakage current | $V_D = V_{DRM(\text{max})}$; $I_T = 0.1\text{ A}$; $T_j = 125^\circ\text{C}$ $V_D = V_{DRM(\text{max})}$; $V_R = V_{RRM(\text{max})}$; $T_j = 125^\circ\text{C}$ | 0.25 | 0.4 | - | V |
| | | | - | 0.1 | 0.5 | mA |

DYNAMIC CHARACTERISTICS

 $T_j = 25^\circ\text{C}$ unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|-----------|--|---|-----------|-------------|--------|--------------------------------------|
| dV_D/dt | Critical rate of rise of off-state voltage | $V_{DM} = 67\% V_{DRM(\text{max})}$; $T_j = 125^\circ\text{C}$; exponential waveform; | | | | |
| t_{gt} | Gate controlled turn-on time | Gate open circuit $R_{GK} = 100\ \Omega$ $I_{TM} = 40\text{ A}$; $V_D = V_{DRM(\text{max})}$; $I_G = 0.1\text{ A}$; $dI_G/dt = 5\text{ A}/\mu\text{s}$ | 50 200 | 130 1000 | - - | V/ μs V/ μs |
| t_q | Circuit commutated turn-off time | $V_D = 67\% V_{DRM(\text{max})}$; $T_j = 125^\circ\text{C}$; $I_{TM} = 20\text{ A}$; $V_R = 25\text{ V}$; $dI_{TM}/dt = 30\text{ A}/\mu\text{s}$; $dV_D/dt = 50\text{ V}/\mu\text{s}$; $R_{GK} = 100\ \Omega$ | - | 70 | - | μs |

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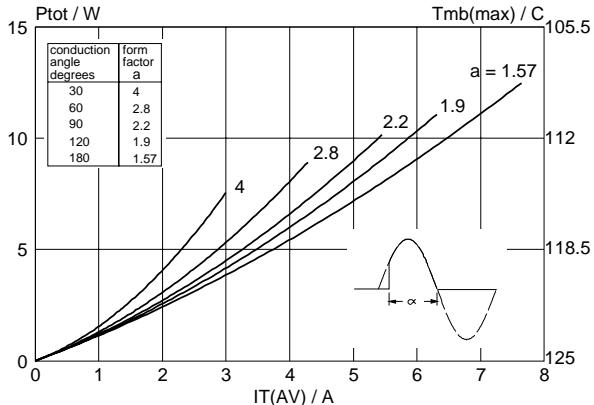


Fig.1. Maximum on-state dissipation, P_{tot} , versus average on-state current, $IT_{(AV)}$, where a = form factor = $IT_{(RMS)}/IT_{(AV)}$.

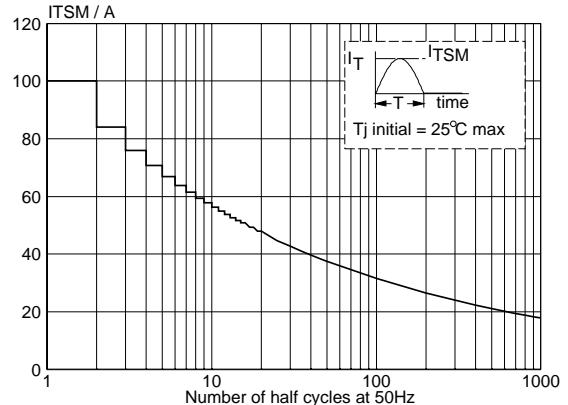


Fig.4. Maximum permissible non-repetitive peak on-state current IT_{SM} , versus number of cycles, for sinusoidal currents, $f = 50$ Hz.

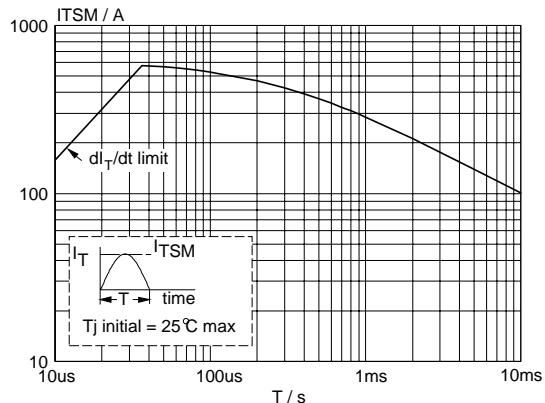


Fig.2. Maximum permissible non-repetitive peak on-state current IT_{SM} , versus pulse width t_p , for sinusoidal currents, $t_p \leq 10$ ms.

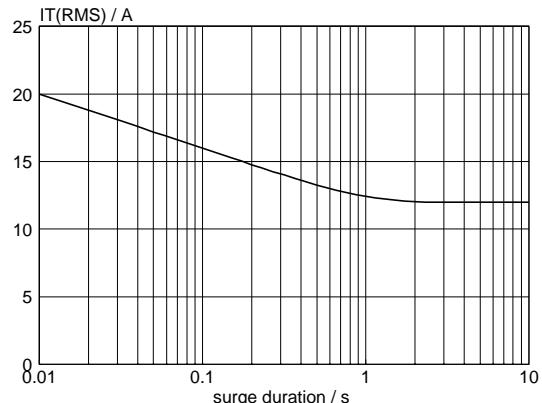


Fig.5. Maximum permissible repetitive rms on-state current $IT_{(RMS)}$, versus surge duration, for sinusoidal currents, $f = 50$ Hz; $T_{mb} \leq 109^\circ\text{C}$.

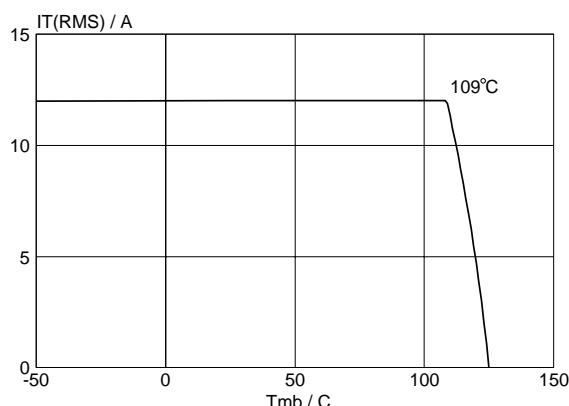


Fig.3. Maximum permissible rms current $IT_{(RMS)}$, versus mounting base temperature T_{mb} .

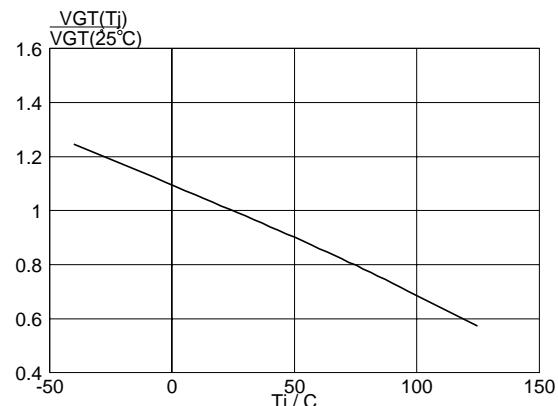


Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/V_{GT}(25^\circ\text{C})$, versus junction temperature T_j .

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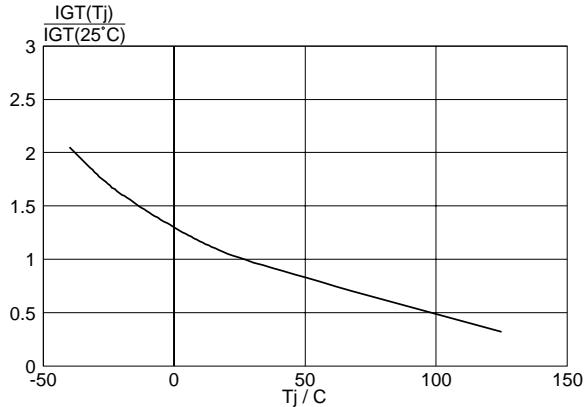


Fig.7. Normalised gate trigger current $I_{GT}(T_j)/I_{GT}(25^\circ\text{C})$, versus junction temperature T_j .

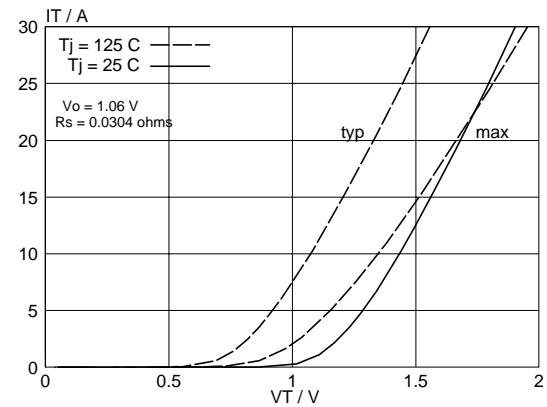


Fig.10. Typical and maximum on-state characteristic.

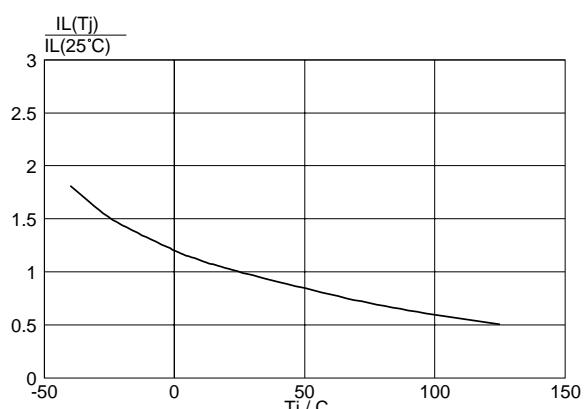


Fig.8. Normalised latching current $I_L(T_j)/I_L(25^\circ\text{C})$, versus junction temperature T_j .

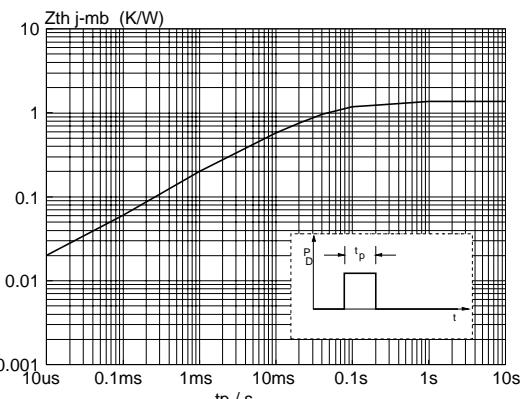


Fig.11. Transient thermal impedance $Z_{th,j-mb}$, versus pulse width t_p .

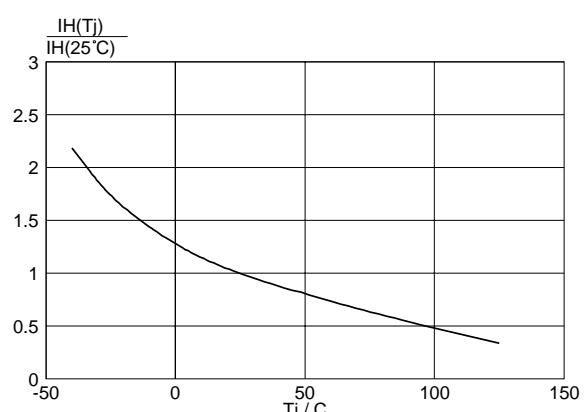


Fig.9. Normalised holding current $I_H(T_j)/I_H(25^\circ\text{C})$, versus junction temperature T_j .

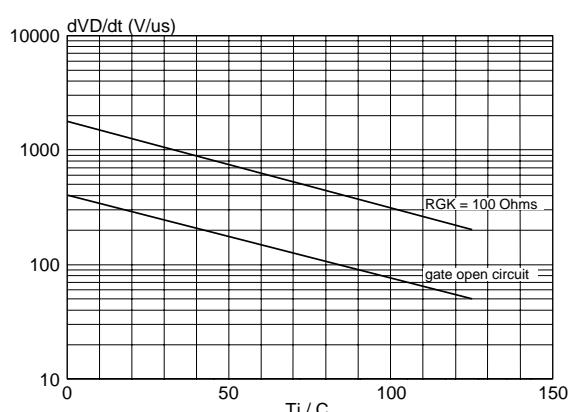


Fig.12. Typical, critical rate of rise of off-state voltage, dV_D/dt versus junction temperature T_j .

MECHANICAL DATA

Dimensions in mm

Net Mass: 1.4 g

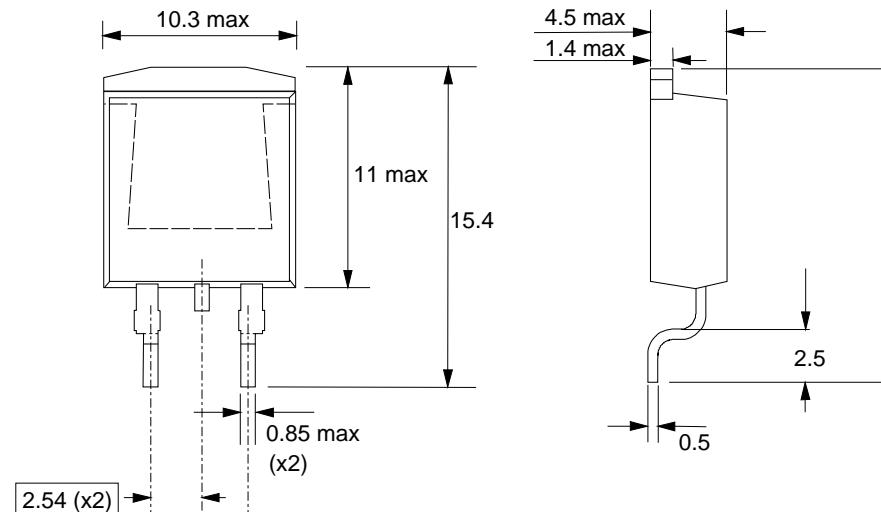


Fig.13. SOT404 : centre pin connected to mounting base.

Notes

1. Epoxy meets UL94 V0 at 1/8".

MOUNTING INSTRUCTIONS

Dimensions in mm

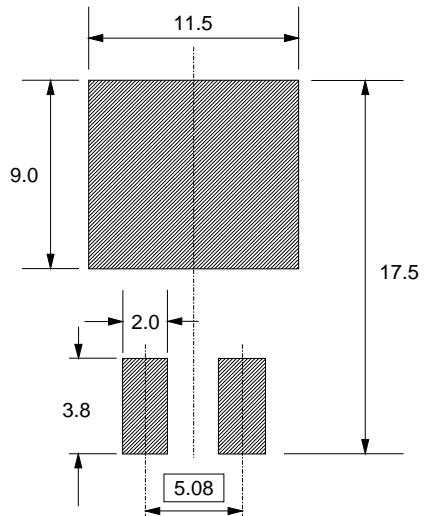


Fig.14. SOT404 : minimum pad sizes for surface mounting.

Notes

1. Plastic meets UL94 V0 at 1/8".

DEFINITIONS

| Data sheet status | |
|--|---|
| Objective specification | This data sheet contains target or goal specifications for product development. |
| Preliminary specification | This data sheet contains preliminary data; supplementary data may be published later. |
| Product specification | This data sheet contains final product specifications. |
| Limiting values | |
| Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability. | |
| Application information | |
| Where application information is given, it is advisory and does not form part of the specification. | |
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