



BIPOLAR ANALOG INTEGRATED CIRCUIT
 μ PC3215TB

5 V, SUPER MINIMOLD SILICON MMIC WIDEBAND AMPLIFIER

DESCRIPTION

The μ PC3215TB is a silicon monolithic IC designed as wideband amplifier. The μ PC3215TB is suitable to systems required wideband operation from HF to L band.

This IC is manufactured using NEC's 30 GHz f_{max} UHS0 (Ultra High Speed Process) silicon bipolar process. The package is 6-pin super minimold suitable for surface mount.

FEATURES

- Wideband response : $f_u = 2.9$ GHz TYP. @3 dB bandwidth
- Noise figure : NF = 2.3 dB TYP. @f = 1.5 GHz
- Power gain : $G_P = 20.5$ dB TYP. @f = 1.5 GHz
- Supply voltage : $V_{CC} = 4.5$ to 5.5 V
- High-density surface mounting: 6-pin super minimold package

APPLICATION

- Systems required wideband operation from HF to L band

ORDERING INFORMATION

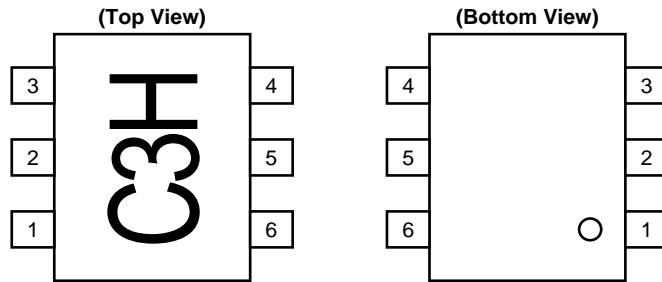
Part Number	Package	Marking	Supplying Form
μ PC3215TB-E3	6-pin super minimold	C3H	Embossed tape 8 mm wide. 1, 2, 3 pins face the perforation side of the tape. Qty 3 kpcs/reel.

Remark To order evaluation samples, please contact your local NEC sales office. (Part number for sample order: μ PC3215TB)

Caution Electro-static sensitive devices

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 Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

PIN CONNECTIONS



Pin No.	Pin Name
1	INPUT
2	GND
3	GND
4	OUTPUT
5	GND
6	V _{cc}

PRODUCT LINE-UP OF 5V-BIAS SILICON MMIC WIDEBAND AMPLIFIERS
 (T_A = +25 °C, V_{cc} = 5.0 V, Z_s = Z_L = 50 Ω)

Part No.	f _u (GHz)	P _{O (sat)} (dBm)	G _P (dB)	NF (dB)	I _{cc} (mA)	Package	Marking
μ PC2711T	2.9	+1.0	13	5.0 @f = 1 GHz	12	6-pin minimold	C1G
μ PC2711TB						6-pin super minimold	
μ PC2712T	2.6	+3.0	20	4.5 @f = 1 GHz	12	6-pin minimold	C1H
μ PC2712TB						6-pin super minimold	
μ PC3210TB	2.3	+3.5	20	3.4 @f = 1.5 GHz	15	6-pin super minimold	C2X
μ PC3215TB	2.9	+3.5	20.5	2.3 @f = 1.5 GHz	14	6-pin super minimold	C3H

Remark Typical performance. Please refer to ELECTRICAL CHARACTERISTICS in detail.

Caution The package size distinguishes between minimold and super minimold.

PIN EXPLANATION

Pin No.	Pin Name	Applied Voltage (V)	Pin Voltage (V) ^{Note}	Function and Applications	Internal Equivalent Circuit
1	INPUT	—	0.82	Signal input pin. A internal matching circuit, configured with resistors, enables 50 Ω connection over a wideband. A multi-feedback circuit is designed to cancel the deviations of h_{FE} and resistance. This pin must be coupled to signal source with capacitor for DC cut.	
2 3 5	GND	0	—	Ground pin. This pin should be connected to system ground with minimum inductance. Ground pattern on the board should be formed as wide as possible. All the ground pins must be connected together with wide ground pattern to decrease impedance difference.	
4	OUTPUT	—	3.8	Signal output pin. A internal matching circuit, configured with resistors, enables 50 Ω connection over a wideband. This pin must be coupled to next stage with capacitor for DC cut.	
6	V _{CC}	4.5 to 5.5	—	Power supply pin. This pin should be externally equipped with bypass capacitor to minimize ground impedance.	

Note Pin voltage is measured at V_{CC} = 5.0 V

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Ratings	Unit
Supply Voltage	V_{CC}	$T_A = +25\text{ }^\circ\text{C}$	6.0	V
Circuit Current	I_{CC}	$T_A = +25\text{ }^\circ\text{C}$	30	mA
Input Power	P_{in}	$T_A = +25\text{ }^\circ\text{C}$	+10	dBm
Power Dissipation	P_D	$T_A = +85\text{ }^\circ\text{C}^{\text{Note}}$	200	mW
Operating Ambient Temperature	T_A		-40 to +85	$^\circ\text{C}$
Storage Temperature	T_{stg}		-55 to +150	$^\circ\text{C}$

Note Mounted on $50 \times 50 \times 1.6$ -mm epoxy glass PWB, with copper patterning on both sides.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Operating Ambient Temperature	T_A	-40	+25	+85	$^\circ\text{C}$
Input Power	P_{in}	-	-	0	dBm
Input Frequency	F_{in}	0.1	-	2.9	GHz

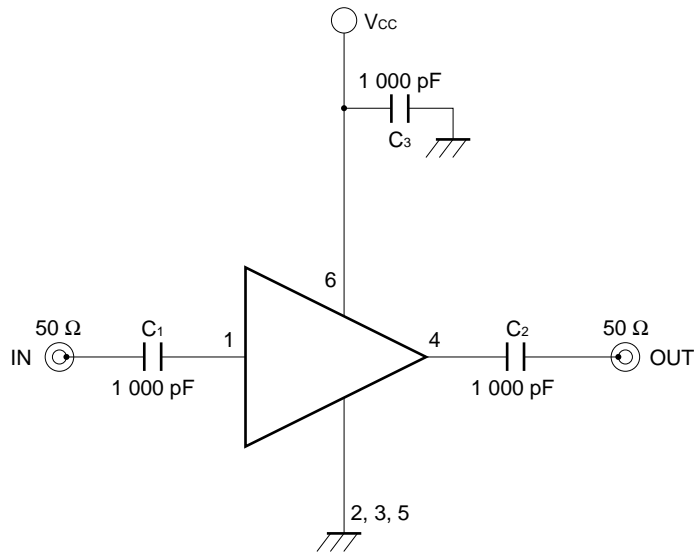
ELECTRICAL CHARACTERISTICS ($T_A = +25\text{ }^\circ\text{C}$, $V_{CC} = 5.0\text{ V}$, $Z_s = Z_L = 50\ \Omega$)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Circuit Current	I_{CC}	No input signals	10.5	14.0	17.5	mA
Power Gain	G_P	$f = 1.5\text{ GHz}$, $P_{in} = -30\text{ dBm}$	18.5	20.5	-	dB
Noise Figure	NF	$f = 1.5\text{ GHz}$	-	2.3	3.0	dB
Upper Limit Operating Frequency	f_u	3 dB down below from gain at $f = 0.1\text{ GHz}$	2.5	2.9	-	GHz
Isolation	ISL	$f = 1.5\text{ GHz}$, $P_{in} = -30\text{ dBm}$	39	44	-	dB
Input Return Loss	RL_{in}	$f = 1.5\text{ GHz}$, $P_{in} = -30\text{ dBm}$	10	15	-	dB
Output Return Loss	RL_{out}	$f = 1.5\text{ GHz}$, $P_{in} = -30\text{ dBm}$	6.5	9.5	-	dB
1 dB Compression Point	P-1		-4	-1.5	-	dBm

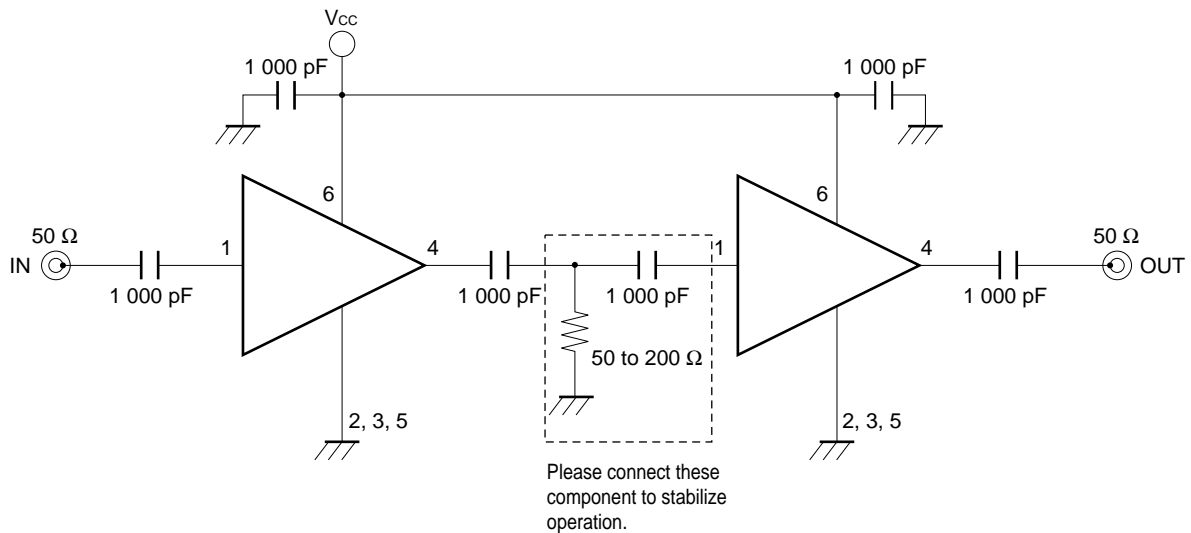
STANDARD CHARACTERISTICS ($T_A = +25\text{ }^\circ\text{C}$, $V_{CC} = 5.0\text{ V}$, $Z_s = Z_L = 50\ \Omega$)

Parameter	Symbol	Test Conditions	Reference Values	Unit
Saturated Output Power	$P_{O(sat)}$	$P_{in} = 0\text{ dBm}$	+3.5	dBm
Output Intercept Point	OIP_3	$f_1 = 1.5\text{ GHz}$, $f_2 = 1.501\text{ GHz}$	+10	dBm
Gain Flatness	ΔG_P	$f = 0.1\text{ to }2.15\text{ GHz}$	1.0	dB

TEST CIRCUIT



EXAMPLE OF APPLICATION CIRCUIT



The application circuits and their parameters are for reference only and are not intended for use in actual design-ins.

Capacitors for Vcc, input and output pins

1 000 pF capacitors are recommendable as bypass capacitor for Vcc pin and coupling capacitors for input/output pins.

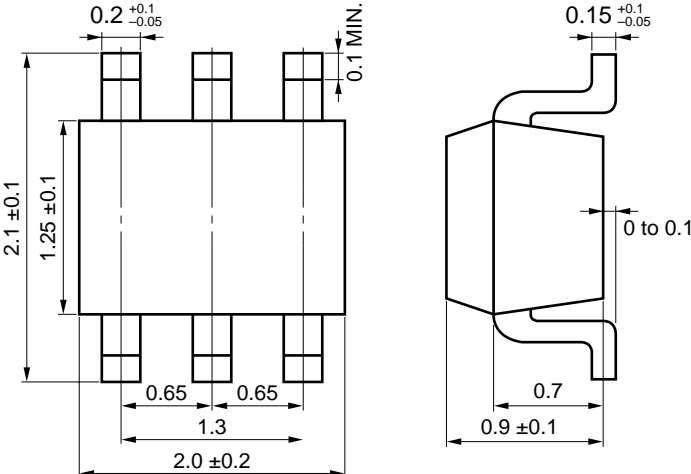
Bypass capacitor for Vcc pin is intended to minimize Vcc pin's ground impedance. Therefore, stable bias can be supplied against Vcc fluctuation.

Coupling capacitors for input/output pins are intended to minimize RF serial impedance and cut DC.

To get flat gain from 100 MHz up, 1 000 pF capacitors are assembled on the test circuit. [Actually, 1 000 pF capacitors give flat gain at least 10 MHz. In the case of under 10 MHz operation, increase the value of coupling capacitor such as 2 200 pF. Because the coupling capacitors are determined by the equation of $C = 1/(2 \pi fZ_s)$.]

PACKAGE DIMENSIONS

6 PIN SUPER MINIMOLD (UNIT: mm)



NOTES ON CORRECT USE

- (1) Observe precautions for handling because of electro-static sensitive devices.
- (2) Form a ground pattern as widely as possible to minimize ground impedance (to prevent undesired oscillation).
- (3) Keep the track length of the ground pins as short as possible.
- (4) A low pass filter must be attached to Vcc line.

RECOMMENDED SOLDERING CONDITIONS

This product should be soldered under the following recommended conditions. For soldering methods and conditions other than those recommended below, contact your NEC sales representative.

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared Reflow	Package peak temperature: 235 °C or below Time: 30 seconds or less (at 210 °C) Count: 3, Exposure limit: None ^{Note}	IR35-00-3
VPS	Package peak temperature: 215 °C or below Time: 40 seconds or less (at 200 °C) Count: 3, Exposure limit: None ^{Note}	VP15-00-3
Wave Soldering	Soldering bath temperature: 260 °C or below Time: 10 seconds or less Count: 1, Exposure limit: None ^{Note}	WS60-00-1
Partial Heating	Pin temperature: 300 °C Time: 3 seconds or less (per side of device) Exposure limit: None ^{Note}	—

Note After opening the dry pack, keep it in a place below 25 °C and 65 % RH for the allowable storage period.

Caution Do not use different soldering methods together (except for partial heating).

For details of recommended soldering conditions for surface mounting, refer to information document SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL (C10535E).

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