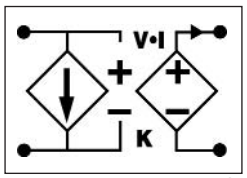
PRELIMINARY

V•I Chip™ – BCM Bus Converter Module

- 48 V to 6 V V•I Chip Converter
- 240 Watt (360 Watt for 1 ms)
- High density – 974 W/in³
- Small footprint – 220 W/in²
- Low weight – 0.5 oz (14 g)
- ZVS/ZCS isolated sine amplitude converter
- Typical efficiency 95%
- 125°C operation
- <1 µs transient response
- 3.5 million hours MTBF
- No output filtering required
- Surface mount BGA or J-Lead packages



©

Vin = 38 - 55 V
Vout = 4.75 - 6.87 V
Iout = 40.0 A
K = 1/8
Rout = 7.5 mΩ max

B048K060T24

K indicates BGA configuration. For other mounting options see Part Numbering below.

Actual size

Product Description

The V•I Chip Bus Converter Module (BCM) is a high efficiency (>95%), narrow input range Sine Amplitude Converter (SAC) operating from a 38 to 55 Vdc primary bus to deliver an isolated 4.75 V to 6.87 V secondary. The BCM may be used to power non-isolated POL converters or as an independent 4.75 – 6.87 V source. Due to the fast response time and low noise of the BCM, the need for limited life aluminum electrolytic or tantalum capacitors at the input of POL converters is reduced—or eliminated—resulting in savings of board area, materials and total system cost.

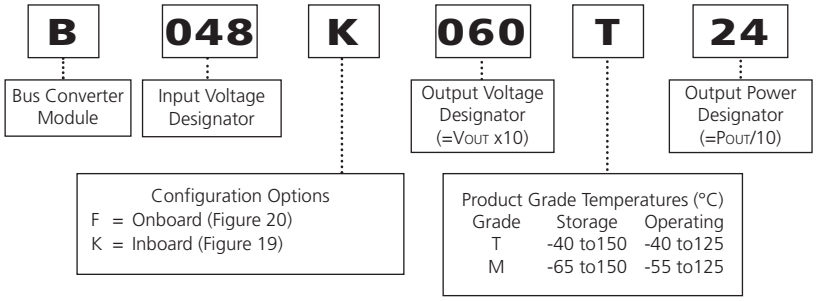
The BCM achieves a power density of 974 W/in³ and may be surface mounted with a profile as low as 0.16" (4 mm) over the PCB. Its V•I Chip power package is compatible with onboard or inboard surface mounting. The V•I Chip package provides flexible thermal management through its low Junction-to-Case and Junction-to-BGA thermal resistance. Owing to its high conversion efficiency and safe operating temperature range, the BCM does not require a discrete heat sink in typical applications. It is also available with heat sink options, assuring low junction temperatures and long life in the harshest environments.

Absolute Maximum Ratings

Parameter	Values	Unit	Notes
+In to -In	-1.0 to 60	Vdc	
+In to -In	100	Vdc	For 100 ms
PC to -In	-0.3 to 7.0	Vdc	
+Out to -Out	-0.5 to 15.0	Vdc	
Isolation voltage	2,250	Vdc	Input to Output
Output current	42.4	A	Continuous
Peak output current	60.0	A	For 1 ms
Output power	240	W	Continuous
Peak output power	360	W	For 1 ms
Case temperature	208	°C	During reflow
Operating junction temperature(1)	-40 to 125 -55 to 125	°C °C	T - Grade M - Grade
Storage temperature	-40 to 150 -65 to 150	°C °C	T - Grade M - Grade

Note:
(1) The referenced junction is defined as the semiconductor having the highest temperature. This temperature is monitored by a shutdown comparator.

Part Numbering



Input (Conditions are at 48 Vin, full load, and 25°C ambient unless otherwise specified)

Parameter	Min	Typ	Max	Unit	Note
Input voltage range	38	48	55	Vdc	
Input dV/dt			1	V/µs	
Input undervoltage turn-on			37.4	Vdc	
Input undervoltage turn-off	32.6			Vdc	
Input overvoltage turn-on	55.0			Vdc	
Input overvoltage turn-off			59.0	Vdc	
Input quiescent current		2.66		mA	PC low
Inrush current overshoot		1.3		A	Using test circuit in Figure 21; See Figure 1
Input current			5.5	Adc	
Input reflected ripple current		275		mA p-p	Using test circuit in Figure 21; See Figure 4
No load power dissipation		2.3	3.5	W	
Internal input capacitance		4.0		µF	
Internal input inductance		20		nH	
Recommended external input capacitance		100		µF	200 nH maximum source inductance; See Figure 21

Input Waveforms

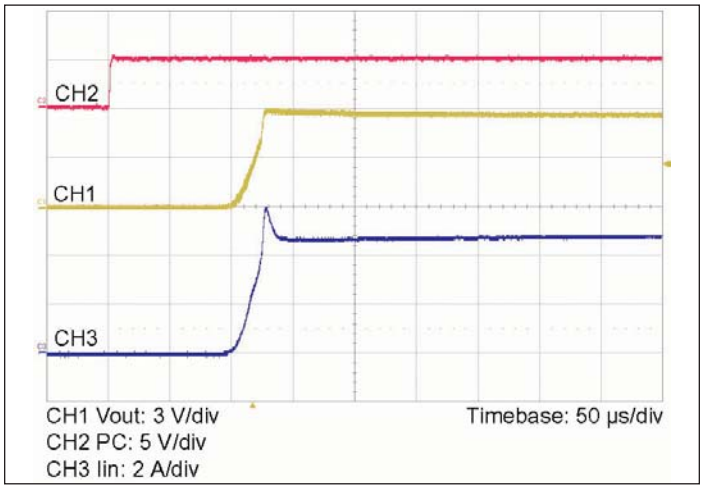


Figure 1— *Inrush transient current at full load and 48 Vin with PC enabled*

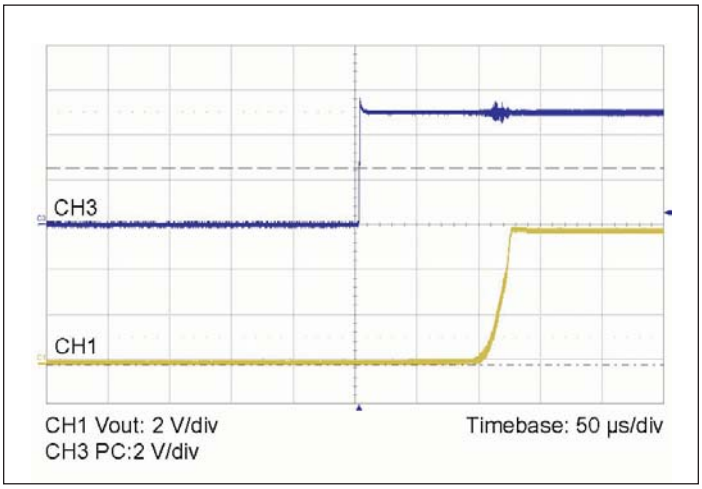


Figure 2— *Output voltage turn-on waveform with PC enabled at full load and 48 Vin*

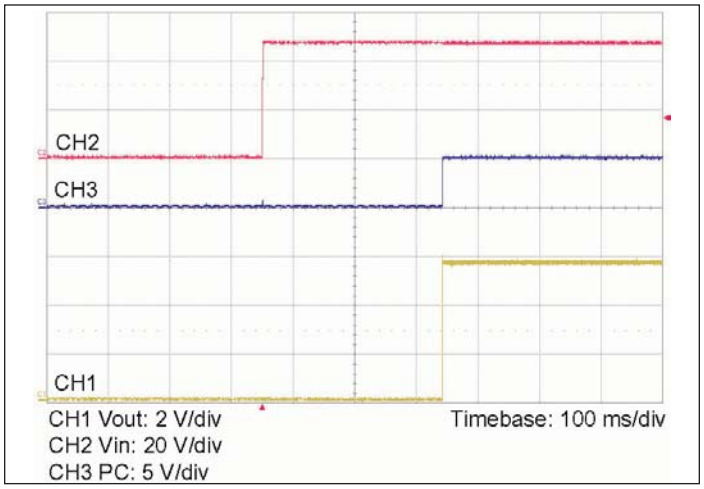


Figure 3—*Output voltage turn-on waveform with input turn-on at full load and 48 Vin*

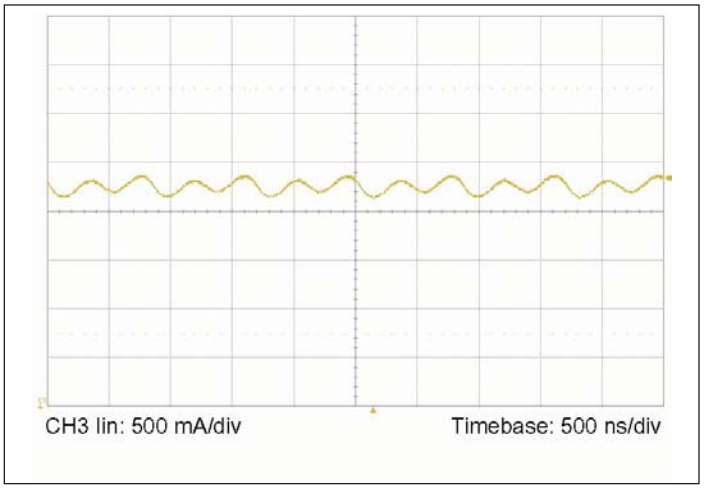


Figure 4— *Input reflected ripple current at full load and 48 Vin*

Output (Conditions are at 48 Vin, full load, and 25°C ambient unless otherwise specified)

Parameter	Min	Typ	Max	Unit	Note
Output voltage	4.75		6.87	Vdc	No load
	4.45		6.60	Vdc	Full load
Output power	0		240	W	48 - 55 VIN
	0		188	W	38 - 55 VIN
Rated DC current	0		42.4	Adc	POUT ≤ 240 W
Peak repetitive power			360	W	Max pulse width 1ms, max duty cycle 10%, baseline power 50%
Current share accuracy		5	10	%	See Parallel Operation on Page 12
Efficiency					
Half load	94.3	95.8		%	See Figure 5
Full load	93.8	94.8		%	See Figure 5
Internal output inductance		1.1		nH	
Internal output capacitance		55.0		µF	Effective value
Load capacitance			4,000	µF	
Output overvoltage setpoint	6.9			Vdc	Module will shut down
Output ripple voltage					
No external bypass		230	300	mV	See Figures 7 and 9
10 µF bypass capacitor		12.5		mV	See Figure 8
Short circuit protection set point	42.8	49.9	55.0	Adc	Module will shut down
Average short circuit current		1		A	
Effective switching frequency	2.0	2.5	3.0	MHz	Fixed, 1.25 MHz per phase
Line regulation					
K	0.1238	1/8	0.1263		VOUT = K•VIN at no load
Load regulation					
ROUT		5.5	7.5	mΩ	
Transient response					
Voltage overshoot		180		mV	100% load step; See Figures 10 and 11
Response time		200		ns	See Figures 10 and 11
Recovery time		1		µs	See Figures 10 and 11
Output overshoot					
Input turn-on		0		mV	No output filter; See Fig.3
PC enable		0		mV	No output filter; See Fig.2
Output turn-on delay					
From application of power		290		ms	No output filter; See Fig.3
From release of PC pin		85		ms	No output filter

Output Waveforms

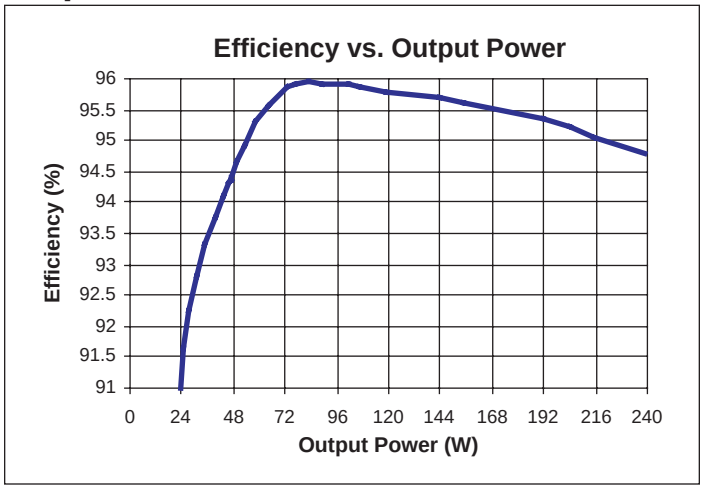


Figure 5— *Efficiency vs. output power at 48 Vin*

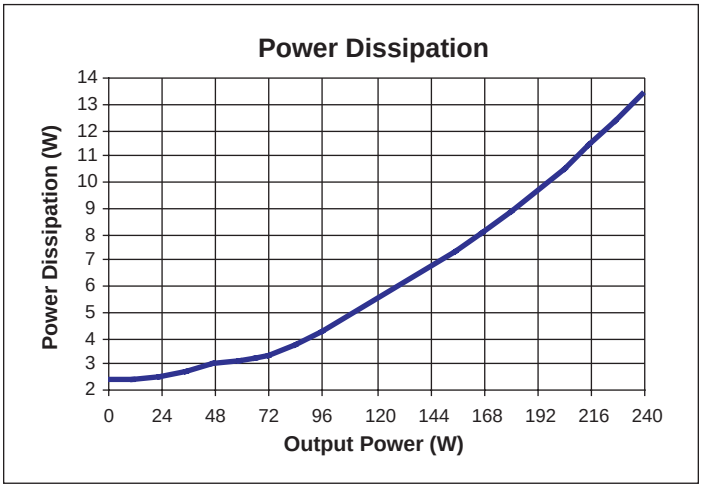


Figure 6—*Power dissipation as a function of output power*

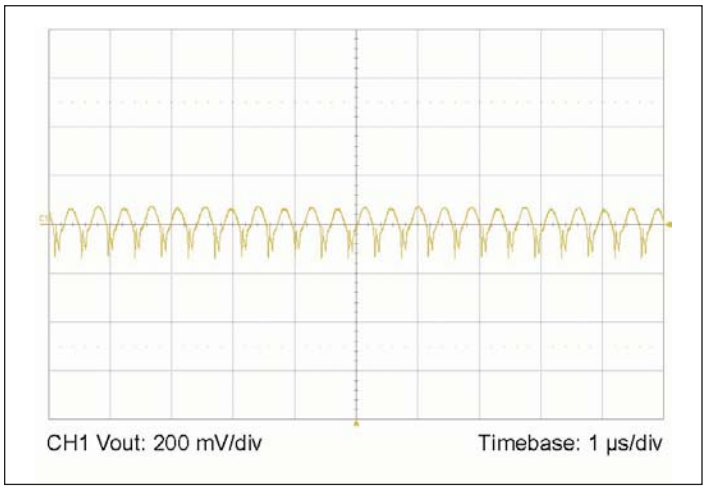


Figure 7— *Output voltage ripple at full load and 48 Vin; without any external bypass capacitor.*

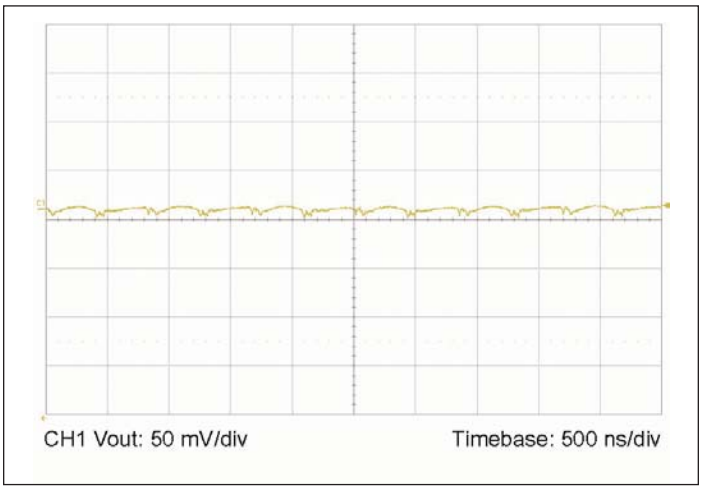


Figure 8—*Output voltage ripple at full load and 48 Vin with 10 µF ceramic external bypass capacitor and 20 nH of distribution inductance.*

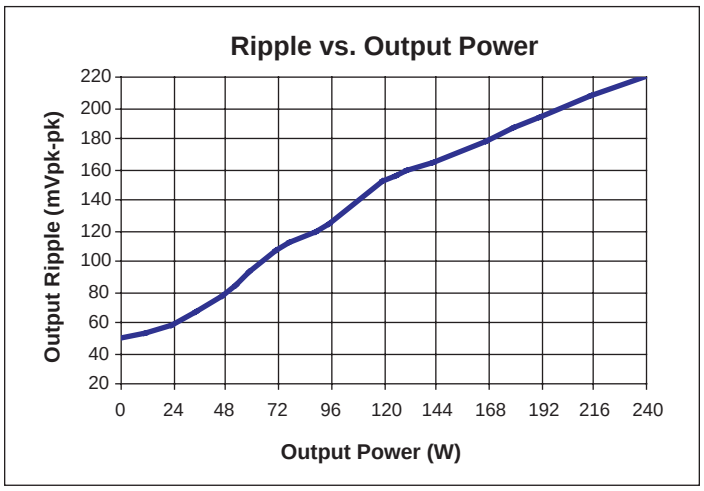


Figure 9— *Output voltage ripple vs. output power at 48 Vin line without any external bypass capacitor.*

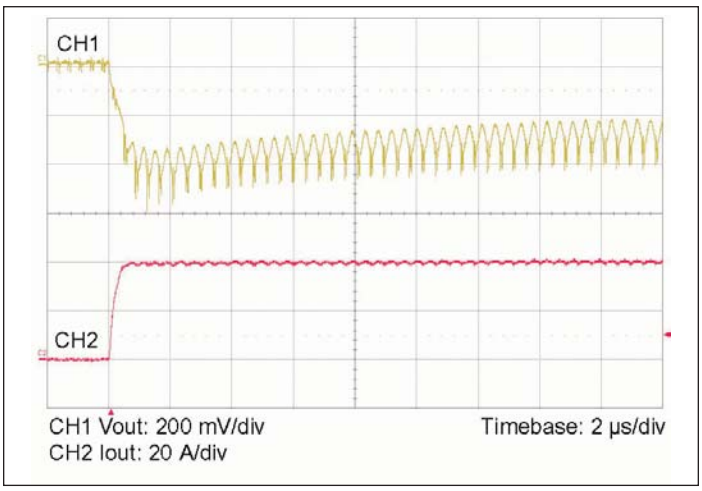


Figure 10— *0 -40.0 A load step with 100 µF input capacitor and no output capacitor.*

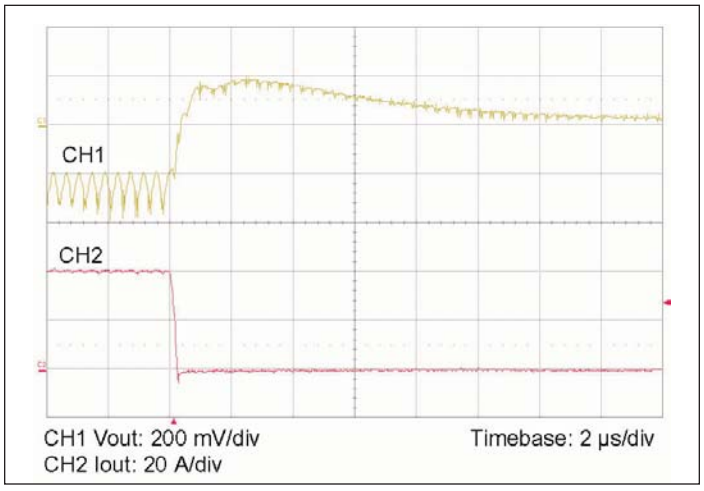


Figure 11— *40.0-0 A load step with 100 µF input capacitance.*

General

Parameter	Min	Typ	Max	Unit	Note
MTBF					
MIL-HDBK-217F		3.5		Mhrs	25°C, GB
Isolation specifications					
Voltage	2,250			Vdc	Input to Output
Capacitance		3,000		pF	Input to Output
Resistance	10			MΩ	Input to Output
Agency approvals (pending)		cTÜVus			UL/CSA 60950, EN 60950
		CE Mark			Low voltage directive
Mechanical parameters					See Mechanical Drawing, Figures 15 and 17
Weight		0.50 / 14		oz / g	
Dimensions					
Length		1.26 / 32		in / mm	
Width		0.85 / 21.5		in / mm	
Height		0.23 / 6		in / mm	

Auxiliary Pins (Conditions are at 48 Vin, full load, and 25°C ambient unless otherwise specified)

Parameter	Min	Typ	Max	Unit	Note
Primary control (PC)					
DC voltage	4.8	5.0	5.2	Vdc	
Module disable voltage	2.4	2.5		Vdc	
Module enable voltage		2.5	2.6	Vdc	
Current limit	2.4	2.5	2.9	mA	Source only
Enable delay time		85		ms	
Disable delay time		10		µs	See Fig.12 time from PC low to output low

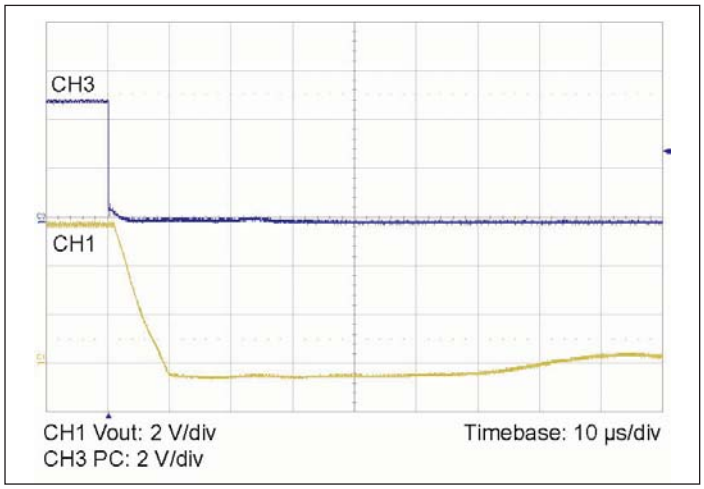


Figure 12— *VOUT at full load vs. PC disable*

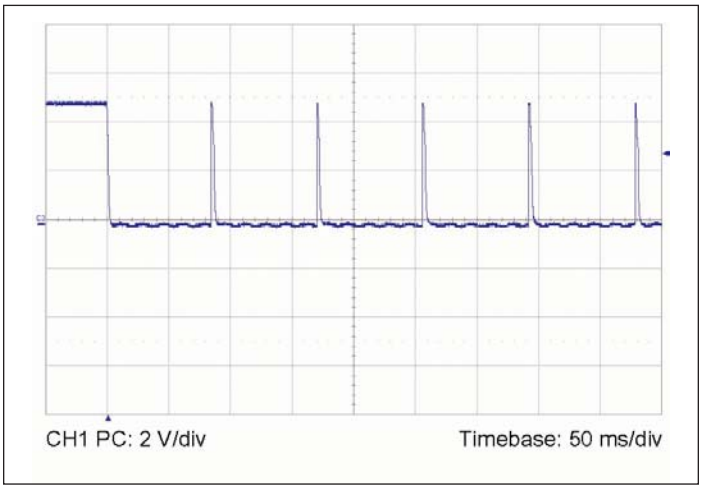


Figure 13— *PC signal during fault*

Thermal

Symbol	Parameter	Min	Typ	Max	Unit	Note
	Over temperature shutdown	125	130	135	°C	Junction temperature
	Thermal capacity		0.61		Ws/°C	BGA package
$R_{\theta JC}$	Junction-to-case thermal impedance		1.1		°C/W	
$R_{\theta JB}$	Junction-to-BGA thermal impedance		2.1		°C/W	
$R_{\theta JA}$	Junction-to-ambient (1)		6.5		°C/W	
$R_{\theta JA}$	Junction-to-ambient (2)		5.0		°C/W	

Notes:
(1 B048K060T24 surface mounted in-board to a 2" x 2" FR4 board, 4 layers 2 oz Cu, 300 LFM.
(2) B048K060T24 with optional 0.25"H Pin Fins surface mounted on FR4 board, 300 LFM.

V•I Chip Stress Driven Product Qualification Process

Test	Standard	Environment
High Temperature Operational Life (HTOL)	JESD22-A-108-B	125°C, Vmax, 1,008 hrs
Temperature cycling	JESD22-A-104B	-55°C to 125°C, 1,000 cycles
High temperature storage	JESD22-A-103A	150°C, 1,000 hrs
Moisture resistance	JESD22-A113-B	Moisture sensitivity Level 5
Temperature Humidity Bias Testing (THB)	EIA/JESD22-A-101-B	85°C, 85% RH, Vmax, 1,008 hrs
Pressure cooker testing (Autoclave)	JESD22-A-102-C	121°C, 100% RH, 15 PSIG, 96 hrs
Highly Accelerated Stress Testing (HAST)	JESD22-A-110B	130°C, 85% RH, Vmax, 96 hrs
Solvent resistance/marking permanency	JESD22-B-107-A	Solvents A, B & C as defined
Mechanical vibration	JESD22-B-103-A	20g peak, 20-2,000 Hz, test in X, Y & Z directions
Mechanical shock	JESD22-B-104-A	1,500g peak 0.5 ms pulse duration, 5 pulses in 6 directions
Electro static discharge testing – human body model	EIA/JESD22-A114-A	Meets or exceeds 2,000 Volts
Electro static discharge testing – machine model	EIA/JESD22-A115-A	Meets or exceeds 200 Volts
Highly Accelerated Life Testing (HALT)	Per Vicor Internal Test Specification(1)	Operation limits verified, destruct margin determined
Dynamic cycling	Per Vicor internal test specification(1)	Constant line, 0-100% load, -20°C to 125°C

Note:
(1) For details of the test protocols see Vicor's website.

V•I Chip Ball Grid Array Interconnect Qualification

Test	Standard	Environment
BGA solder fatigue evaluation	IPC-9701	Cycle condition: TC3 (-40 to +125°C)
	IPC-SM-785	Test duration: NTC-B (500 failure free cycles)
Solder ball shear test	IPC-9701	Failure through bulk solder or copper pad lift-off

+IN/-IN – DC Voltage Input Ports

The V•I Chip input voltage range should not be exceeded. An internal under/over voltage lockout-function prevents operation outside of the normal operating input range. The BCM turns ON within an input voltage window bounded by the "Input under-voltage turn-on" and "Input over-voltage turn-off" levels, as specified. The V•I Chip may be protected against accidental application of a reverse input voltage by the addition of a rectifier in series with the positive input, or a reverse rectifier in shunt with the positive input located on the load side of the input fuse.

The connection of the V•I Chip to its power source should be implemented with minimal distribution inductance. If the interconnect inductance exceeds 100 nH, the input should be bypassed with a RC damper to retain low source impedance and stable operation. With an interconnect inductance of 200 nH, the RC damper may be 100 µF in series with 0.3Ω. A single electrolytic or equivalent low-Q capacitor may be used in place of the series RC bypass.

PC – Primary Control

The Primary Control port is a multifunction node that provides the following functions:

Enable/Disable – If the PC port is left floating, the BCM output is enabled. Once this port is pulled lower than 2.4 Vdc with respect to –In, the output is disabled. This action can be realized by employing a relay, opto-coupler, or open collector transistor. Refer to Figures 1-3, 12 and 13 for the typical Enable/Disable characteristics. This port should not be toggled at a rate higher than 1 Hz. The PC port should also not be driven by or pulled up to an external voltage source.

Primary Auxiliary Supply – The PC port can source up to 2.4 mA at 5.0 Vdc. The PC port should never be used to sink current.

Alarm – The BCM contains circuitry that monitors output overload, input over voltage or under voltage, and internal junction temperatures. In response to an abnormal condition in any of the monitored parameters, the PC port will toggle. Refer to Figure 13 for PC alarm characteristics.

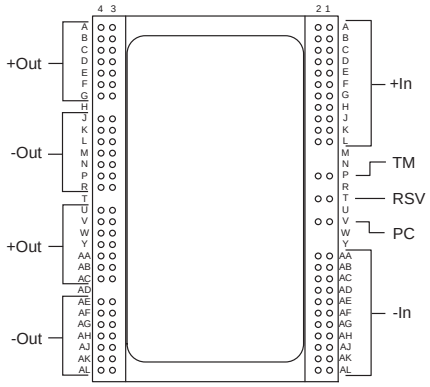
TM and RSV – Reserved for factory use.

+OUT/-OUT – DC Voltage Output Ports

Two sets of contacts are provided for the +Out port. They must be connected in parallel with low interconnect resistance. Similarly, two sets of contacts are provided for the –Out port. They must be connected in parallel with low interconnect resistance. Within the specified operating range, the average output voltage is defined by the Level 1 DC behavioral model of Figure 25. The current source capability of the BCM is rated in the specifications section of this document.

The low output impedance of the BCM reduces or eliminates the need for limited life aluminum electrolytic or tantalum capacitors at the input of POL converters.

Total load capacitance at the output of the BCM should not exceed the specified maximum. Owing to the wide bandwidth and low output impedance of the BCM, low frequency bypass capacitance and significant energy storage may be more densely and efficiently provided by adding capacitance at the input of the BCM.



Bottom View

Signal Name	BGA Designation
+In	A1-L1, A2-L2
–In	AA1-AL1, AA2-AL2
TM	P1, P2
RSV	T1, T2
PC	V1, V2
+Out	A3-G3, A4-G4, U3-AC3, U4-AC4
–Out	J3-R3, J4-R4, AE3-AL3, AE4-AL4

Figure 14*—BCM BGA configuration*

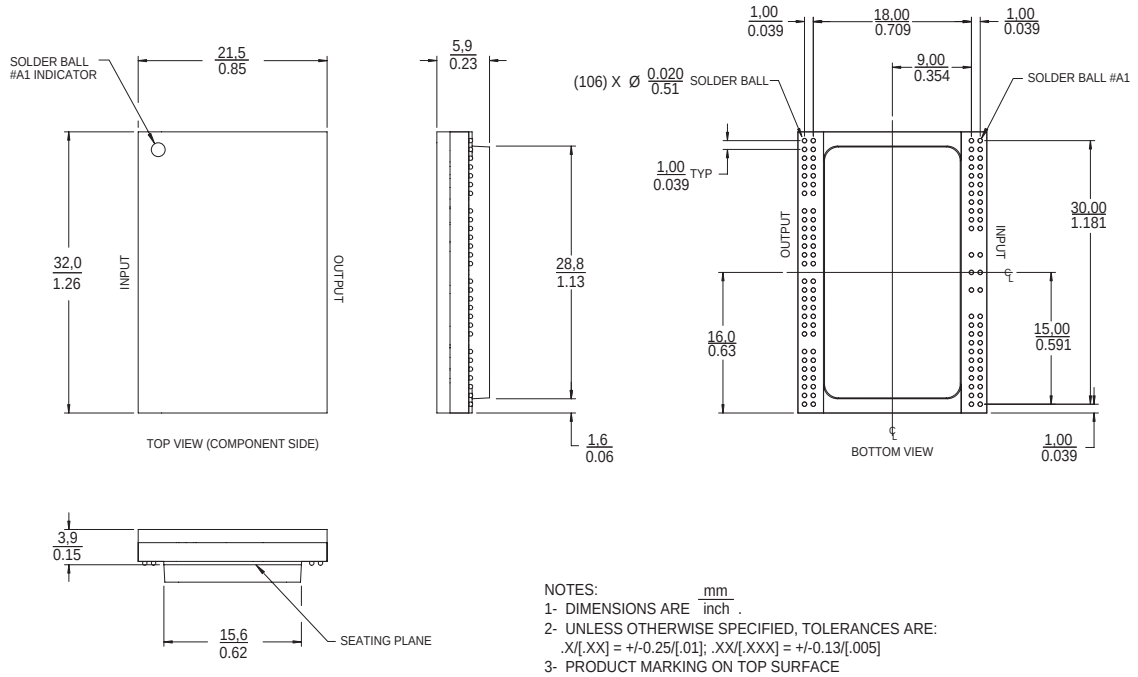


Figure 15*—BCM BGA mechanical outline; Inboard mounting*

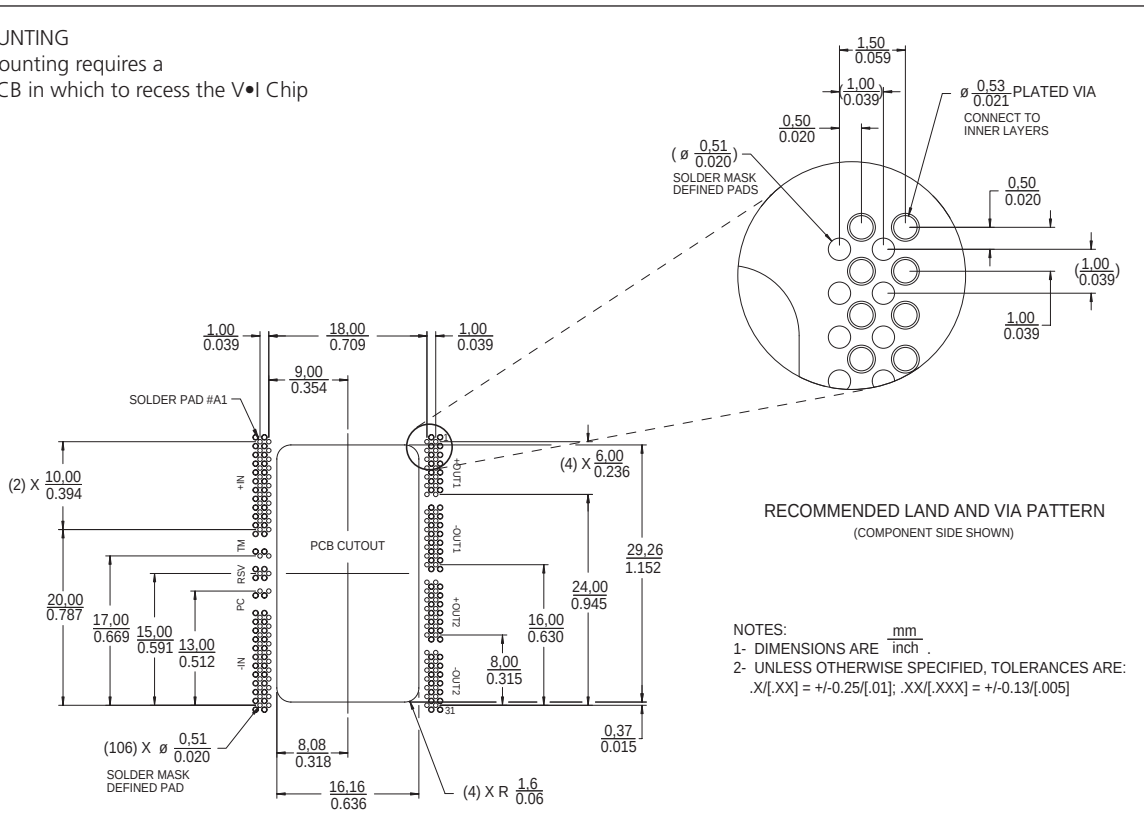


Figure 16*—BCM BGA PCB land/VIA layout information; Inboard mounting*

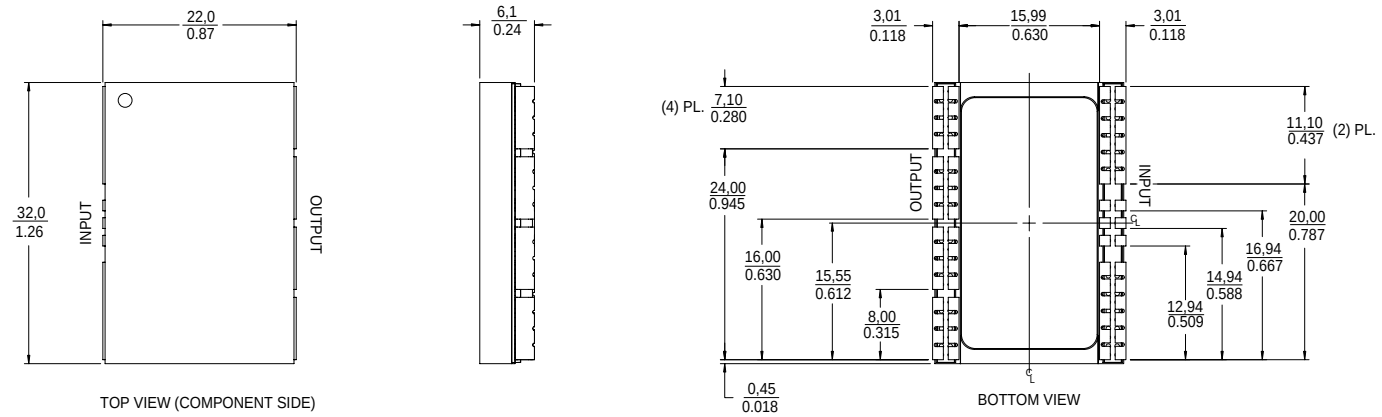


Figure 17*—BCM J-Lead mechanical outline; Onboard mounting*

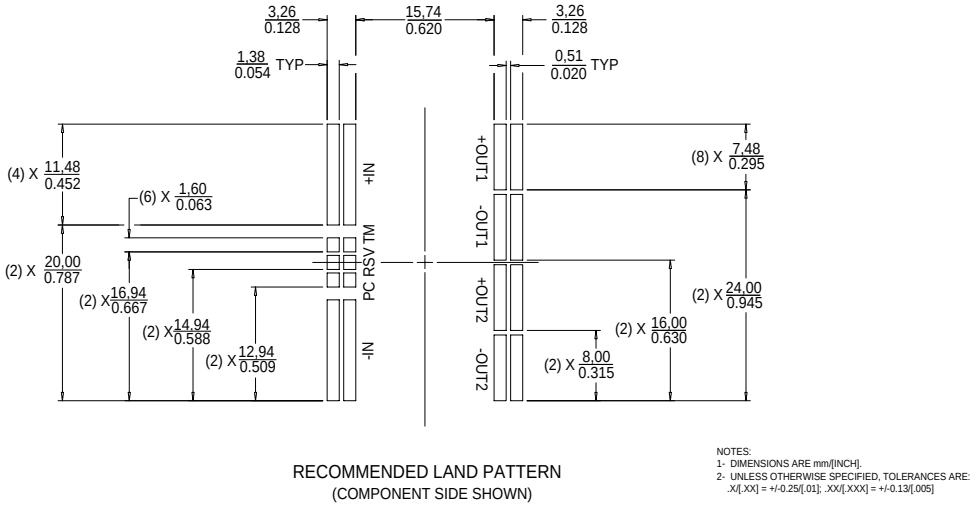


Figure 18*— BCM J-Lead PCB land layout information; Onboard mounting*

Configuration	Inboard(1) (Package K)	Onboard(1) (Package F)	Inboard with 0.25" Pin Fins(2)	Onboard with 0.25" Pin Fins(2)
Effective power density	1400 W/in³	880 W/in³	550 W/in³	440 W/in³
Junction-Board thermal resistance	2.1 °C/W	2.4 °C/W	2.1 °C/W	2.4 °C/W
Junction-Case thermal resistance	1.1 °C/W	1.1 °C/W	N/A	N/A
Junction-Ambient thermal resistance 300LFM	6.5 °C/W	6.8 °C/W	5.0 °C/W	5.0 °C/W

Notes:

(1) Surface mounted to a 2" x 2" FR4 board, 4 layers 2 oz Cu

(2) Pin Fin heat sink available as a separate item

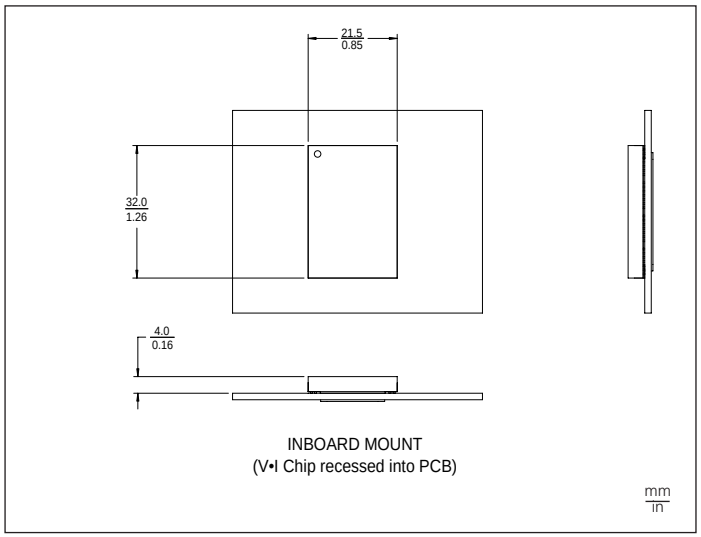


Figure 19*—Inboard mounting – package K*

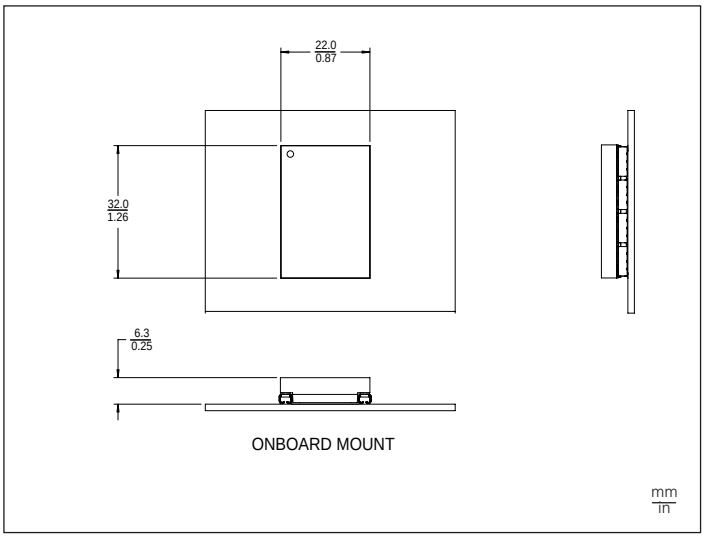


Figure 20*— Onboard mounting – package F*

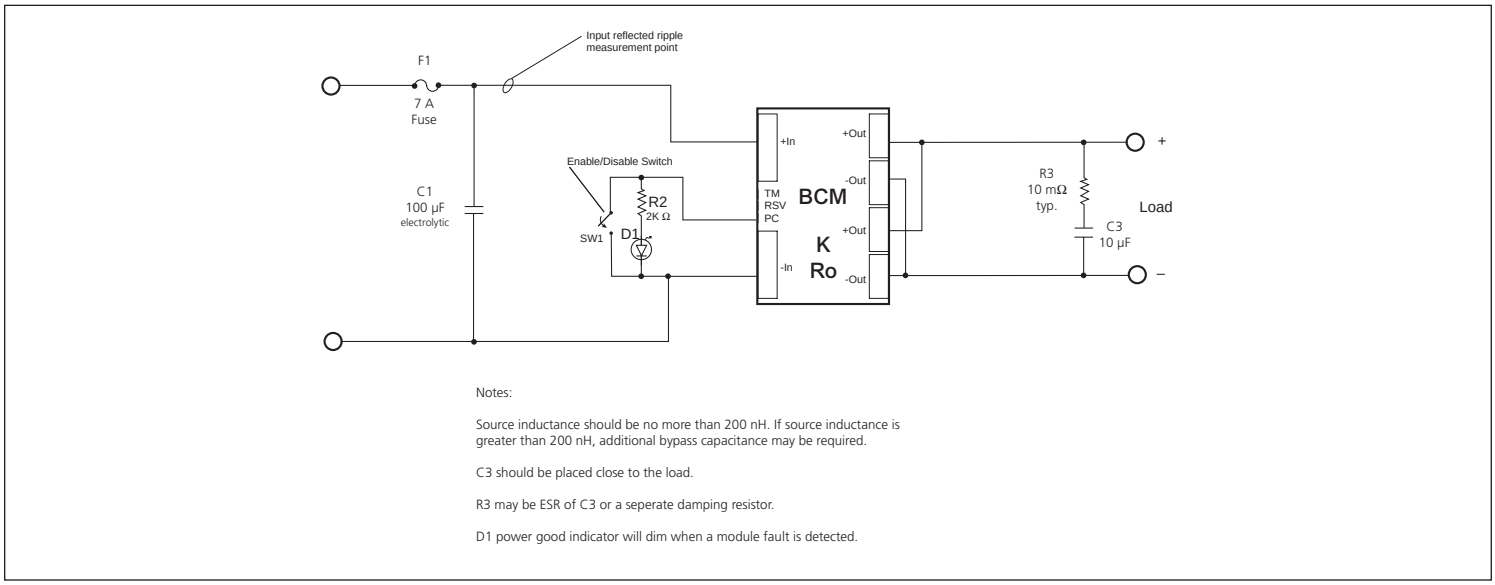


Figure 21*—BCM test circuit*

Parallel Operation

The BCM will inherently current share when operated in an array. Arrays may be used for higher power or redundancy in an application.

Current sharing accuracy is maximized when the source and load impedance presented to each BCM within an array are equal.

The recommended method to achieve matched impedances is to dedicate common copper planes within the PCB to deliver and return the current to the array, rather than rely upon traces of varying lengths. In typical applications the current being delivered to the load is larger than that sourced from the input, allowing traces to be utilized on the input side if necessary. The use of dedicated power planes is, however, preferable.

The BCM power train and control architecture allow bi-directional power transfer, including reverse power processing from the BCM output to its input. Reverse power transfer is enabled if the BCM input is within its operating range and the BCM is otherwise enabled. The BCM's ability to process power in reverse improves the BCM transient response to an output load dump.

Thermal Management

The high efficiency of the V•I Chip results in relatively low power dissipation and correspondingly low generation of heat. The heat generated within internal semiconductor junctions is coupled with low effective thermal resistances, $R\theta_{JC}$ and $R\theta_{JB}$, to the V•I Chip case and its Ball Grid Array allowing thermal management flexibility to adapt to specific application requirements (Figure 22).

CASE 1 Convection via optional Pin Fins to air.

If the application is in a typical environment with forced convection over the surface of the PCB and greater than 0.4" headroom, a simple thermal management strategy is to procure V•I Chips with the Pin Fin option. The total Junction-to-Ambient thermal resistance, $R\theta_{JA}$, of a surface mounted V•I Chip with optional 0.25" Pin Fins is 4.8 °C/W in 300 LFM air flow (Figure 24). At full rated output power of 240 W, the heat generated by the BCM is approximately 13 W (Figure 6). Therefore, the junction temperature rise to ambient is approximately 62°C. Given a maximum junction temperature of 125°C, a temperature rise of 62°C allows the V•I Chip to operate at rated output power at up to 63°C ambient temperature. At 100 W of output power, operating ambient temperature extends to 104°C.

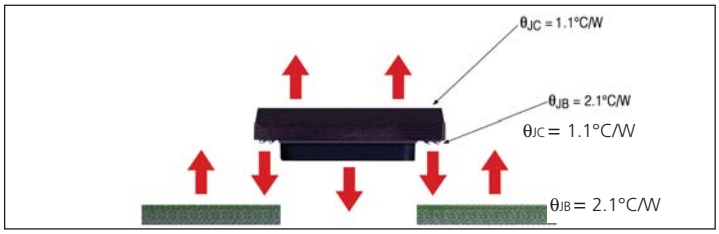


Figure 22—*Thermal resistance*

CASE 2—Conduction to the PCB

The low thermal resistance Junction-to-BGA, $R\theta_{JB}$, allows use of the PCB to exchange heat from the V•I Chip, including convection from the PCB to the ambient or conduction to a cold plate.

For example, with a V•I Chip surface mounted on a 2" x 2" area of a multi-layer PCB, with an aggregate 8 oz of effective copper weight, the total Junction-to-Ambient thermal resistance, $R\theta_{JA}$, is 6.5°C/W in 300 LFM air flow (see Thermal section, Page 6). Given a maximum junction temperature of 125°C and 13 W dissipation at 240 W of output power, a temperature rise of 85°C allows the V•I Chip to operate at rated output power at up to 40°C ambient temperature.

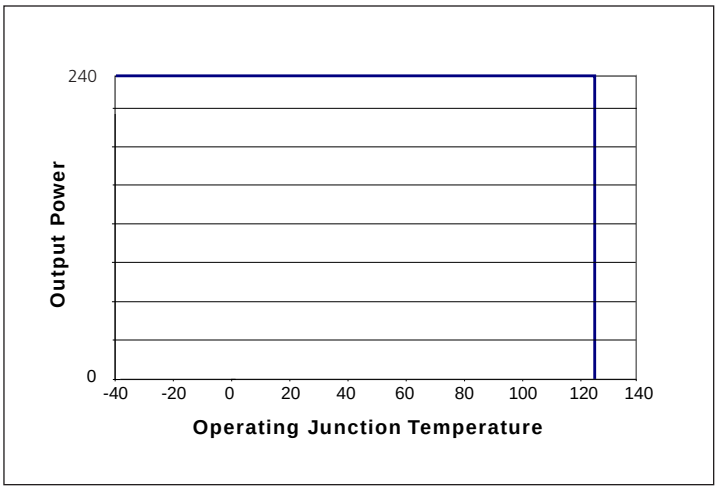


Figure 23— *Thermal derating curve*

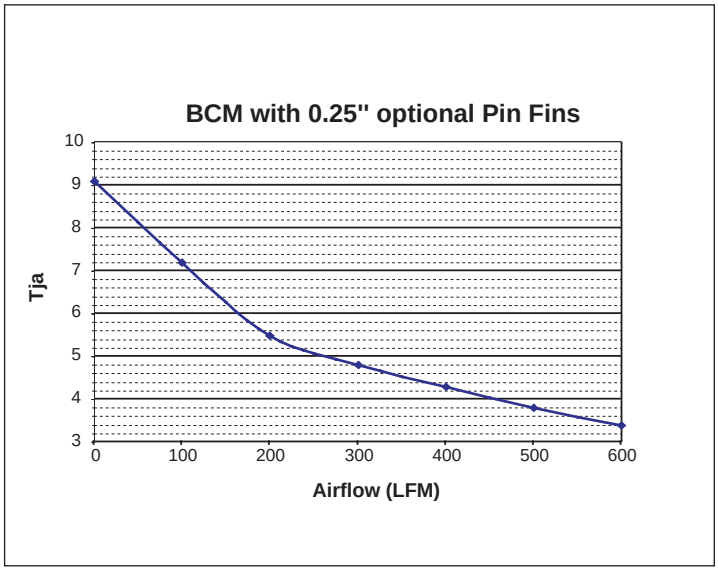


Figure 24—*Junction-to-ambient thermal resistance of BCM with 0.25" Pin Fins (Pin Fins available as a separate item.)*

The thermal resistance of the PCB to the surrounding environment in proximity to V•I Chips may be reduced by low profile heat sinks surface mounted to the PCB.The PCB may also be coupled to a cold plate by low thermal resistance standoff elements as a means of achieving effective cooling for an array of V•I Chips, without a direct interface to their case.

CASE 3—Combined direct convection to the air and conduction to the PCB.

Parallel use of the V•I Chip internal thermal resistances (including Junction-to-Case and Junction-to-BGA) in series with external thermal resistances provides an efficient thermal management strategy as it reduces total thermal resistance. This may be readily estimated as the parallel network of two pairs of series configured resistors.

V•I Chip Bus Converter Level 1 DC Behavioral Model for 48 V to 6 V, 240 W

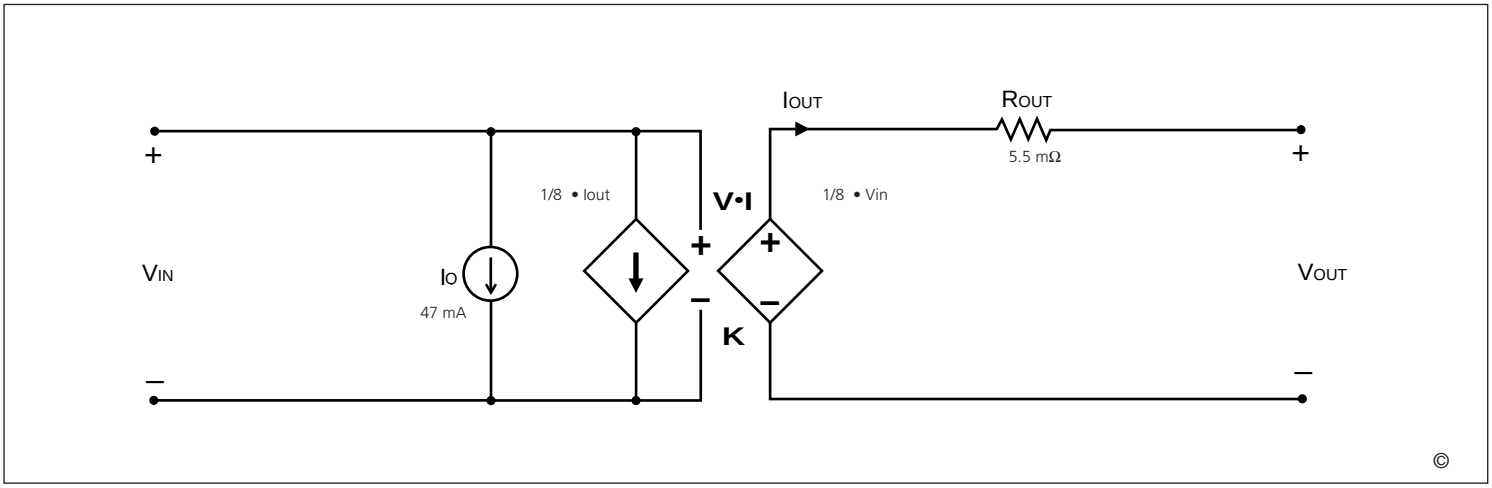


Figure 25*—This model characterizes the DC operation of the V•I Chip bus converter, including the converter transfer function and its losses. The model enables estimates or simulations of output voltage as a function of input voltage and output load, as well as total converter power dissipation or heat generation.*

V•I Chip Bus Converter Level 2 Transient Behavioral Model for 48 V to 6 V, 240 W

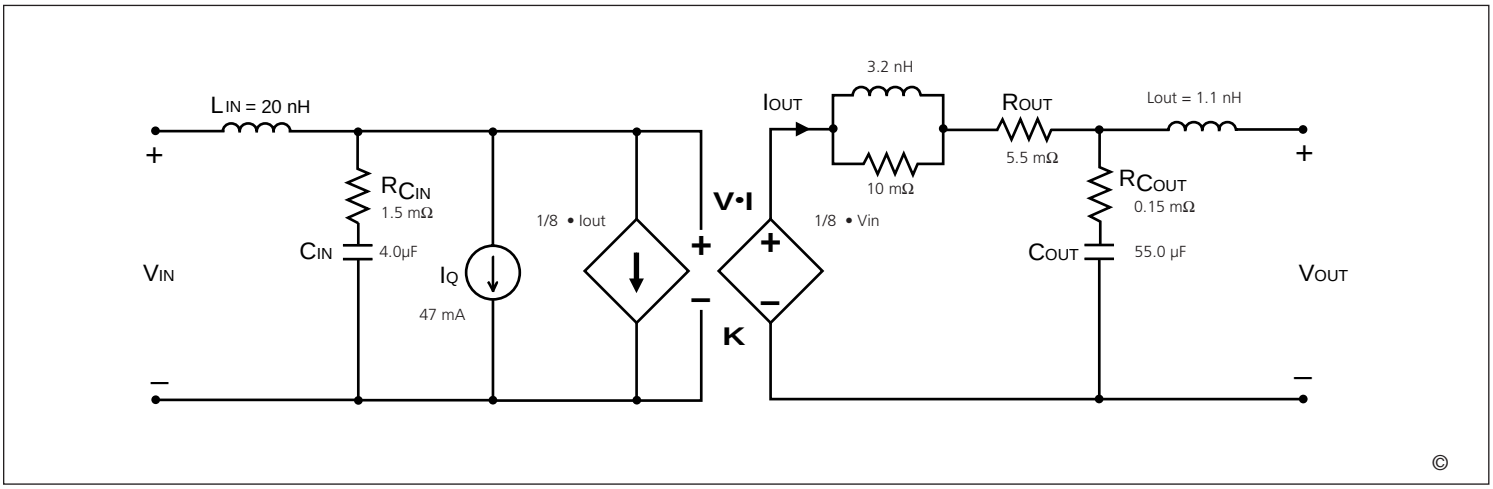


Figure 26*—This model characterizes the AC operation of the V•I Chip bus converter including response to output load or input voltage transients or steady state modulations. The model enables estimates or simulations of input and output voltages under transient conditions, including response to a stepped load with or without external filtering elements.*

Input Impedance Recommendations

To take full advantage of the BCM capabilities, the impedance presented to its input terminals must be low from DC to approximately 5 MHz. The source should exhibit low inductance (less than 100 nH) and should have a critically damped response. If the interconnect inductance exceeds 100 nH, the BCM input pins should be bypassed with an RC damper (e.g., 100 µF in series with 0.3 ohm) to retain low source impedance and stable operations. Given the wide bandwidth of the BCM, the source response is generally the limiting factor in the overall system response.

Anomalies in the response of the source will appear at the output of the BCM multiplied by its K factor. The DC resistance of the source should be kept as low as possible to minimize voltage deviations. This is especially important if the BCM is operated near low or high line as the over/under voltage detection circuitry could be activated.

Input Fuse Recommendations

V•I Chips are not internally fused in order to provide flexibility in configuring power systems. However, input line fusing of V•I Chips must always be incorporated within the power system. A fast acting fuse should be placed in series with the +IN port.

Application Circuits

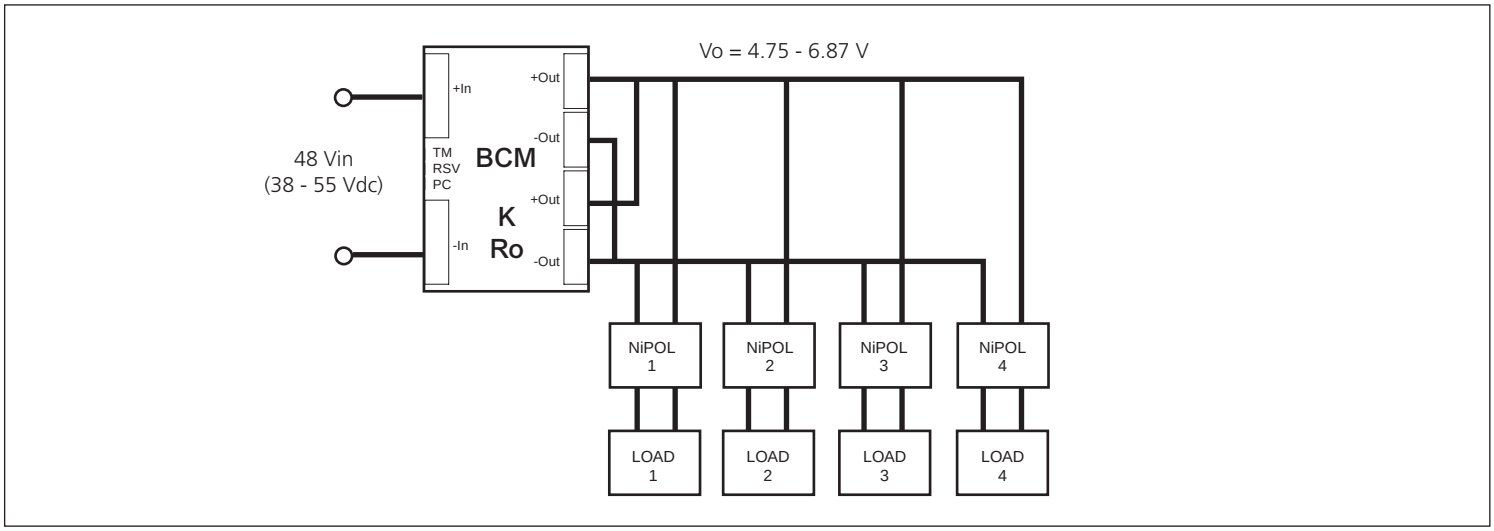


Figure 27*—The BCM provides an isolated output from a narrow range input ideal for driving non-isolated point of load converters (niPOLs)*

In the following figure;

K = BCM Transformation Ratio
R_O = BCM Output Resistance
V_O = BCM Output
V_f = PRM Output (Factorized Bus Voltage)
V_L = Desired Load Voltage
V_S = PRM Output Set Point Voltage

FPA Local Loop

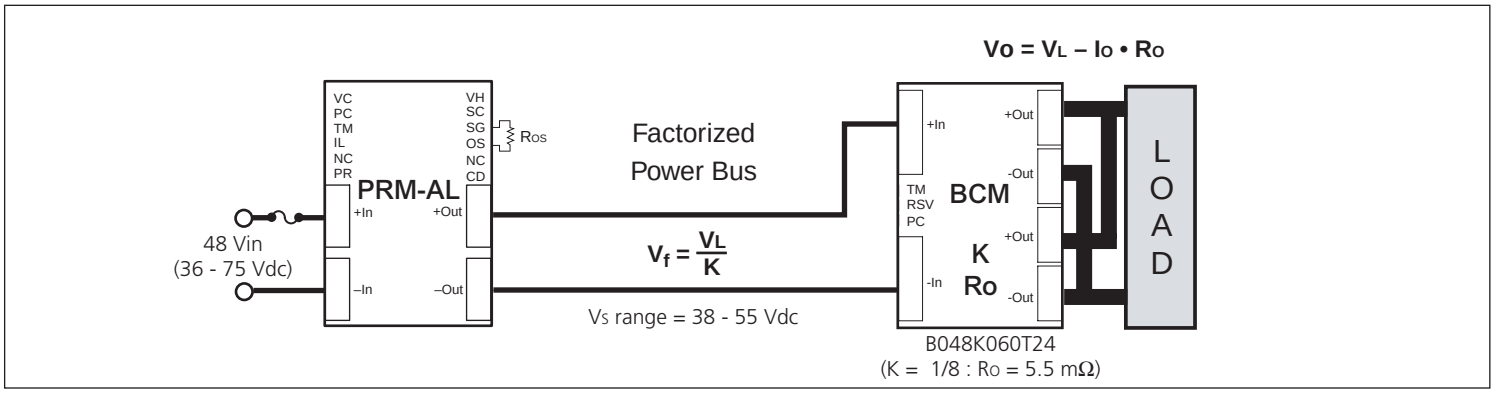


Figure 28*—The PRM regulates its output to provide a constant factorized bus voltage. The output voltage is the nominal load voltage, Vo, at no load and decreases with load at a constant rate equal to the BCM output resistance Ro.*

V•I Chip soldering recommendations

V•I Chip modules are intended for reflow soldering processes. The following information defines the processing conditions required for successful attachment of a V•I Chip to a PCB. Failure to follow the recommendations provided can result in aesthetic or functional failure of the module.

Storage

V•I Chip modules are currently rated at MSL 5. Exposure to ambient conditions for more than 72 hours requires a 24 hour bake at 125ºC to remove moisture from the package.

Solder paste stencil design

Solder paste is recommended for a number of reasons, including overcoming minor solder sphere co-planarity issues as well as simpler integration into overall SMD process.

63/37 SnPb, either no-clean or water-washable, solder paste should be used. Pb-free development is underway.

The recommended stencil thickness is 6 mils. The apertures should be 20 mils in diameter for the Inboard (BGA) application and 0.9-0.9:1 for the Onboard (J-Leaded).

Pick and place

Inboard (BGA) modules should be placed as accurately as possible to minimize any skewing of the solder joint; a maximum offset of 10 mils is allowable. Onboard (J-Leaded) modules should be placed within ±5 mils.

To maintain placement position, the modules should not be subjected to acceleration greater than 500 in/sec^2 prior to reflow.

Reflow

There are two temperatures critical to the reflow process; the solder joint temperature and the module's case temperature. The solder joint's temperature should reach at least 220ºC, with a time above liquidus (183ºC) of ~30 seconds.

The module's case temperature must not exceed 208 ºC at anytime during reflow.

Because of the ΔT needed between the pin and the case, a forced-air convection oven is preferred for reflow soldering. This reflow method generally transfers heat from the PCB to the solder joint. The module's large mass also reduces its temperature rise. Care should be taken to prevent smaller devices from excessive temperatures. Reflow of modules onto a PCB using Air-Vac-type equipment is not recommended due to the high temperature the module will experience.

Inspection

For the BGA-version, a visual examination of the post-reflow solder joints should show relatively columnar solder joints with no bridges. An inspection using x-ray equipment can be done, but the module's materials may make imaging difficult.

The J-Lead versions solder joints should conform to IPC 12.2

- Properly wetted fillet must be evident.
- Heel fillet height must exceed lead thickness plus solder thickness.

Removal and rework

V•I Chip modules can be removed from PCBs using special tools such as those made by Air-Vac. These tools heat a very localized region of the board with a hot gas while applying a tensile force to the component (using vacuum). Prior to component heating and removal, the entire board should be heated to 80-100ºC to decrease the component heating time as well as local PCB warping. If there are adjacent moisture-sensitive components, a 125ºC bake should be used prior to component removal to prevent popcorning. V•I Chip modules should not be expected to survive a removal operation.

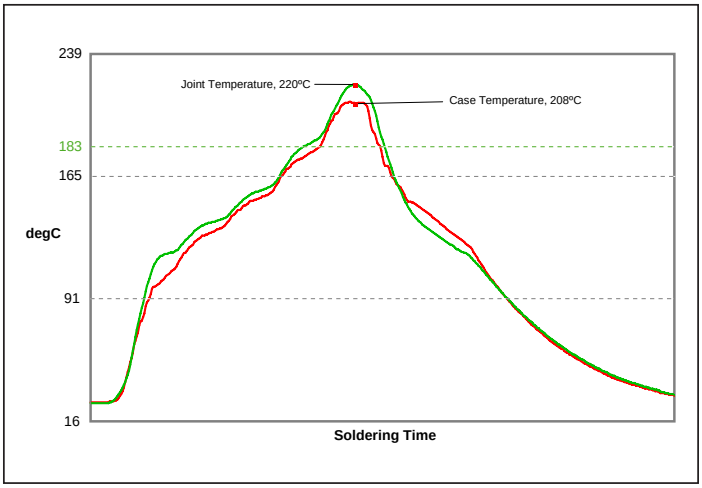


Figure 29—*Thermal profile diagram*

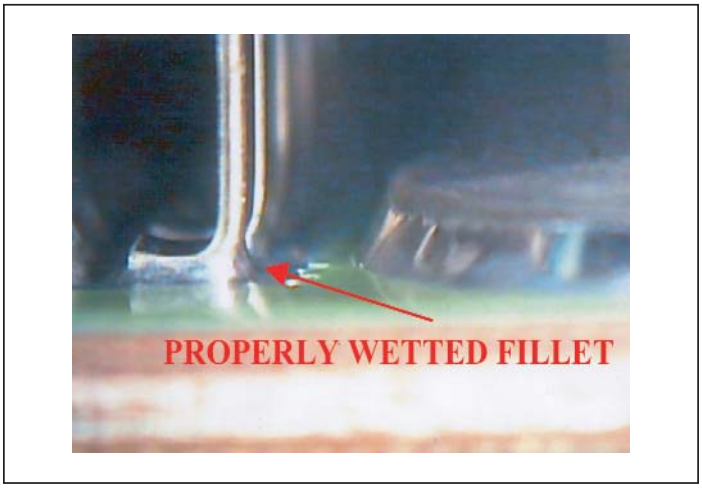


Figure 30— *Properly reflowed V•I Chip J-Lead*

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