



16 Mbit Concurrent SuperFlash + 2/4/8 Mbit SRAM ComboMemory

SST34HF1602C / SST34HF1622C / SST34HF1642C
SST34HF1642D / SST34HF1682D / SST34HF1622S / SST34HF1642S

Advance Information

FEATURES:

- **Flash Organization: 1M x16 or 2M x8**
- **Dual-Bank Architecture for Concurrent Read/Write Operation**
 - 16 Mbit: 4 Mbit + 12 Mbit
- **(P)SRAM Organization:**
 - 2 Mbit: 128K x16 or 256K x8
 - 4 Mbit: 256K x16 or 512K x8
 - 8 Mbit: 512K x16 or 1024K x8
- **Single 2.7-3.3V Read and Write Operations**
- **Superior Reliability**
 - Endurance: 100,000 Cycles (typical)
 - Greater than 100 years Data Retention
- **Low Power Consumption:**
 - Active Current: 25 mA (typical)
 - Standby Current: 20 μ A (typical)
- **Hardware Sector Protection (WP#)**
 - Protects 4 outer most sectors (4 KWord) in the larger bank by holding WP# low and unprotects by holding WP# high
- **Hardware Reset Pin (RST#)**
 - Resets the internal state machine to reading data array
- **Byte Selection for Flash (CIOF pin)**
 - Selects 8-bit or 16-bit mode
- **Sector-Erase Capability**
 - Uniform 2 KWord sectors
- **Block-Erase Capability**
 - Uniform 32 KWord blocks
- **Read Access Time**
 - Flash: 70 ns
 - (P)SRAM: 70 ns
- **Erase-Suspend / Erase-Resume Capabilities**
- **Security ID Feature**
 - SST: 128 bits
 - User: 128 bits
- **Latched Address and Data**
- **Fast Erase and Word-/Byte-Program (typical):**
 - Sector-Erase Time: 18 ms
 - Block-Erase Time: 18 ms
 - Chip-Erase Time: 35 ms
 - Word-Program Time: 7 μ s
- **Automatic Write Timing**
 - Internal V_{PP} Generation
- **End-of-Write Detection**
 - Toggle Bit
 - Data# Polling
 - Ready/Busy# pin
- **CMOS I/O Compatibility**
- **JEDEC Standard Command Set**
- **Packages Available**
 - 56-ball LFBGA (8mm x 10mm)
 - 62-ball LFBGA (8mm x 10mm)

PRODUCT DESCRIPTION

The SST34HF16x2C/D/S ComboMemory devices integrate either a 1M x16 or 2M x8 CMOS flash memory bank with either a 128K x16/256K x8, 256K x16/512 x8, or 512K x16/1024K x8 CMOS SRAM or pseudo SRAM (PSRAM) memory bank in a multi-chip package (MCP). These devices are fabricated using SST's proprietary, high-performance CMOS SuperFlash technology incorporating the split-gate cell design and thick-oxide tunneling injector to attain better reliability and manufacturability compared with alternate approaches. The SST34HF16x2C/D/S devices are ideal for applications such as cellular phones, GPS devices, PDAs, and other portable electronic devices in a low power and small form factor system.

The SST34HF16x2C/D/S feature dual flash memory bank architecture allowing for concurrent operations between the two flash memory banks and the (P)SRAM. The devices can read data from either bank while an Erase or Program operation is in progress in the opposite bank. The two flash

memory banks are partitioned into 4 Mbit and 12 Mbit with top sector protection options for storing boot code, program code, configuration/parameter data and user data.

The SuperFlash technology provides fixed Erase and Program times, independent of the number of Erase/Program cycles that have occurred. Therefore, the system software or hardware does not have to be modified or de-rated as is necessary with alternative flash technologies, whose Erase and Program times increase with accumulated Erase/Program cycles. The SST34HF16x2C/D/S devices offer a guaranteed endurance of 10,000 cycles. Data retention is rated at greater than 100 years. With high performance Word-Program, the flash memory banks provide a typical Word-Program time of 7 μ sec. The entire flash memory bank can be erased and programmed word-by-word in typically 4 seconds for the SST34HF16x2C/D/S, when using interface features such as Toggle Bit, Data# Polling, or RY/BY# to indicate the completion of Program operation. To





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protect against inadvertent flash write, the SST34HF16x2C/D/S devices contain on-chip hardware and software data protection schemes.

The flash and (P)SRAM operate as two independent memory banks with respective bank enable signals. The memory bank selection is done by two bank enable signals. The (P)SRAM bank enable signals, BES1# and BES2, select the (P)SRAM bank (BES1# and BES2 are NC for SST34HF1602C). The flash memory bank enable signal, BEF#, has to be used with Software Data Protection (SDP) command sequence when controlling the Erase and Program operations in the flash memory bank. The memory banks are superimposed in the same memory address space where they share common address lines, data lines, WE# and OE# which minimize power consumption and area.

Designed, manufactured, and tested for applications requiring low power and small form factor, the SST34HF16x2C/D/S are offered in both commercial and extended temperatures and a small footprint package to meet board space constraint requirements. See Figures 3 and 4 for pin assignments.

Device Operation

The SST34HF16x2C/D/S uses BES1#, BES2 and BEF# to control operation of either the flash or the (P)SRAM memory bank. When BEF# is low, the flash bank is activated for Read, Program or Erase operation. When BES1# is low, and BES2 is high the (P)SRAM is activated for Read and Write operation. BEF# and BES1# cannot be at low level, and BES2 cannot be at high level at the same time. **If all bank enable signals are asserted, bus contention will result and the device may suffer permanent damage.** All address, data, and control lines are shared by flash and (P)SRAM memory banks which minimizes power consumption and loading. The device goes into standby when BEF# and BES1# bank enables are raised to V_{IHc} (Logic High) or when BEF# is high and BES2 is low.

Concurrent Read/Write Operation

Dual bank architecture of SST34HF16x2C/D/S devices allows the Concurrent Read/Write operation whereby the user can read from one bank while programming or erasing in the other bank. This operation can be used when the user needs to read system code in one bank while updating data in the other bank. See Figures 1 and 2 for dual-bank memory organization.

CONCURRENT READ/WRITE STATES

Flash		(P)SRAM
Bank 1	Bank 2	
Read	Write	No Operation
Write	Read	No Operation
Write	No Operation	Read
No Operation	Write	Read
Write	No Operation	Write
No Operation	Write	Write

Note: For the purposes of this table, write means to Block-, Sector, or Chip-Erase, or Word-/Byte-Program as applicable to the appropriate bank.

Flash Read Operation

The Read operation of the SST34HF16x2C/D/S is controlled by BEF# and OE#, both have to be low for the system to obtain data from the outputs. BEF# is used for device selection. When BEF# is high, the chip is deselected and only standby power is consumed. OE# is the output control and is used to gate data from the output pins. The data bus is in high impedance state when either BEF# or OE# is high. Refer to the Read cycle timing diagram for further details (Figure 8).

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Flash Word-/Byte-Program Operation

These devices are programmed on a word-by-word or byte-by-byte basis depending on the state of the CIOF pin. Before programming, one must ensure that the sector which is being programmed is fully erased.

The Program operation is accomplished in three steps:

1. Software Data Protection is initiated using the three-byte load sequence.
2. Word address and word data are loaded.

During the Word-Program operation, the addresses are latched on the falling edge of either BEF# or WE#, whichever occurs last. The data is latched on the rising edge of either BEF# or WE#, whichever occurs first.

3. The internal Program operation is initiated after the rising edge of the fourth WE# or BEF#, whichever occurs first. The Program operation, once initiated, will be completed typically within 7 μ s.

See Figures 9 and 10 for WE# and BEF# controlled Program operation timing diagrams and Figure 22 for flowcharts. During the Program operation, the only valid reads are Data# Polling and Toggle Bit. During the internal Program operation, the host is free to perform additional tasks. Any commands issued during an internal Program operation are ignored.

Flash Sector- (Block-) Erase Operation

These devices offer both Sector-Erase and Block-Erase operations. These operations allow the system to erase the devices on a sector-by-sector (or block-by-block) basis. The sector architecture is based on a uniform sector size of 2 KWord. The Block-Erase mode is based on a uniform block size of 32 KWord. The Sector-Erase operation is initiated by executing a six-byte command sequence with a Sector-Erase command (30H) and sector address (SA) in the last bus cycle. The Block-Erase operation is initiated by executing a six-byte command sequence with Block-Erase command (50H) and block address (BA) in the last bus cycle. The sector or block address is latched on the falling edge of the sixth WE# pulse, while the command (30H or 50H) is latched on the rising edge of the sixth WE# pulse. The internal Erase operation begins after the sixth WE# pulse. Any commands issued during the Block- or Sector-Erase operation are ignored except Erase-Suspend and Erase-Resume. See Figures 14 and 15 for timing waveforms.

Flash Chip-Erase Operation

The SST34HF16x2C/D/S provide a Chip-Erase operation, which allows the user to erase all sectors/blocks to the "1" state. This is useful when the device must be quickly erased.

The Chip-Erase operation is initiated by executing a six-byte command sequence with Chip-Erase command (10H) at address 5555H in the last byte sequence. The Erase operation begins with the rising edge of the sixth WE# or BEF#, whichever occurs first. During the Erase operation, the only valid read is Toggle Bits or Data# Polling. See Table 7 for the command sequence, Figure 13 for timing diagram, and Figure 26 for the flowchart. Any commands issued during the Chip-Erase operation are ignored. When WP# is low, any attempt to Chip-Erase will be ignored.

Flash Erase-Suspend/-Resume Operations

The Erase-Suspend operation temporarily suspends a Sector- or Block-Erase operation thus allowing data to be read from any memory location, or program data into any sector/block that is not suspended for an Erase operation. The operation is executed by issuing a one-byte command sequence with Erase-Suspend command (B0H). The device automatically enters read mode within 20 μ s after the Erase-Suspend command had been issued. Valid data can be read from any sector or block that is not suspended from an Erase operation. Reading at address location within erase-suspended sectors/blocks will output DQ₂ toggling and DQ₆ at "1". While in Erase-Suspend mode, a Word-/Byte-Program operation is allowed except for the sector or block selected for Erase-Suspend. To resume Sector-Erase or Block-Erase operation which has been suspended, the system must issue an Erase-Resume command. The operation is executed by issuing a one-byte command sequence with Erase Resume command (30H) at any address in the one-byte sequence.



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Flash Write Operation Status Detection

The SST34HF16x2C/D/S provide one hardware and two software means to detect the completion of a Write (Program or Erase) cycle, in order to optimize the system Write cycle time. The hardware detection uses the Ready/Busy# (RY/BY#) pin. The software detection includes two status bits: Data# Polling (DQ₇) and Toggle Bit (DQ₆). The End-of-Write detection mode is enabled after the rising edge of WE#, which initiates the internal Program or Erase operation.

The actual completion of the nonvolatile write is asynchronous with the system; therefore, either a Ready/Busy# (RY/BY#), Data# Polling (DQ₇) or Toggle Bit (DQ₆) read may be simultaneous with the completion of the Write cycle. If this occurs, the system may possibly get an erroneous result, i.e., valid data may appear to conflict with either DQ₇ or DQ₆. In order to prevent spurious rejection, if an erroneous result occurs, the software routine should include a loop to read the accessed location an additional two (2) times. If both reads are valid, then the device has completed the Write cycle, otherwise the rejection is valid.

Ready/Busy# (RY/BY#)

The SST34HF16x2C/D/S include a Ready/Busy# (RY/BY#) output signal. RY/BY# is an open drain output pin that indicates whether an Erase or Program operation is in progress. Since RY/BY# is an open drain output, it allows several devices to be tied in parallel to V_{DD} via an external pull-up resistor. After the rising edge of the final WE# pulse in the command sequence, the RY/BY# status is valid.

When RY/BY# is actively pulled low, it indicates that an Erase or Program operation is in progress. When RY/BY# is high (Ready), the devices may be read or left in standby mode.

Byte/Word (CIOF)

The device includes a CIOF pin to control whether the device data I/O pins operate x8 or x16. If the CIOF pin is at logic "1" (V_{IH}) the device is in x16 data configuration: all data I/O pins DQ₀-DQ₁₅ are active and controlled by BEF# and OE#.

If the CIOF pin is at logic "0", the device is in x8 data configuration: only data I/O pins DQ₀-DQ₇ are active and controlled by BEF# and OE#. The remaining data pins DQ₈-DQ₁₄ are at Hi-Z, while pin DQ₁₅ is used as the address input A₋₁ for the Least Significant Bit of the address bus.

Flash Data# Polling (DQ₇)

When the devices are in an internal Program operation, any attempt to read DQ₇ will produce the complement of the true data. Once the Program operation is completed, DQ₇ will produce true data. During internal Erase operation, any attempt to read DQ₇ will produce a '0'. Once the internal Erase operation is completed, DQ₇ will produce a '1'. The Data# Polling is valid after the rising edge of fourth WE# (or BEF#) pulse for Program operation. For Sector-, Block-, or Chip-Erase, the Data# Polling is valid after the rising edge of sixth WE# (or BEF#) pulse. See Figure 11 for Data# Polling (DQ₇) timing diagram and Figure 23 for a flowchart.

Toggle Bits (DQ₆ and DQ₂)

During the internal Program or Erase operation, any consecutive attempts to read DQ₆ will produce alternating "1"s and "0"s, i.e., toggling between 1 and 0. When the internal Program or Erase operation is completed, the DQ₆ bit will stop toggling. The device is then ready for the next operation. The toggle bit is valid after the rising edge of the fourth WE# (or BEF#) pulse for Program operations. For Sector-, Block-, or Chip-Erase, the toggle bit (DQ₆) is valid after the rising edge of sixth WE# (or BEF#) pulse. DQ₆ will be set to "1" if a Read operation is attempted on an Erase-suspended Sector/Block. If Program operation is initiated in a sector/block not selected in Erase-Suspend mode, DQ₆ will toggle.

An additional Toggle Bit is available on DQ₂, which can be used in conjunction with DQ₆ to check whether a particular sector is being actively erased or erase-suspended. Table 1 shows detailed status bit information. The Toggle Bit (DQ₂) is valid after the rising edge of the last WE# (or BEF#) pulse of a Write operation. See Figure 12 for Toggle Bit timing diagram and Figure 23 for a flowchart.

TABLE 1: WRITE OPERATION STATUS

Status		DQ ₇	DQ ₆	DQ ₂	RY/BY#
Normal Operation	Standard Program	DQ ₇ #	Toggle	No Toggle	0
	Standard Erase	0	Toggle	Toggle	0
Erase-Suspend Mode	Read From Erase Suspended Sector/Block	1	1	Toggle	1
	Read From Non-Erase Suspended Sector/Block	Data	Data	Data	1
	Program	DQ ₇ #	Toggle	N/A	0

T1.0 1256

Note: DQ₇, DQ₆, and DQ₂ require a valid address when reading status information.

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Data Protection

The SST34HF16x2C/D/S provide both hardware and software features to protect nonvolatile data from inadvertent writes.

Hardware Data Protection

Noise/Glitch Protection: A WE# or BEF# pulse of less than 5 ns will not initiate a Write cycle.

V_{DD} Power Up/Down Detection: The Write operation is inhibited when V_{DD} is less than 1.5V.

Write Inhibit Mode: Forcing OE# low, BEF# high, or WE# high will inhibit the Write operation. This prevents inadvertent writes during power-up or power-down.

Hardware Block Protection

The SST34HF16x2C/D/S provide a hardware block protection which protects the outermost 8 KWord in Bank 1. The block is protected when WP# is held low. See Figures 1 and 2 for Block-Protection location.

A user can disable block protection by driving WP# high thus allowing erase or program of data into the protected sectors. WP# must be held high prior to issuing the write command and remain stable until after the entire Write operation has completed.

Hardware Reset (RST#)

The RST# pin provides a hardware method of resetting the device to read array data. When the RST# pin is held low for at least T_{RP}, any in-progress operation will terminate and return to Read mode (see Figure 19). When no internal Program/Erase operation is in progress, a minimum period of T_{RHR} is required after RST# is driven high before a valid Read can take place (see Figure 18).

The Erase operation that has been interrupted needs to be reinitiated after the device resumes normal operation mode to ensure data integrity. See Figures 18 and 19 for timing diagrams.

Software Data Protection (SDP)

The SST34HF16x2C/D/S provide the JEDEC standard Software Data Protection scheme for all data alteration operations, i.e., Program and Erase. Any Program operation requires the inclusion of the three-byte sequence. The three-byte load sequence is used to initiate the Program operation, providing optimal protection from inadvertent Write operations, e.g., during the system power-up or power-down. Any Erase operation requires the inclusion of six-byte sequence. The SST34HF16x2C/D/S are shipped with the Software Data Protection permanently enabled. See Table 7 for the specific software command codes. During SDP command sequence, invalid commands will abort the device to Read mode within T_{RC}. The contents of DQ₁₅-DQ₈ are “Don't Care” during any SDP command sequence.

Security ID

The SST34HF16x2C/D/S devices offer a 256-bit Security ID space. The Secure ID space is divided into two 128-bit segments—one factory programmed segment and one user programmed segment. The first segment is programmed and locked at SST with a unique, 128-bit number. The user segment is left un-programmed for the customer to program as desired. To program the user segment of the Security ID, the user must use the Security ID Word-Program command. End-of-Write status is checked by reading the toggle bits. Data# Polling is not used for Security ID End-of-Write detection. Once programming is complete, the Sec ID should be locked using the User-Sec-ID-Program-Lock-Out. This disables any future corruption of this space. Note that regardless of whether or not the Sec ID is locked, neither Sec ID segment can be erased. The Secure ID space can be queried by executing a three-byte command sequence with Query-Sec-ID command (88H) at address 5555H in the last byte sequence. To exit this mode, the Exit-Sec-ID command should be executed. Refer to Table 7 for more details.



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Product Identification

The Product Identification mode identifies the device as the SST34HF16x2C/D/S and manufacturer as SST. This mode may be accessed by software operations only. The hardware device ID Read operation, which is typically used by programmers cannot be used on this device because of the shared lines between flash and (P)SRAM in the multi-chip package. Therefore, application of high voltage to pin A₉ may damage this device. Users may use the software Product Identification operation to identify the part (i.e., using the device ID) when using multiple manufacturers in the same socket. For details, see Tables 4 and 7 for software operation, Figure 16 for the Software ID Entry and Read timing diagram and Figure 24 for the ID Entry command sequence flowchart.

TABLE 2: PRODUCT IDENTIFICATION

	ADDRESS	DATA
Manufacturer's ID	BK0000H	00BFH
Device ID SST34HF16x2C/D/S	BK0001H	734AH

T2.0 1256

Note: BK = Bank Address (A₁₉-A₁₈)

Product Identification Mode Exit

In order to return to the standard Read mode, the Software Product Identification mode must be exited. Exit is accomplished by issuing the Software ID Exit command sequence, which returns the device to the Read mode. This command may also be used to reset the device to the Read mode after any inadvertent transient condition that apparently causes the device to behave abnormally, e.g., not read correctly. Please note that the Software ID Exit command is ignored during an internal Program or Erase operation. See Table 7 for software command codes, Figure 17 for timing waveform and Figure 24 for a flowchart.

(P)SRAM Operation

With BES1# low, BES2 and BEF# high, the SST34HF16x2C/D/S operate as either 128K x16, 256K x16, or 512K x16 CMOS (P)SRAM, with fully static operation requiring no external clocks or timing strobes. The SST34HF16x2C/D/S (P)SRAM is mapped into the first 512 KWord address space. When BES1#, BEF# are high and BES2 is low, all memory banks are deselected and the device enters standby. Read and Write cycle times are equal. The control signals UBS# and LBS# provide access to the upper data byte and lower data byte (UBS# and LBS# signals are NC for SST3416x2S parts). See Table 4 for x16 (P)SRAM Read and Write data byte control modes of operation. See Table 5 for x8 SRAM Read and Write data byte control modes of operation.

(P)SRAM Read

The (P)SRAM Read operation of the SST34HF16x2C/D/S is controlled by OE# and BES1#, both have to be low with WE# and BES2 high for the system to obtain data from the outputs. BES1# and BES2 are used for (P)SRAM bank selection. OE# is the output control and is used to gate data from the output pins. The data bus is in high impedance state when OE# is high. Refer to the Read cycle timing diagram, Figure 5, for further details.

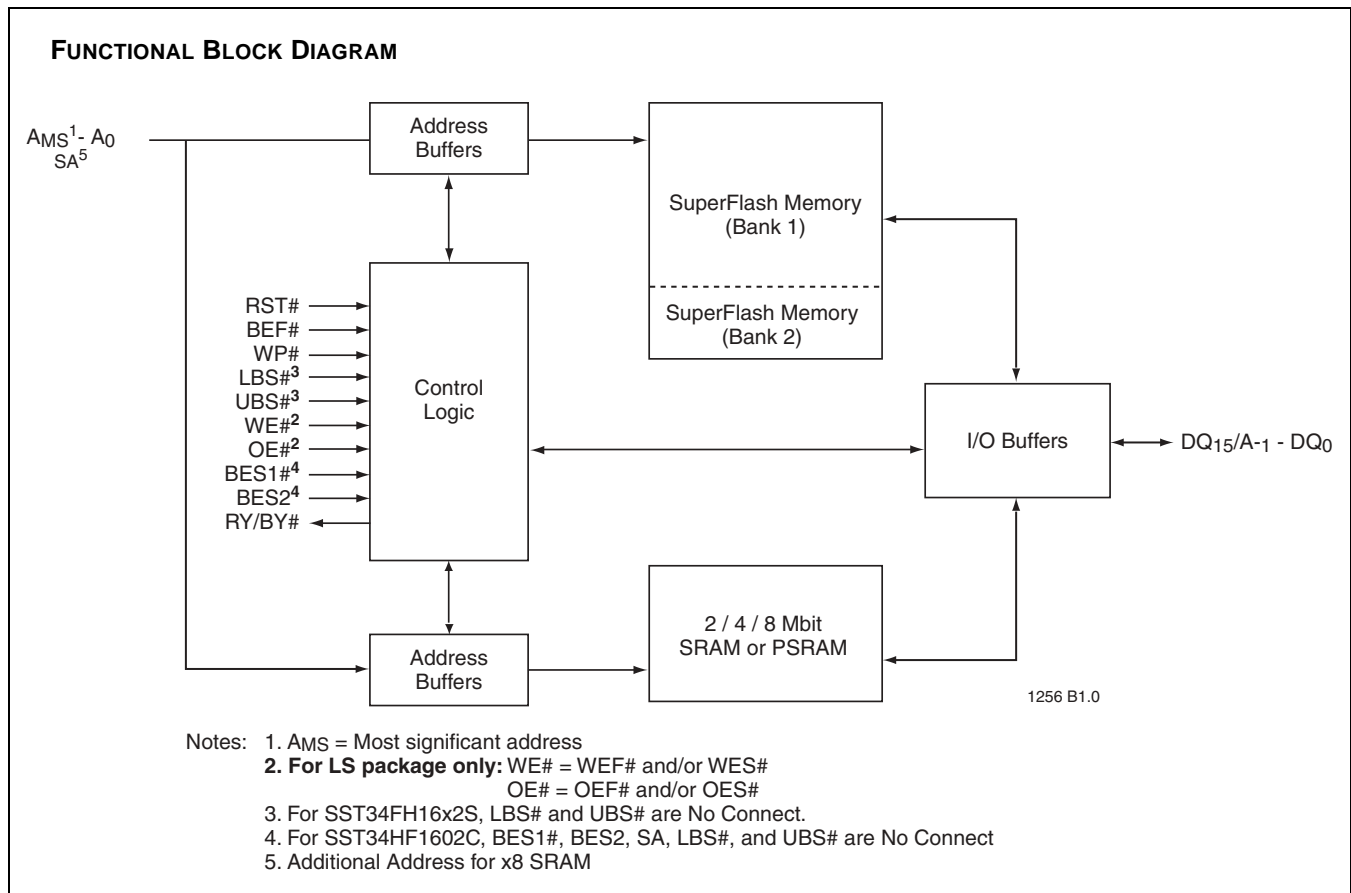
(P)SRAM Write

The (P)SRAM Write operation of the SST34HF16x2C/D/S is controlled by WE# and BES1#, both have to be low, BES2 must be high for the system to write to the (P)SRAM. During the Word-Write operation, the addresses and data are referenced to the rising edge of either BES1#, WE#, or the falling edge of BES2 whichever occurs first. The write time is measured from the last falling edge of BES#1 or WE# or the rising edge of BES2 to the first rising edge of BES1#, or WE# or the falling edge of BES2. Refer to the Write cycle timing diagrams, Figures 6 and 7, for further details.

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Top Block Protection; 32 KWord Blocks; 2 KWord Sectors

8 KWord Block Protection
 (4 - 2 KWord Sectors)

FFFFFH FE000H	Block 31	Bank 2	
FDFFFFH F8000H			
F7FFFFH F0000H	Block 30		
EFFFFFH E8000H	Block 29		
E7FFFFH E0000H	Block 28		
DFFFFFH D8000H	Block 27		
D7FFFFH D0000H	Block 26		
CFFFFFH C8000H	Block 25		
C7FFFFH C0000H	Block 24		
BFFFFFH B8000H	Block 23		
B7FFFFH B0000H	Block 22		
AFFFFFH A8000H	Block 21		
A7FFFFH A0000H	Block 20		
9FFFFFH 98000H	Block 19		
97FFFFH 90000H	Block 18		
8FFFFFH 88000H	Block 17		
87FFFFH 80000H	Block 16		
7FFFFFH 78000H	Block 15		
77FFFFH 70000H	Block 14		
6FFFFFH 68000H	Block 13		
67FFFFH 60000H	Block 12		
5FFFFFH 58000H	Block 11		
57FFFFH 50000H	Block 10		
4FFFFFH 48000H	Block 9		
47FFFFH 40000H	Block 8		
3FFFFFH 38000H	Block 7		Bank 1
37FFFFH 30000H	Block 6		
2FFFFFH 28000H	Block 5		
27FFFFH 20000H	Block 4		
1FFFFFH 18000H	Block 3		
17FFFFH 10000H	Block 2		
0FFFFFH 08000H	Block 1		
07FFFFH 00000H	Block 0		

1256 F01.0

Note: The address input range in x16 mode (BYTE#=#V_{IH}) is A₁₉-A₀

FIGURE 1: SST34HF16x2C/D, CONCURRENT SUPERFLASH DUAL-BANK MEMORY ORGANIZATION

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Top Block Protection; 64 KByte Blocks; 4 KByte Sectors

16 KByte Block Protection
 (4 - 4 KByte Sectors)

1FFFFFFH 1FC000H	Block 31	Bank 2	
1FBFFFH 1F0000H			
1EFFFFH 1E0000H	Block 30		
1DFFFFH 1D0000H	Block 29		
1CFFFFH 1C0000H	Block 28		
1BFFFFH 1B0000H	Block 27		
1AFFFFH 1A0000H	Block 26		
19FFFFH 190000H	Block 25		
18FFFFH 180000H	Block 24		
17FFFFH 170000H	Block 23		
16FFFFH 160000H	Block 22		
15FFFFH 150000H	Block 21		
14FFFFH 140000H	Block 20		
13FFFFH 130000H	Block 19		
12FFFFH 120000H	Block 18		
11FFFFH 110000H	Block 17		
10FFFFH 100000H	Block 16		
0FFFFFFH 0F0000H	Block 15		
0EFFFFH 0E0000H	Block 14		
0DFFFFH 0D0000H	Block 13		
0CFFFFH 0C0000H	Block 12		
0BFFFFH 0B0000H	Block 11		
0AFFFFH 0A0000H	Block 10		
09FFFFH 090000H	Block 9		
08FFFFH 080000H	Block 8		
07FFFFH 070000H	Block 7		Bank 1
06FFFFH 060000H	Block 6		
05FFFFH 050000H	Block 5		
04FFFFH 040000H	Block 4		
03FFFFH 030000H	Block 3		
02FFFFH 020000H	Block 2		
01FFFFH 010000H	Block 1		
00FFFFH 000000H	Block 0		

1256 F01b.0

Note: The address input range in x8 mode (BYTE#=V_{IL}) is A₁₉-A₁

FIGURE 2: SST34HF16x2S, 2M x8 CONCURRENT SUPERFLASH DUAL-BANK MEMORY ORGANIZATION



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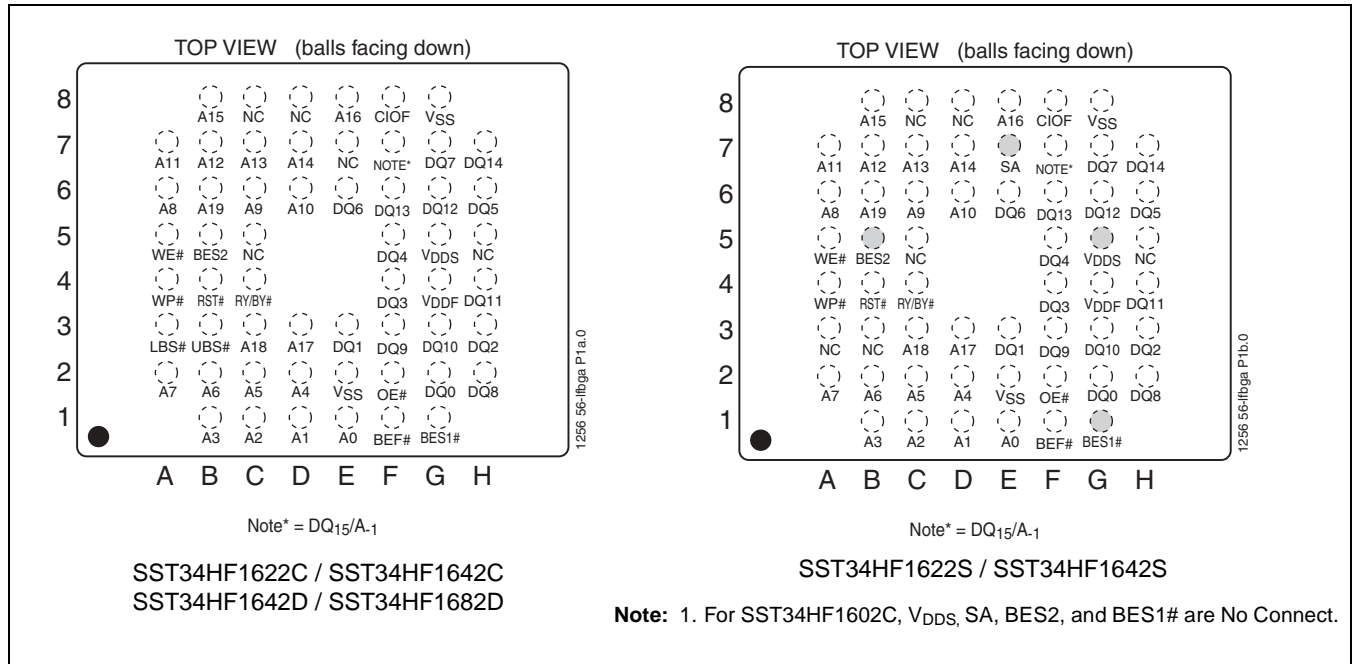


FIGURE 3: PIN ASSIGNMENTS FOR 56-BALL LFBGA (8MM X 10MM)

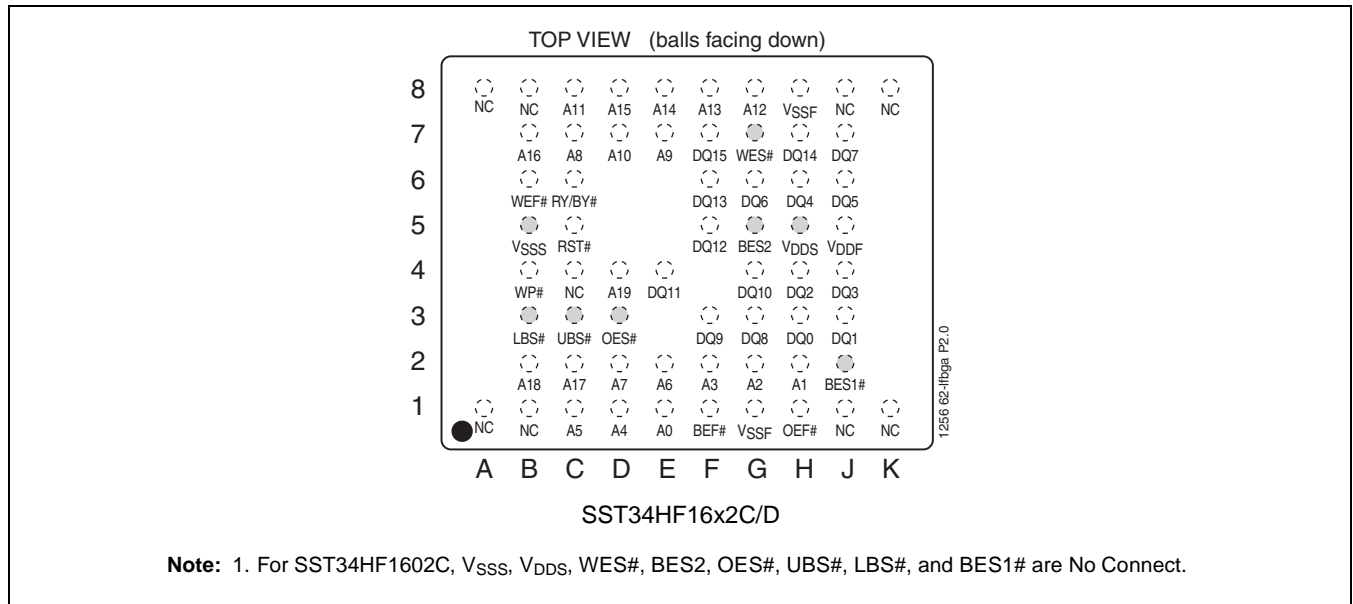


FIGURE 4: PIN ASSIGNMENTS FOR 62-BALL LFBGA (8MM X 10MM)

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TABLE 3: PIN DESCRIPTION

Symbol	Pin Name	Functions
A _{MS} ¹ to A ₀	Address Inputs	To provide flash address, A ₁₉ -A ₀ . To provide (P)SRAM address, A _{MS} -A ₀
SA	SRAM x8 Address	To provide additional address for x8 SRAM
DQ ₁₄ -DQ ₀	Data Inputs/Outputs	To output data during Read cycles and receive input data during Write cycles. Data is internally latched during a flash Erase/Program cycle. The outputs are in tri-state when OE# is high or BES1# is high or BES2 is low and BEF# is high.
DQ ₁₅ /A ₋₁	Data Input/Output and LBS Address	DQ ₁₅ is used as data I/O pin when in x16 mode (CIOF = "1") A ₋₁ is used as the LBS address pin when in x8 mode (CIOF = "0")
BEF#	Flash Memory Bank Enable	To activate the Flash memory bank when BEF# is low
BES1#	(P)SRAM Memory Bank Enable	To activate the (P)SRAM memory bank when BES1# is low
BES2	(P)SRAM Memory Bank Enable	To activate the (P)SRAM memory bank when BES2 is high
OEF# ²	Output Enable	To gate the data output buffers for Flash ² only
OES# ²	Output Enable	To gate the data output buffers for SRAM ² only
WEF# ²	Write Enable	To control the Write operations for Flash ² only
WES# ²	Write Enable	To control the Write operations for SRAM ² only
OE#	Output Enable	To gate the data output buffers
WE#	Write Enable	To control the Write operations
CIOF	Byte Selection for Flash	When low, select Byte mode. When high, select Word mode.
UBS#	Upper Byte Control ((P)SRAM)	To enable DQ ₁₅ -DQ ₈
LBS#	Lower Byte Control ((P)SRAM)	To enable DQ ₇ -DQ ₀
WP#	Write Protect	To protect and unprotect the top 8 KWord (4 sectors) from Erase or Program operation
RST#	Reset	To Reset and return the device to Read mode
RY/BY#	Ready/Busy#	To output the status of a Program or Erase Operation RY/BY# is a open drain output, so a 10KΩ- 100KΩ pull-up resistor is required to allow RY/BY# to transition high indicating the device is ready to read.
V _{SSF} ²	Ground	Flash ² only
V _{SSS} ²	Ground	SRAM ² only
V _{SS}	Ground	
V _{DDF}	Power Supply (Flash)	2.7-3.3V Power Supply to Flash only
V _{DDS}	Power Supply ((P)SRAM)	2.7-3.3V Power Supply to (P)SRAM only
NC	No Connection	Unconnected pins

T3.0 1256

1. A_{MS} = Most Significant Address
A_{MS} = A₁₆ for SST34HF1622C/S, A₁₇ for SST34HF1642C/D/S, and A₁₈ for SST34HF1682D
2. LS package only



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TABLE 4: OPERATIONAL MODES SELECTION FOR x16 (P)SRAM

Mode	BEF# ¹	BES1# ^{1,2}	BES2 ^{1,2}	OE# ^{2,3}	WE# ^{2,3}	LBS# ²	UBS# ²	DQ ₁₅₋₈		
								DQ ₇₋₀	CIOF = V _{IH}	CIOF = V _{IL}
Full Standby	V _{IH}	V _{IH}	X	X	X	X	X	HIGH-Z	HIGH-Z	HIGH-Z
		X	V _{IL}	X	X	X	X			
Output Disable	V _{IH}	V _{IL}	V _{IH}	V _{IH}	V _{IH}	X	X	HIGH-Z	HIGH-Z	HIGH-Z
		V _{IL}	V _{IH}	X	X	V _{IH}	V _{IH}			
	V _{IL}	V _{IH}	X	V _{IH}	V _{IH}	X	X	HIGH-Z	HIGH-Z	HIGH-Z
Flash Read	V _{IL}	V _{IH}	X	V _{IL}	V _{IH}	X	X	D _{OUT}	D _{OUT}	DQ ₁₄₋₈ = HIGH-Z DQ ₁₅ = A ₋₁
		X	V _{IL}							
Flash Write	V _{IL}	V _{IH}	X	V _{IH}	V _{IL}	X	X	D _{IN}	D _{IN}	DQ ₁₄₋₈ = HIGH-Z DQ ₁₅ = A ₋₁
		X	V _{IL}							
Flash Erase	V _{IL}	V _{IH}	X	V _{IH}	V _{IL}	X	X	X	X	X
		X	V _{IL}							
(P)SRAM Read	V _{IH}	V _{IL}	V _{IH}	V _{IL}	V _{IH}	V _{IL}	V _{IL}	D _{OUT}	D _{OUT}	D _{OUT}
						V _{IH}	V _{IL}	HIGH-Z	D _{OUT}	D _{OUT}
						V _{IL}	V _{IH}	D _{OUT}	HIGH-Z	HIGH-Z
(P)SRAM Write	V _{IH}	V _{IL}	V _{IH}	X	V _{IL}	V _{IL}	V _{IL}	D _{IN}	D _{IN}	D _{IN}
						V _{IH}	V _{IL}	HIGH-Z	D _{IN}	D _{IN}
						V _{IL}	V _{IH}	D _{IN}	HIGH-Z	HIGH-Z
Product Identification ⁴	V _{IL}	V _{IH}	V _{IL}	V _{IL}	V _{IH}	X	X	Manufacturer's ID ⁵ Device ID ⁵		

T4.0 1256

1. Do not apply BEF# = V_{IL}, BES1# = V_{IL} and BES2 = V_{IH} at the same time
2. X can be V_{IL} or V_{IH}, but no other value.
3. OE# = OEF# and OES#
WE# = WEF# and WES# for LS package only
4. Software mode only
5. With A₁₉-A₁₈ = V_{IL}, SST Manufacturer's ID = BFH, is read with A₀=0,
SST34HF16x2C/D/S Device ID = 734AH, is read with A₀=1

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TABLE 5: OPERATIONAL MODES SELECTION FOR x8 SRAM

Mode	BEF# ¹	BES1# ^{1,2}	BES2 ^{1,2}	OE# ²	WE# ²	SA ²	DQ ₁₅₋₈		
							DQ ₇₋₀	CIOF = V _{IH}	CIOF = V _{IL}
Full Standby	V _{IH}	V _{IH}	X	X	X	X	HIGH-Z	HIGH-Z	HIGH-Z
		X	V _{IL}	X	X	X			
Output Disable	V _{IH}	V _{IL}	V _{IH}	V _{IH}	V _{IH}	X	HIGH-Z	HIGH-Z	HIGH-Z
		V _{IL}	V _{IH}	X	X	V _{IH}			
	V _{IL}	V _{IH}	X	V _{IH}	V _{IH}	X	HIGH-Z	HIGH-Z	HIGH-Z
Flash Read	V _{IL}	V _{IH}	X	V _{IL}	V _{IH}	X	D _{OUT}	D _{OUT}	DQ ₁₄₋₈ = HIGH-Z DQ ₁₅ = A ₋₁
		X	V _{IL}						
Flash Write	V _{IL}	V _{IH}	X	V _{IH}	V _{IL}	X	D _{IN}	D _{IN}	DQ ₁₄₋₈ = HIGH-Z DQ ₁₅ = A ₋₁
		X	V _{IL}						
Flash Erase	V _{IL}	V _{IH}	X	V _{IH}	V _{IL}	X	X	X	X
		X	V _{IL}						
SRAM Read	V _{IH}	V _{IL}	V _{IH}	V _{IL}	V _{IH}	SA	D _{OUT}	HIGH-Z	HIGH-Z
SRAM Write	V _{IH}	V _{IL}	V _{IH}	X	V _{IL}	SA	D _{IN}	HIGH-Z	HIGH-Z
Product Identification ³	V _{IL}	V _{IH}	V _{IL}	V _{IL}	V _{IH}	X	Manufacturer's ID ⁴ Device ID ⁴	Manufacturer's ID ⁴ Device ID ⁴	

T5.0 1256

1. Do not apply BEF# = V_{IL}, BES1# = V_{IL} and BES2 = V_{IH} at the same time
2. X can be V_{IL} or V_{IH}, but no other value.
3. Software mode only
4. With A₁₉-A₁₈ = V_{IL}; SST Manufacturer's ID = BFH, is read with A₀=0,
SST34HF16x2C/D/S Device ID = 734AH, is read with A₀=1, for x8 A₋₁ will not be part of the Device ID

TABLE 6: OPERATIONAL MODES SELECTION FOR 0 MBIT SRAM: SST34HF1602C

Mode	BEF#	OE# ^{1,2}	WE# ^{1,2}	DQ ₁₅₋₈		
				DQ ₇₋₀	CIOF = V _{IH}	CIOF = V _{IL}
Full Standby	V _{IH}	X	X	HIGH-Z	HIGH-Z	HIGH-Z
		X	X			
Output Disable	V _{IH}	V _{IH}	V _{IH}	HIGH-Z	HIGH-Z	HIGH-Z
		X	X			
	V _{IL}	V _{IH}	V _{IH}	HIGH-Z	HIGH-Z	HIGH-Z
Flash Read	V _{IL}	V _{IL}	V _{IH}	D _{OUT}	D _{OUT}	DQ ₁₄₋₈ = HIGH-Z DQ ₁₅ = A ₋₁
Flash Write	V _{IL}	V _{IH}	V _{IL}	D _{IN}	D _{IN}	DQ ₁₄₋₈ = HIGH-Z DQ ₁₅ = A ₋₁
Flash Erase	V _{IL}	V _{IH}	V _{IL}	X	X	X
Product Identification ³	V _{IL}	V _{IL}	V _{IH}	Manufacturer's ID ⁴ Device ID ⁴	Manufacturer's ID ⁴ Device ID ⁴	

T6.0 1256

1. X can be V_{IL} or V_{IH}, but no other value.
2. OE# = OEF#, WE# = WEF#
3. Software mode only
4. With A₁₉-A₁₈ = V_{IL}; SST Manufacturer's ID = BFH, is read with A₀=0,
SST34HF1602C Device ID = 734AH, is read with A₀=1, for x8 A₋₁ will not be part of the Device ID



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TABLE 7: SOFTWARE COMMAND SEQUENCE

Command Sequence	1st Bus Write Cycle		2nd Bus Write Cycle		3rd Bus Write Cycle		4th Bus Write Cycle		5th Bus Write Cycle		6th Bus Write Cycle	
	Addr ¹	Data ²	Addr ¹	Data ²	Addr ¹	Data ²	Addr ¹	Data ²	Addr ¹	Data ²	Addr ¹	Data ²
Word-/Byte-Program	5555H	AAH	2AAAH	55H	5555H	A0H	WA ³	Data				
Sector-Erase	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	SA _X ⁴	30H
Block-Erase	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	BA _X ⁴	50H
Chip-Erase	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	10H
Erase-Suspend	XXXXH	B0H										
Erase-Resume	XXXXH	30H										
Query Sec ID ⁵	5555H	AAH	2AAAH	55H	5555H	88H						
User Security ID Word-/Byte-Program	5555H	AAH	2AAAH	55H	5555H	A5H	SIWA ⁶	Data				
User Security ID Program Lock-out ⁷	5555H	AAH	2AAAH	55H	5555H	85H	XXH	0000H				
Software ID Entry ⁸	5555H	AAH	2AAAH	55H	BK _X ⁹ 5555H	90H						
Software ID Exit/ Sec ID Exit ^{10,11}	5555H	AAH	2AAAH	55H	5555H	F0H						
Software ID Exit/ Sec ID Exit ^{10,11}	XXH	F0H										

T7.0 1256

1. Address format A₁₄-A₀ (Hex), Addresses A₁₉-A₁₅ can be V_{IL} or V_{IH}, but no other value, for the command sequence when in x16 mode.
When in x8 mode, Addresses A₁₉-A₁₅, Address A₋₁ and DQ₁₄-DQ₈ can be V_{IL} or V_{IH}, but no other value, for the command sequence.
2. DQ₁₅-DQ₈ can be V_{IL} or V_{IH}, but no other value, for the command sequence
3. WA = Program word/byte address
4. SA_X for Sector-Erase; uses A₁₉-A₁₀ address lines
BA_X for Block-Erase; uses A₁₉-A₁₅ address lines
5. For SST34HF16x2C/D/S,
SST ID is read with A₃ = 0 (Address range = 00000H to 00007H),
User ID is read with A₃ = 1 (Address range = 00010H to 00017H).
Lock Status is read with A₇-A₀ = 000FFH. Unlocked: DQ₃ = 1 / Locked: DQ₃ = 0.
6. SIWA = User Security ID Program word/byte address
For SST34HF16x2C/D/S, valid Word-Addresses for User Sec ID are from C0010H-C0017H.
All 4 cycles of User Security ID Word-Program and Program Lock-out must be completed before going back to Read-Array mode.
7. The User Security ID Program Lock-out command must be executed in x16 mode (BYTE#=V_{IH}).
8. The device does not remain in Software Product Identification mode if powered down.
9. A₁₉ and A₁₈ = V_{IL}
10. Both Software ID Exit operations are equivalent
11. If users never lock after programming, User Sec ID can be programmed over the previously unprogrammed bits (data=1) using the User Sec ID mode again (the programmed "0" bits cannot be reversed to "1").
For SST34HF16x2C/D/S, valid Word-Addresses for User Sec ID are from C0010H-C0017H.

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Absolute Maximum Stress Ratings (Applied conditions greater than those listed under “Absolute Maximum Stress Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Operating Temperature -20°C to +85°C
 Storage Temperature -65°C to +125°C
 D. C. Voltage on Any Pin to Ground Potential -0.5V to $V_{DD}^1+0.3V$
 Transient Voltage (<20 ns) on Any Pin to Ground Potential -1.0V to $V_{DD}^1+1.0V$
 Package Power Dissipation Capability ($T_a = 25^\circ C$) 1.0W
 Output Short Circuit Current² 50 mA

1. $V_{DD} = V_{DDF}$ and V_{DDS}
2. Outputs shorted for no more than one second. No more than one output shorted at a time.

OPERATING RANGE

Range	Ambient Temp	V_{DD}
Commercial	0°C to +70°C	2.7-3.3V
Extended	-20°C to +85°C	2.7-3.3V

AC CONDITIONS OF TEST

Input Rise/Fall Time 5 ns
Output Load $C_L = 30$ pF
See Figures 20 and 21



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TABLE 8: DC OPERATING CHARACTERISTICS ($V_{DD} = V_{DDF}$ AND $V_{DDs} = 2.7-3.3V$)

Symbol	Parameter	Limits			Test Conditions
		Min	Max	Units	
I_{DD}^1	Active V_{DD} Current				Address input = V_{ILT}/V_{IHT} , at $f=1/T_{RC}$ Min, $V_{DD}=V_{DD}$ Max, all DQs open
	Read				$OE\#=V_{IL}$, $WE\#=V_{IH}$
	Flash		35	mA	$BEF\#=V_{IL}$, $BES1\#=V_{IH}$, or $BES2=V_{IL}$
	(P)SRAM		30	mA	$BEF\#=V_{IH}$, $BES1\#=V_{IL}$, $BES2=V_{IH}$
	Concurrent Operation		60	mA	$BEF\#=V_{IH}$, $BES1\#=V_{IL}$, $BES2=V_{IH}$
	Write ²				$WE\#=V_{IL}$
	Flash		40	mA	$BEF\#=V_{IL}$, $BES1\#=V_{IH}$, or $BES2=V_{IL}$, $OE\#=V_{IH}$
	(P)SRAM		30	mA	$BEF\#=V_{IH}$, $BES1\#=V_{IL}$, $BES2=V_{IH}$
I_{SB}	Standby V_{DD} Current	SRAM	30	μA	$V_{DD} = V_{DD}$ Max, $BEF\#=BES1\#=V_{IHC}$, $BES2=V_{ILC}$
		PSRAM	85	μA	
I_{RT}	Reset V_{DD} Current		30	μA	$RST\#=GND$
I_{LI}	Input Leakage Current		1	μA	$V_{IN}=GND$ to V_{DD} , $V_{DD}=V_{DD}$ Max
I_{LIW}	Input Leakage Current on $WP\#$ pin and $RST\#$ pin		10	μA	$WP\#=GND$ to V_{DD} , $V_{DD}=V_{DD}$ Max $RST\#=GND$ to V_{DD} , $V_{DD}=V_{DD}$ Max
I_{LO}	Output Leakage Current		10	μA	$V_{OUT}=GND$ to V_{DD} , $V_{DD}=V_{DD}$ Max
V_{IL}	Input Low Voltage		0.8	V	$V_{DD}=V_{DD}$ Min
V_{ILC}	Input Low Voltage (CMOS)		0.3	V	$V_{DD}=V_{DD}$ Max
V_{IH}	Input High Voltage	$0.7 V_{DD}$		V	$V_{DD}=V_{DD}$ Max
V_{IHC}	Input High Voltage (CMOS)	$V_{DD}-0.3$		V	$V_{DD}=V_{DD}$ Max
V_{OLF}	Flash Output Low Voltage		0.2	V	$I_{OL}=100 \mu A$, $V_{DD}=V_{DD}$ Min
V_{OHF}	Flash Output High Voltage	$V_{DD}-0.2$		V	$I_{OH}=-100 \mu A$, $V_{DD}=V_{DD}$ Min
V_{OLS}	(P)SRAM Output Low Voltage		0.4	V	$I_{OL}=1 \text{ mA}$, $V_{DD}=V_{DD}$ Min
V_{OHS}	(P)SRAM Output High Voltage	2.2		V	$I_{OH}=-500 \mu A$, $V_{DD}=V_{DD}$ Min

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1. Address input = V_{ILT}/V_{IHT} , $V_{DD}=V_{DD}$ Max (See Figure 20)
2. I_{DD} active while Erase or Program is in progress.

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TABLE 9: RECOMMENDED SYSTEM POWER-UP TIMINGS

Symbol	Parameter	Minimum	Units
$T_{PU-READ}^1$	Power-up to Read Operation	100	μ s
$T_{PU-WRITE}^1$	Power-up to Write Operation	100	μ s

T9.0 1256

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 10: CAPACITANCE (Ta = 25°C, f=1 Mhz, other pins open)

Parameter	Description	Test Condition	Maximum
$C_{I/O}^1$	I/O Pin Capacitance	$V_{I/O} = 0V$	20 pF
C_{IN}^1	Input Capacitance	$V_{IN} = 0V$	16 pF

T10.0 1256

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 11: FLASH RELIABILITY CHARACTERISTICS

Symbol	Parameter	Minimum Specification	Units	Test Method
N_{END}^1	Endurance	10,000	Cycles	JEDEC Standard A117
T_{DR}^1	Data Retention	100	Years	JEDEC Standard A103
I_{LTH}^1	Latch Up	$100 + I_{DD}$	mA	JEDEC Standard 78

T11.0 1256

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.



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AC CHARACTERISTICS

TABLE 12: (P)SRAM READ CYCLE TIMING PARAMETERS

		Min	Max	Units
T _{RCS}	Read Cycle Time	70		ns
T _{AAS}	Address Access Time		70	ns
T _{BES}	Bank Enable Access Time		70	ns
T _{OES}	Output Enable Access Time		35	ns
T _{BYES}	UBS#, LBS# Access Time		70	ns
T _{BLZS} ¹	BES# to Active Output	0		ns
T _{OLZS} ¹	Output Enable to Active Output	0		ns
T _{BYLZS} ¹	UBS#, LBS# to Active Output	0		ns
T _{BHZS} ¹	BES# to High-Z Output		25	ns
T _{OHSZS} ¹	Output Disable to High-Z Output		25	ns
T _{BYHSZS} ¹	UBS#, LBS# to High-Z Output		35	ns
T _{OHS}	Output Hold from Address Change	10		ns

T12.0 1256

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 13: (P)SRAM WRITE CYCLE TIMING PARAMETERS

Symbol	Parameter	Min	Max	Units
T _{WCS}	Write Cycle Time	70		ns
T _{BWS}	Bank Enable to End-of-Write	60		ns
T _{AWS}	Address Valid to End-of-Write	60		ns
T _{ASTS}	Address Set-up Time	0		ns
T _{WPS}	Write Pulse Width	60		ns
T _{WRS}	Write Recovery Time	0		ns
T _{BYWS}	UBS#, LBS# to End-of-Write	60		ns
T _{ODWS}	Output Disable from WE# Low		30	ns
T _{OEWS}	Output Enable from WE# High	0		ns
T _{DSS}	Data Set-up Time	30		ns
T _{DHS}	Data Hold from Write Time	0		ns

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TABLE 14: FLASH READ CYCLE TIMING PARAMETERS $V_{DD} = 2.7-3.3V$

Symbol	Parameter	Min	Max	Units
T_{RC}	Read Cycle Time	70		ns
T_{CE}	Chip Enable Access Time		70	ns
T_{AA}	Address Access Time		70	ns
T_{OE}	Output Enable Access Time		35	ns
T_{CLZ}^1	BEF# Low to Active Output	0		ns
T_{OLZ}^1	OE# Low to Active Output	0		ns
T_{CHZ}^1	BEF# High to High-Z Output		20	ns
T_{OHZ}^1	OE# High to High-Z Output		20	ns
T_{OH}^1	Output Hold from Address Change	0		ns
T_{RP}^1	RST# Pulse Width	500		ns
T_{RHR}^1	RST# High Before Read	50		ns
$T_{RY}^{1,2}$	RST# Pin Low to Read		20	μs

T14.0 1256

1. This parameter is measured only for initial qualification and after the design or process change that could affect this parameter.
2. This parameter applies to Sector-Erase, Block-Erase and Program operations. This parameter does not apply to Chip-Erase.

TABLE 15: FLASH PROGRAM/ERASE CYCLE TIMING PARAMETERS

Symbol	Parameter	Min	Max	Units
T_{BP}	Word-Program Time		10	μs
T_{AS}	Address Setup Time	0		ns
T_{AH}	Address Hold Time	40		ns
T_{CS}	WE# and BEF# Setup Time	0		ns
T_{CH}	WE# and BEF# Hold Time	0		ns
T_{OES}	OE# High Setup Time	0		ns
T_{OEH}	OE# High Hold Time	10		ns
T_{CP}	BEF# Pulse Width	40		ns
T_{WP}	WE# Pulse Width	40		ns
T_{WPH}^1	WE# Pulse Width High	30		ns
T_{CPH}^1	BEF# Pulse Width High	30		ns
T_{DS}	Data Setup Time	30		ns
T_{DH}^1	Data Hold Time	0		ns
T_{IDA}^1	Software ID Access and Exit Time		150	ns
T_{ES}	Erase-Suspend Latency		20	μs
$T_{BY}^{1,2}$	RY/BY# Delay Time	90		ns
T_{BR}^1	Bus# Recovery Time		1	μs
T_{SE}	Sector-Erase		25	ms
T_{BE}	Block-Erase		25	ms
T_{SCE}	Chip-Erase		50	ms

T15.0 1256

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.
2. This parameter applies to Sector-Erase, Block-Erase, and Program operations.
This parameter does not apply to Chip-Erase operations.

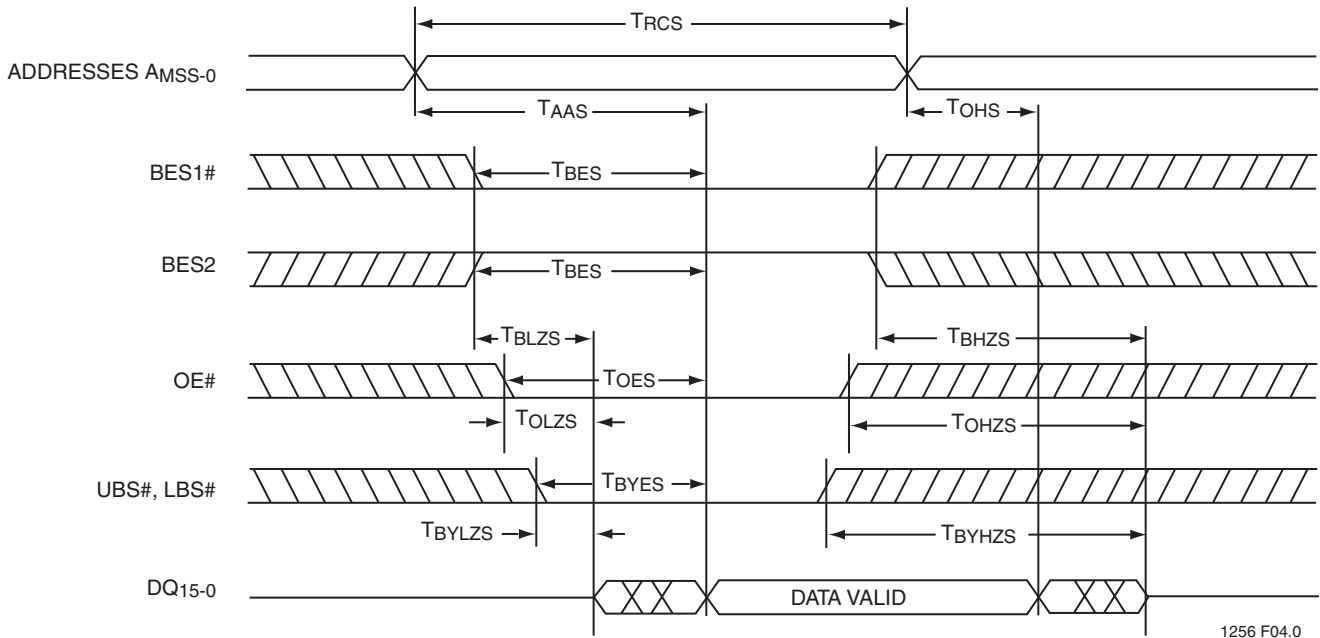


16 Mbit Concurrent SuperFlash + 2/4/8 Mbit SRAM ComboMemory

SST34HF1602C / SST34HF1622C / SST34HF1642C

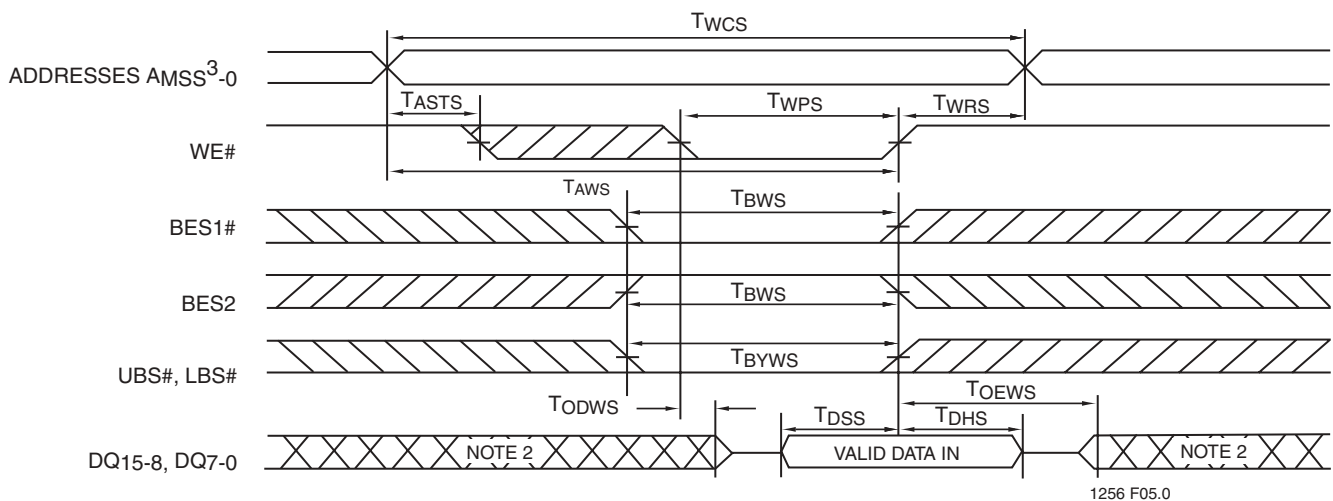
SST34HF1642D / SST34HF1682D / SST34HF1622S / SST34HF1642S

Advance Information



Note: A_{MSS} = Most Significant Address
 $A_{MSS} = A_{16}$ for SST34HF1622C/S, A_{17} for SST34HF1622C/D/S, and A_{18} for SST34HF1682D
 For SST34HF16x2S, LBS# and UBS# are No Connect and in x8 mode, the additional SRAM address is SA.

FIGURE 5: (P)SRAM READ CYCLE TIMING DIAGRAM



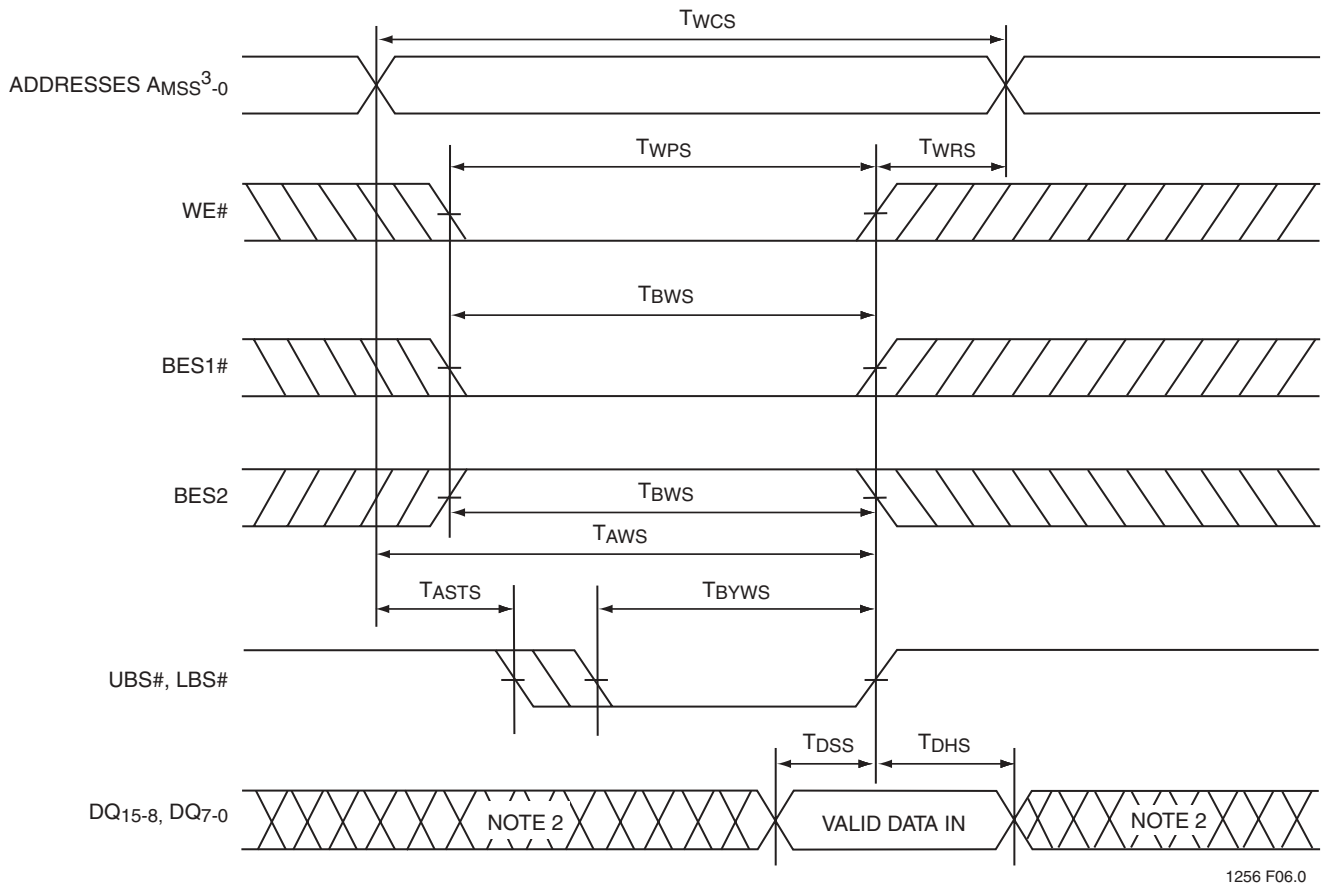
Note: 1. If OE# is High during the Write cycle, the outputs will remain at high impedance.
 2. If BES1# goes Low or BES2 goes high coincident with or after WE# goes Low, the output will remain at high impedance. If BES1# goes High or BES2 goes low coincident with or before WE# goes High, the output will remain at high impedance. Because D_{IN} signals may be in the output state at this time, input signals of reverse polarity must not be applied.
 3. A_{MSS} = Most Significant SRAM Address
 $A_{MSS} = A_{16}$ for SST34HF1622C/S, A_{17} for SST34HF1622C/D/S, and A_{18} for SST34HF1682D
 For SST34HF16x2S, LBS# and UBS# are No Connect and in x8 mode, the additional SRAM address is SA.

FIGURE 6: (P)SRAM WRITE CYCLE TIMING DIAGRAM (WE# CONTROLLED)¹

16 Mbit Concurrent SuperFlash + 2/4/8 Mbit SRAM ComboMemory
 SST34HF1602C / SST34HF1622C / SST34HF1642C
 SST34HF1642D / SST34HF1682D / SST34HF1622S / SST34HF1642S



Advance Information



- Note:**
1. If OE# is High during the Write cycle, the outputs will remain at high impedance.
 2. Because D_{IN} signals may be in the output state at this time, input signals of reverse polarity must not be applied.
 3. A_{MSS} = Most Significant SRAM Address
 $A_{MSS} = A_{16}$ for SST34HF1622C, A_{17} for SST34HF1622C/D, and A_{18} for SST34HF1682D

FIGURE 7: (P)SRAM WRITE CYCLE TIMING DIAGRAM (UBS#, LBS# CONTROLLED)¹ x16 (P)SRAM ONLY



16 Mbit Concurrent SuperFlash + 2/4/8 Mbit SRAM ComboMemory
SST34HF1602C / SST34HF1622C / SST34HF1642C
SST34HF1642D / SST34HF1682D / SST34HF1622S / SST34HF1642S

Advance Information

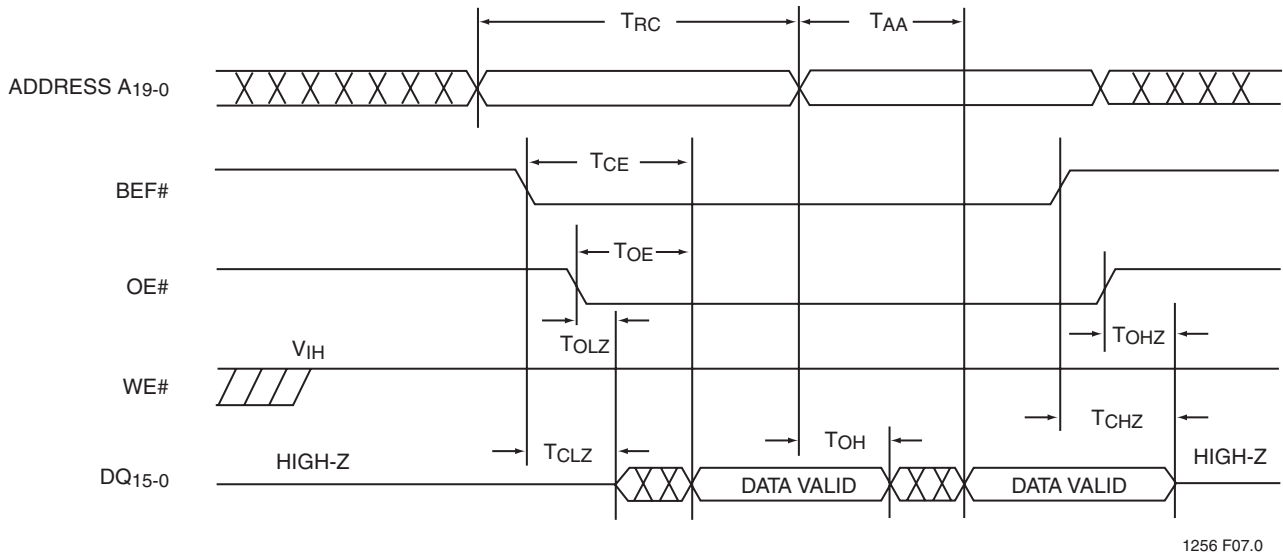
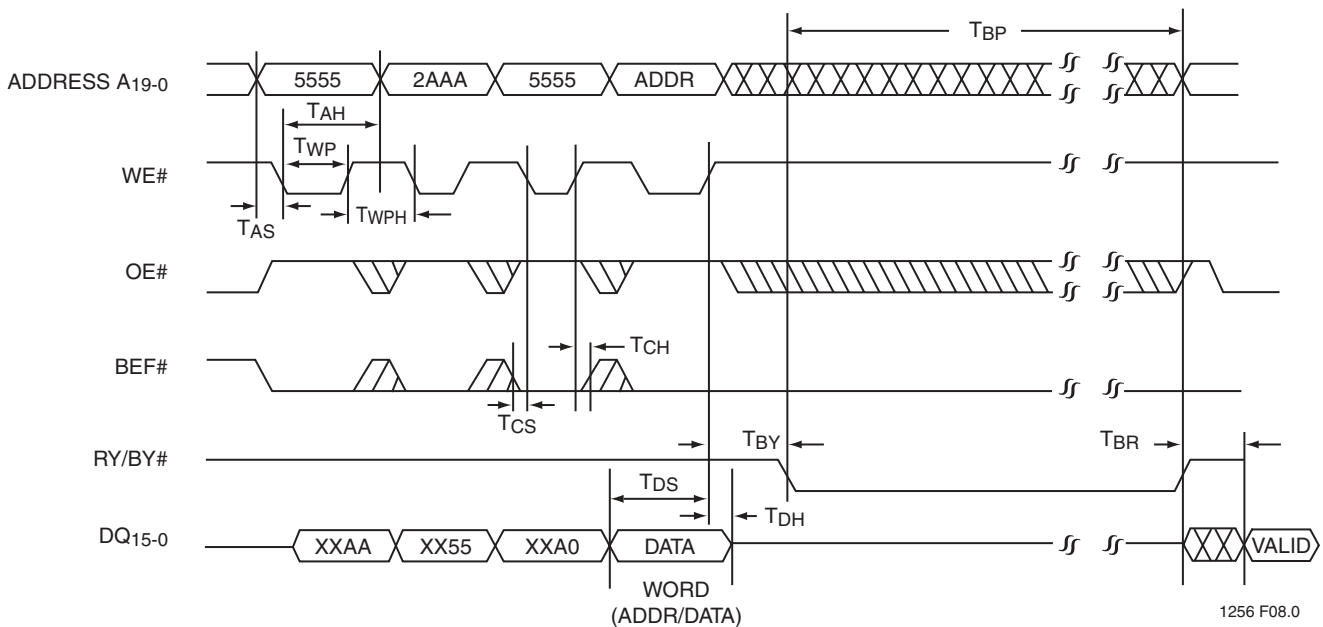
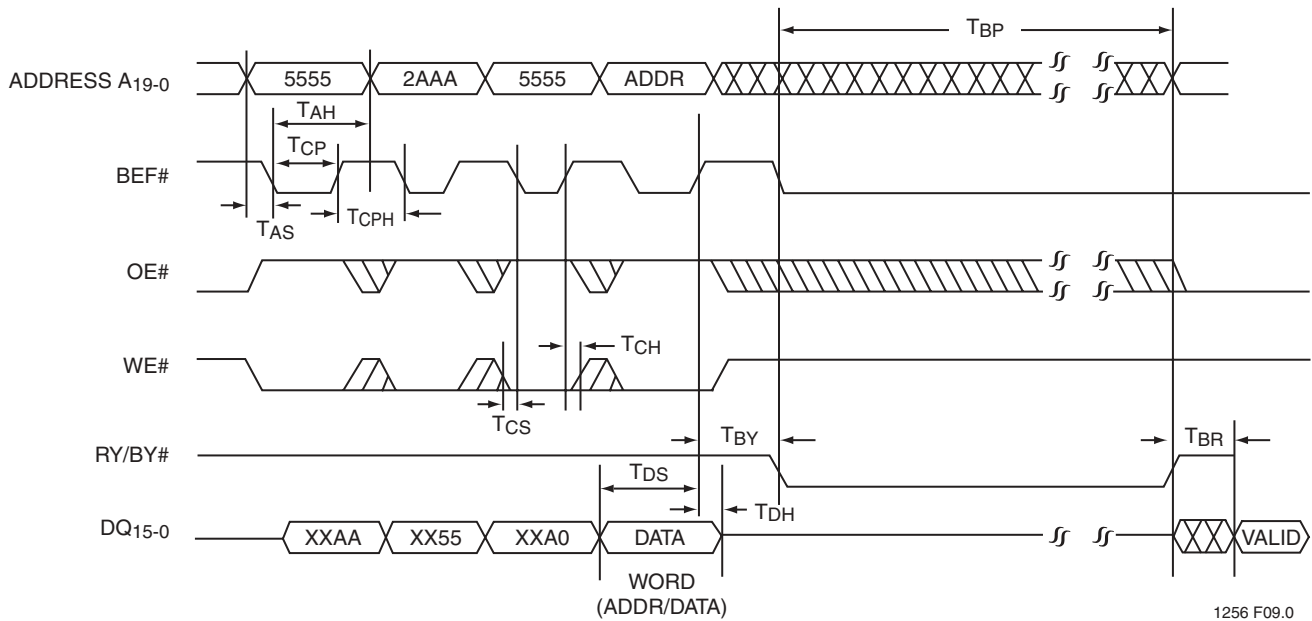


FIGURE 8: FLASH READ CYCLE TIMING DIAGRAM FOR WORD MODE
(FOR BYTE MODE A₁ = ADDRESS INPUT)



Note: X can be V_{IL} or V_{IH}, but no other value.

FIGURE 9: FLASH WE# CONTROLLED WORD-PROGRAM CYCLE TIMING DIAGRAM FOR WORD MODE
(FOR BYTE MODE A₁ = ADDRESS INPUT)



Note: X can be V_{IL} or V_{IH}, but no other value.

FIGURE 10: FLASH BEF# CONTROLLED WORD-PROGRAM CYCLE TIMING DIAGRAM FOR WORD MODE (FOR BYTE MODE A₁ = ADDRESS INPUT)

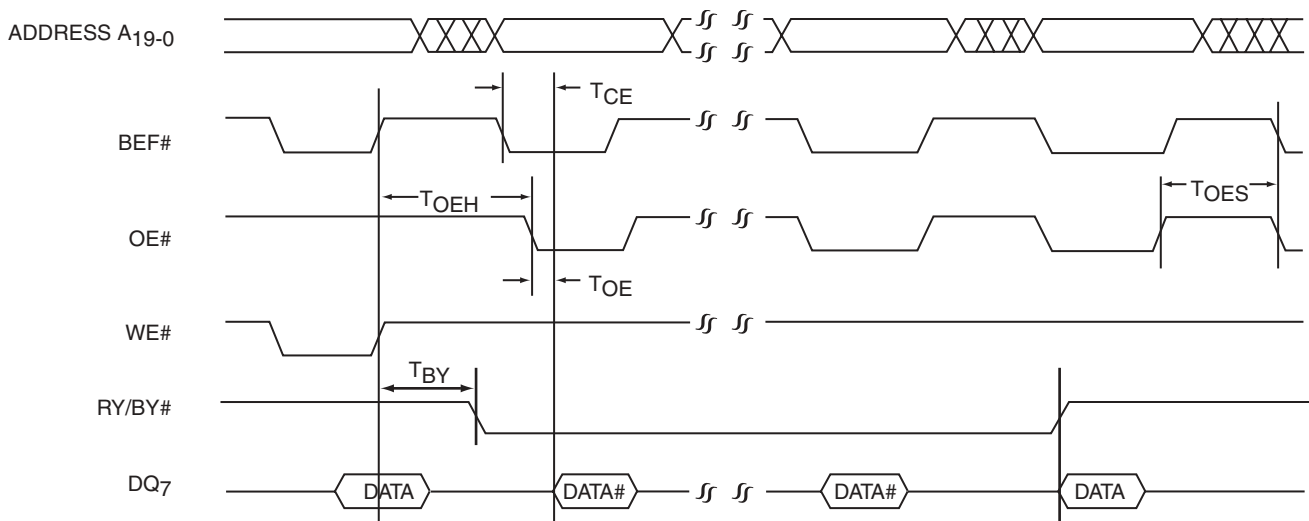


FIGURE 11: FLASH DATA# POLLING TIMING DIAGRAM FOR WORD MODE (FOR BYTE MODE A₁ = ADDRESS INPUT)



16 Mbit Concurrent SuperFlash + 2/4/8 Mbit SRAM ComboMemory
SST34HF1602C / SST34HF1622C / SST34HF1642C
SST34HF1642D / SST34HF1682D / SST34HF1622S / SST34HF1642S

Advance Information

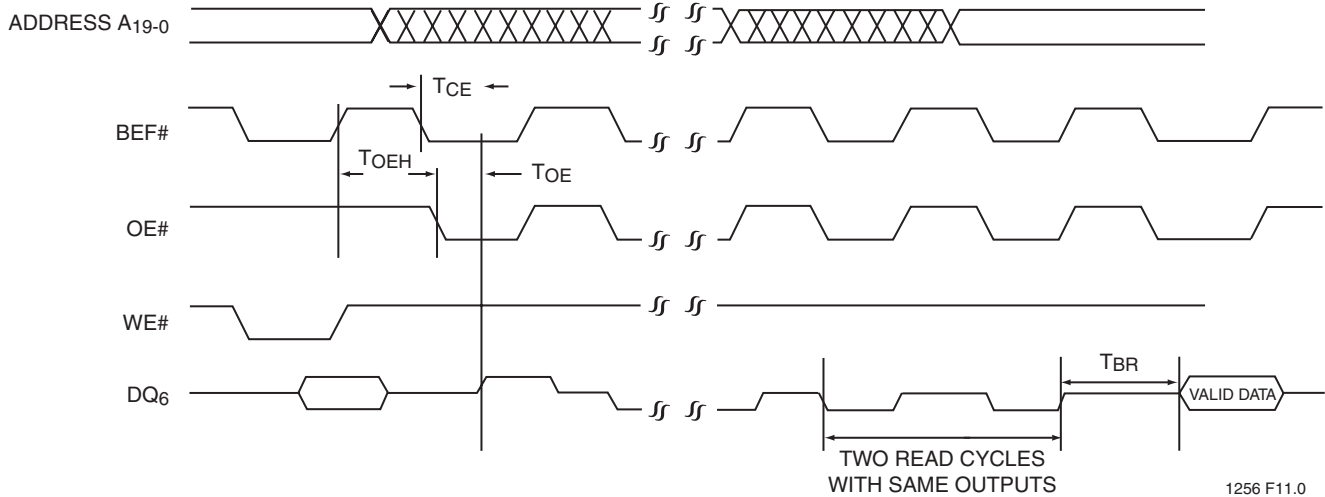
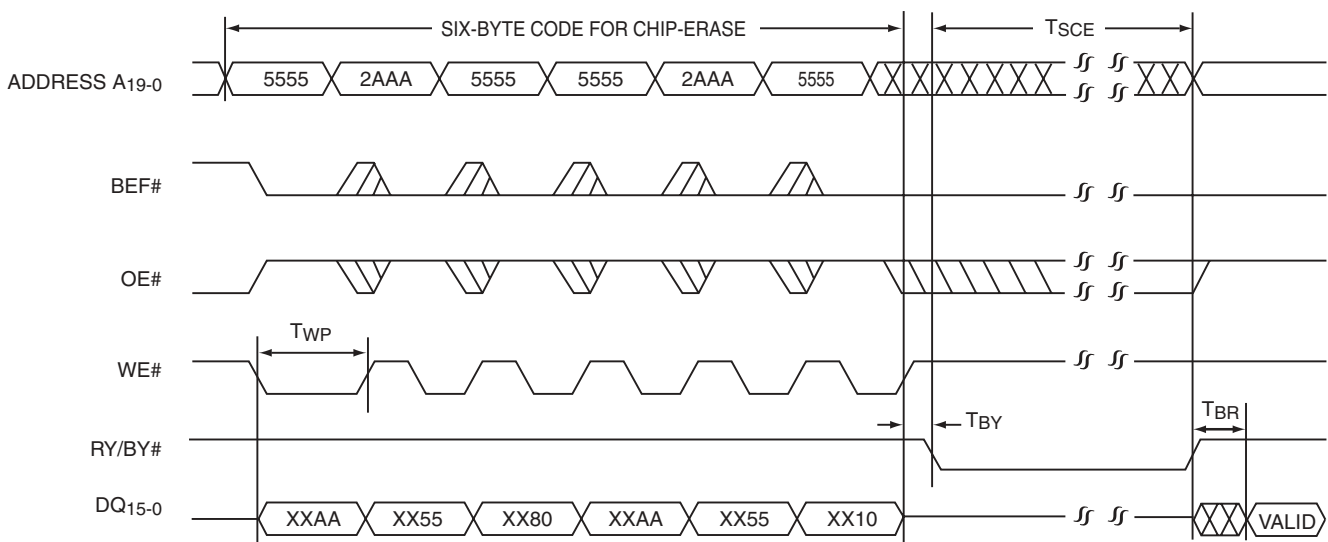
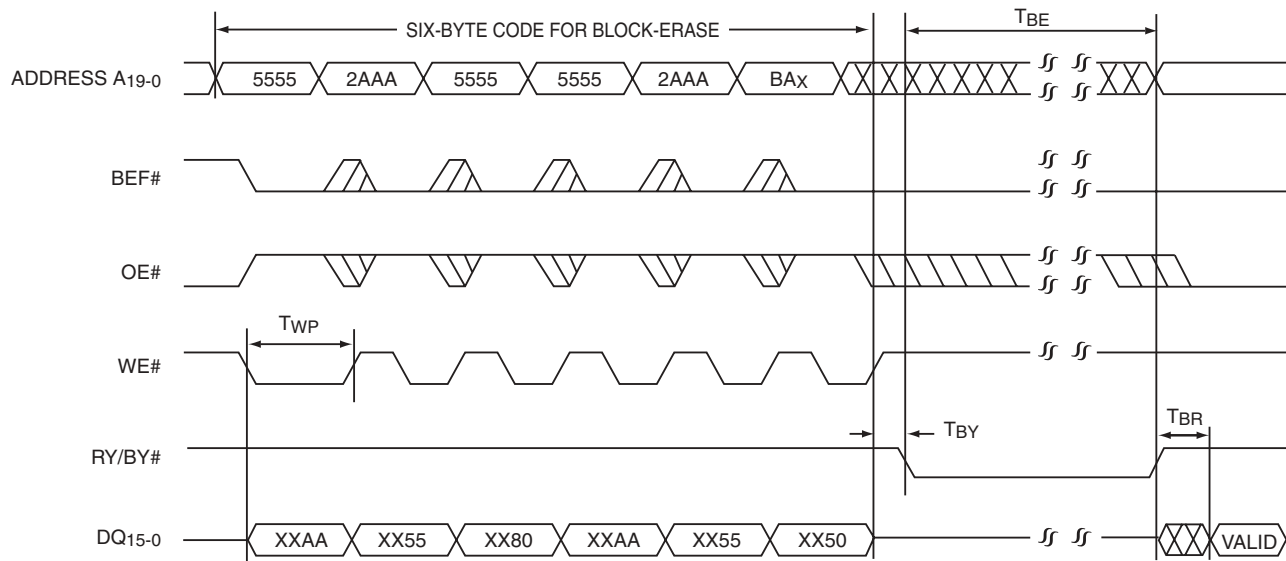


FIGURE 12: FLASH TOGGLE BIT TIMING DIAGRAM FOR WORD MODE
(FOR BYTE MODE A₁ = DON'T CARE)



Note: This device also supports BEF# controlled Chip-Erase operation.
 The WE# and BEF# signals are interchangeable as long as minimum timings are met. (See Table 15.)
 X can be V_{IL} or V_{IH}, but no other value.

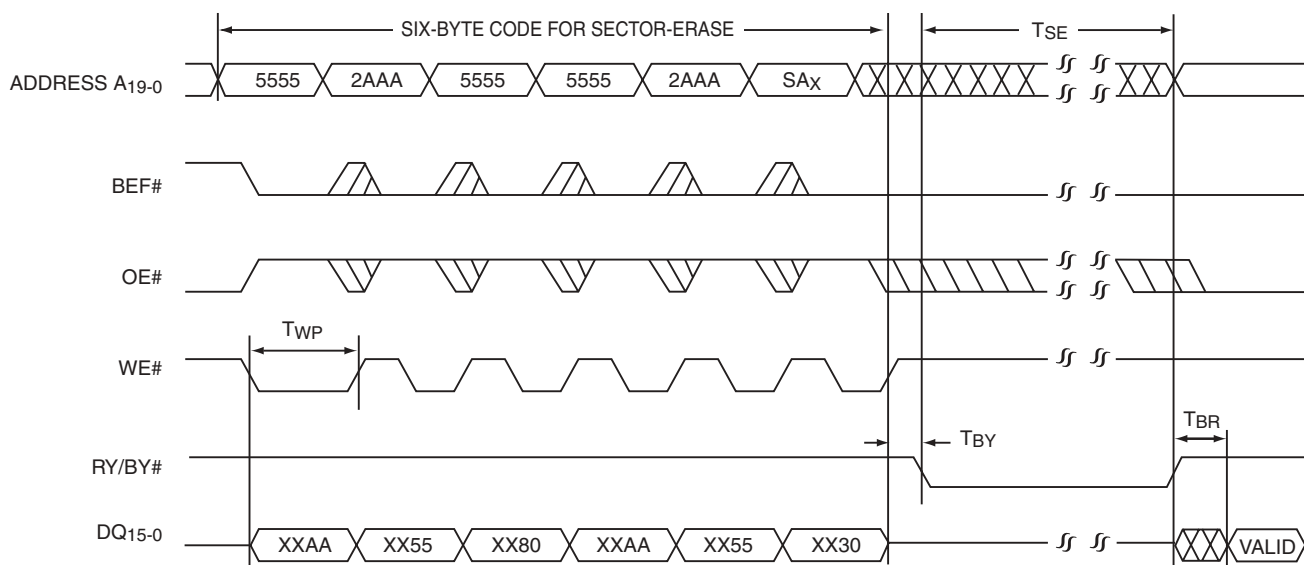
FIGURE 13: FLASH WE# CONTROLLED CHIP-ERASE TIMING DIAGRAM FOR WORD MODE
(FOR BYTE MODE A₁ = DON'T CARE)



1256 F13.0

Note: This device also supports BEF# controlled Block-Erase operation.
 The WE# and BEF# signals are interchangeable as long as minimum timings are meet. (See Table 15.)
 BA_x = Block Address
 X can be V_{IL} or V_{IH}, but no other value.

**FIGURE 14: FLASH WE# CONTROLLED BLOCK-ERASE TIMING DIAGRAM FOR WORD MODE
 (FOR BYTE MODE A₁ = DON'T CARE)**



1256 F14.0

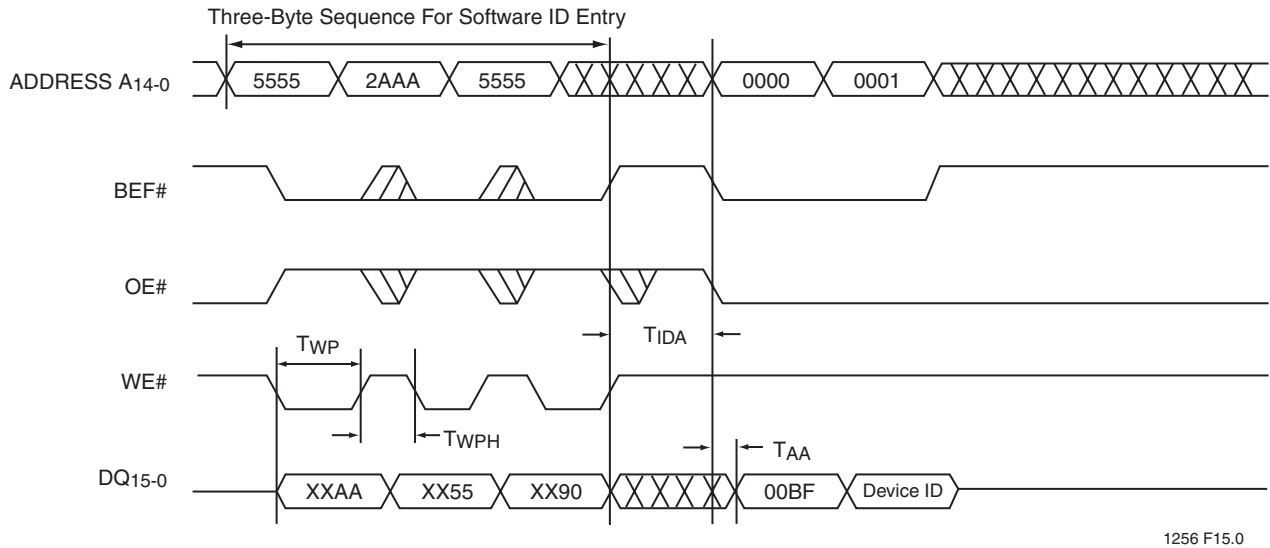
Note: This device also supports BEF# controlled Sector-Erase operation.
 The WE# and BEF# signals are interchangeable as long as minimum timings are meet. (See Table 15.)
 SA_x = Sector Address
 X can be V_{IL} or V_{IH}, but no other value.

**FIGURE 15: FLASH WE# CONTROLLED SECTOR-ERASE TIMING DIAGRAM FOR WORD MODE
 (FOR BYTE MODE A₁ = DON'T CARE)**



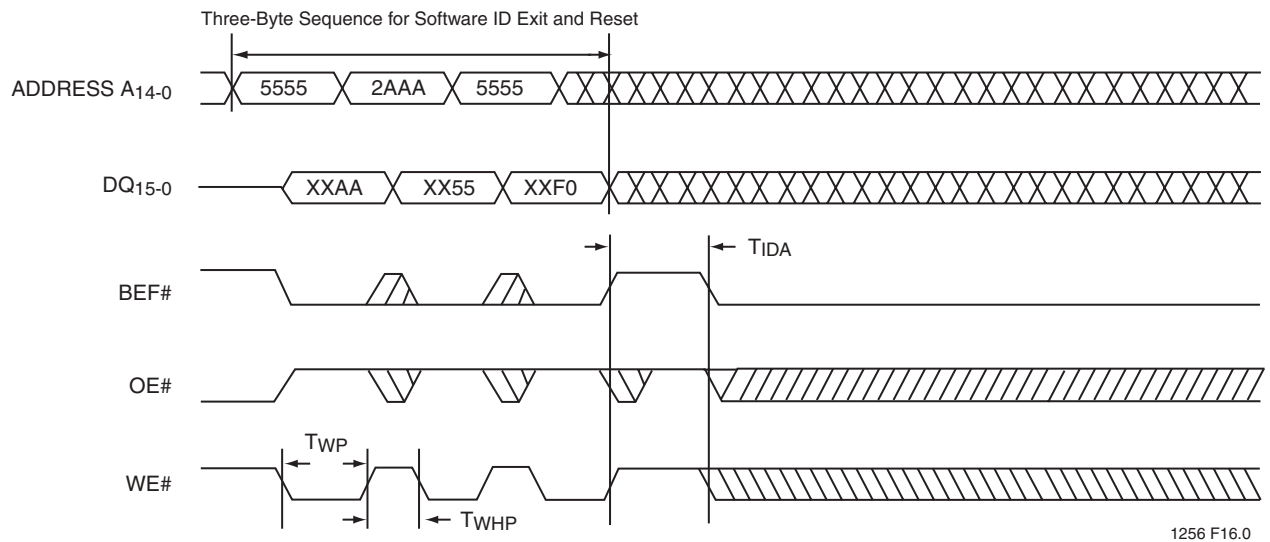
16 Mbit Concurrent SuperFlash + 2/4/8 Mbit SRAM ComboMemory
SST34HF1602C / SST34HF1622C / SST34HF1642C
SST34HF1642D / SST34HF1682D / SST34HF1622S / SST34HF1642S

Advance Information



Note: X can be V_{IL} or V_{IH}, but no other value.
 Device ID - 734AH for SST34HF16x2C/DS

FIGURE 16: FLASH SOFTWARE ID ENTRY AND READ FOR WORD MODE
(FOR BYTE MODE A₋₁ = 0)



Note: X can be V_{IL} or V_{IH}, but no other value

FIGURE 17: FLASH SOFTWARE ID EXIT FOR WORD MODE
(FOR BYTE MODE A₋₁ = 0)

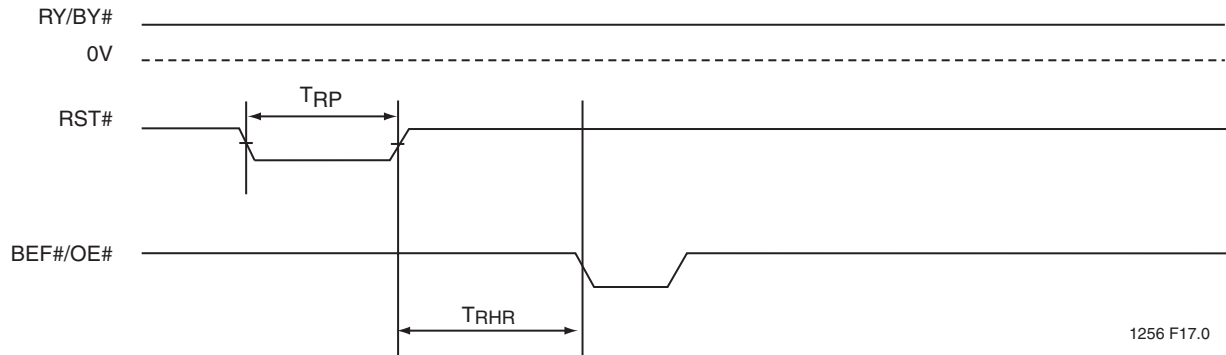


FIGURE 18: RST# TIMING (WHEN NO INTERNAL OPERATION IS IN PROGRESS)

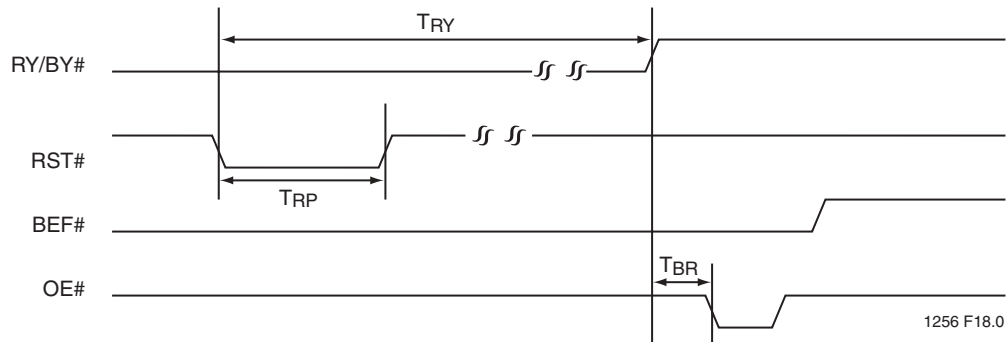


FIGURE 19: RST# TIMING (DURING SECTOR- OR BLOCK-ERASE OPERATION)



16 Mbit Concurrent SuperFlash + 2/4/8 Mbit SRAM ComboMemory
SST34HF1602C / SST34HF1622C / SST34HF1642C
SST34HF1642D / SST34HF1682D / SST34HF1622S / SST34HF1642S

Advance Information

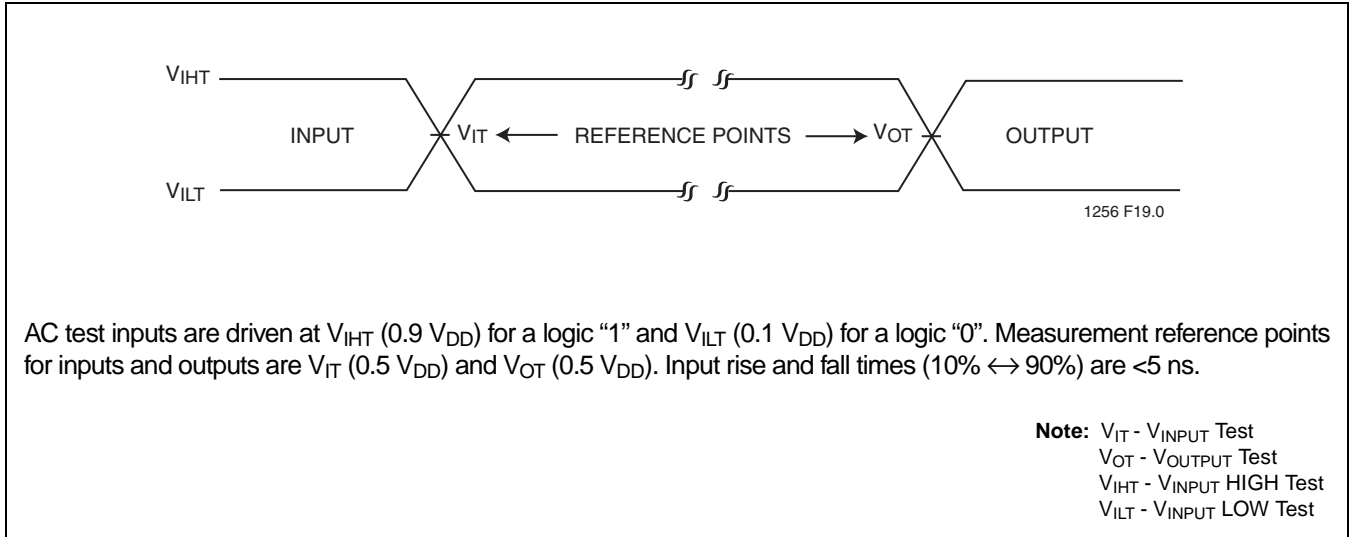


FIGURE 20: AC INPUT/OUTPUT REFERENCE WAVEFORMS

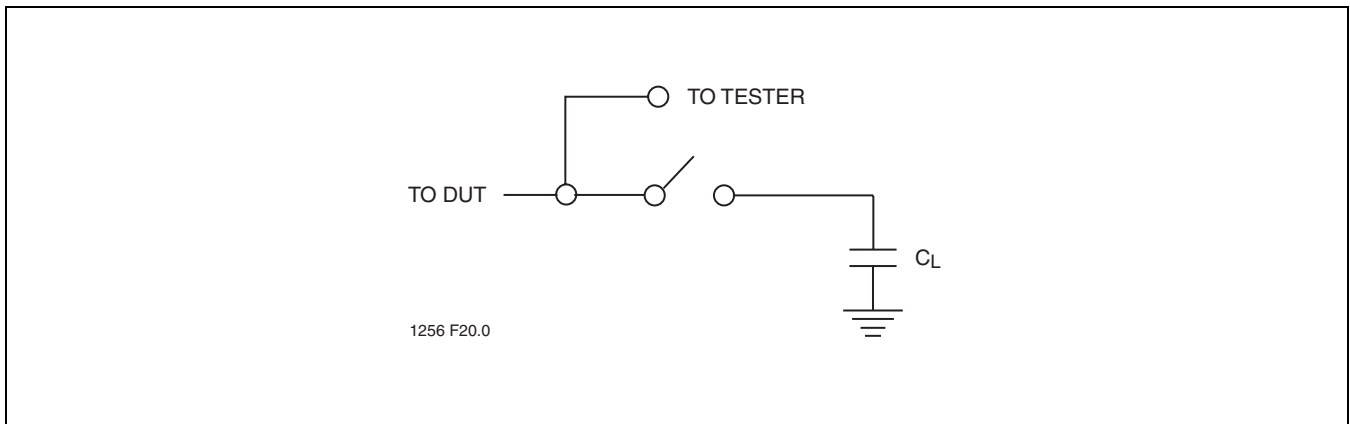


FIGURE 21: A TEST LOAD EXAMPLE

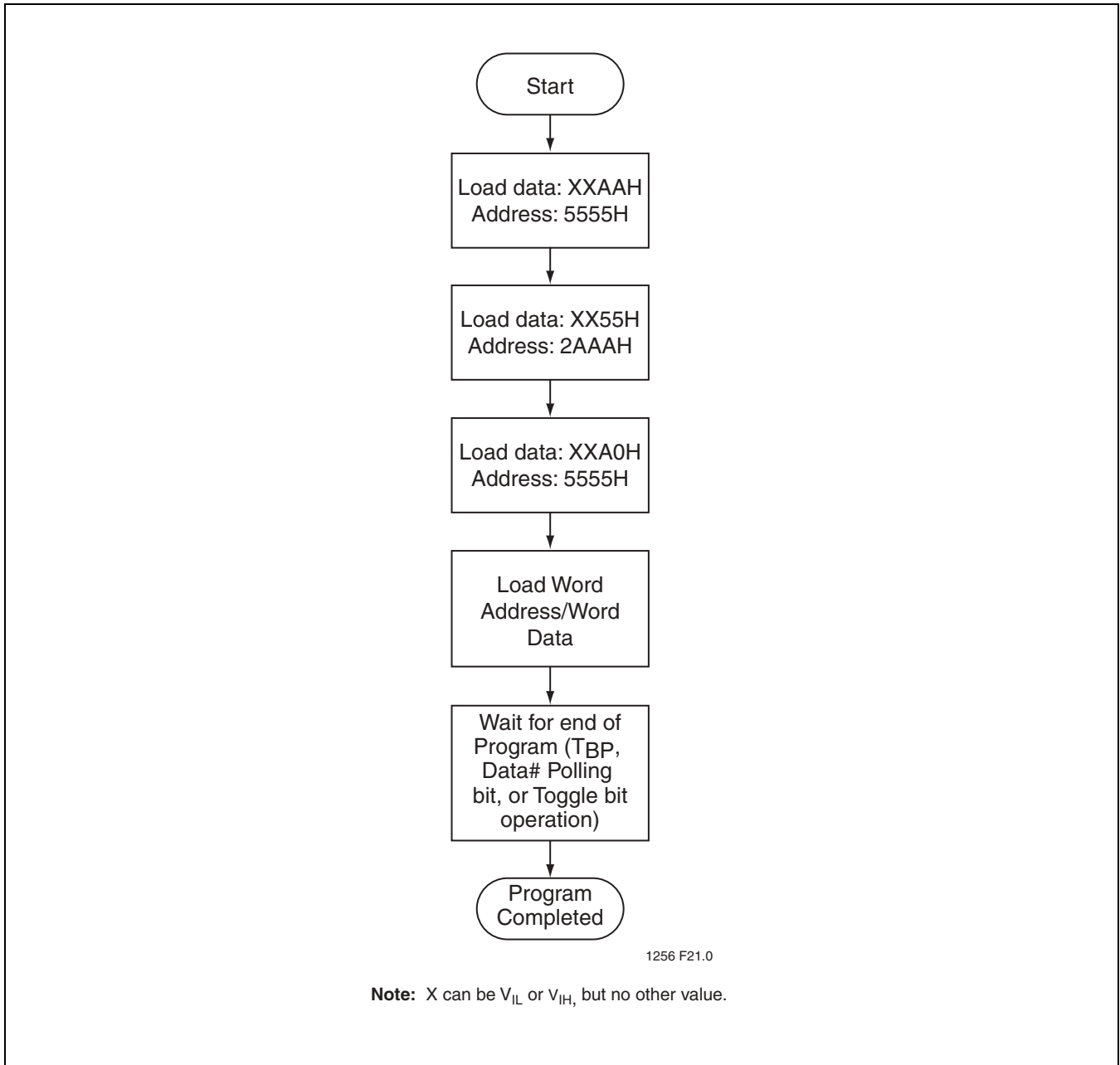


FIGURE 22: WORD-PROGRAM ALGORITHM



16 Mbit Concurrent SuperFlash + 2/4/8 Mbit SRAM ComboMemory
SST34HF1602C / SST34HF1622C / SST34HF1642C
SST34HF1642D / SST34HF1682D / SST34HF1622S / SST34HF1642S

Advance Information

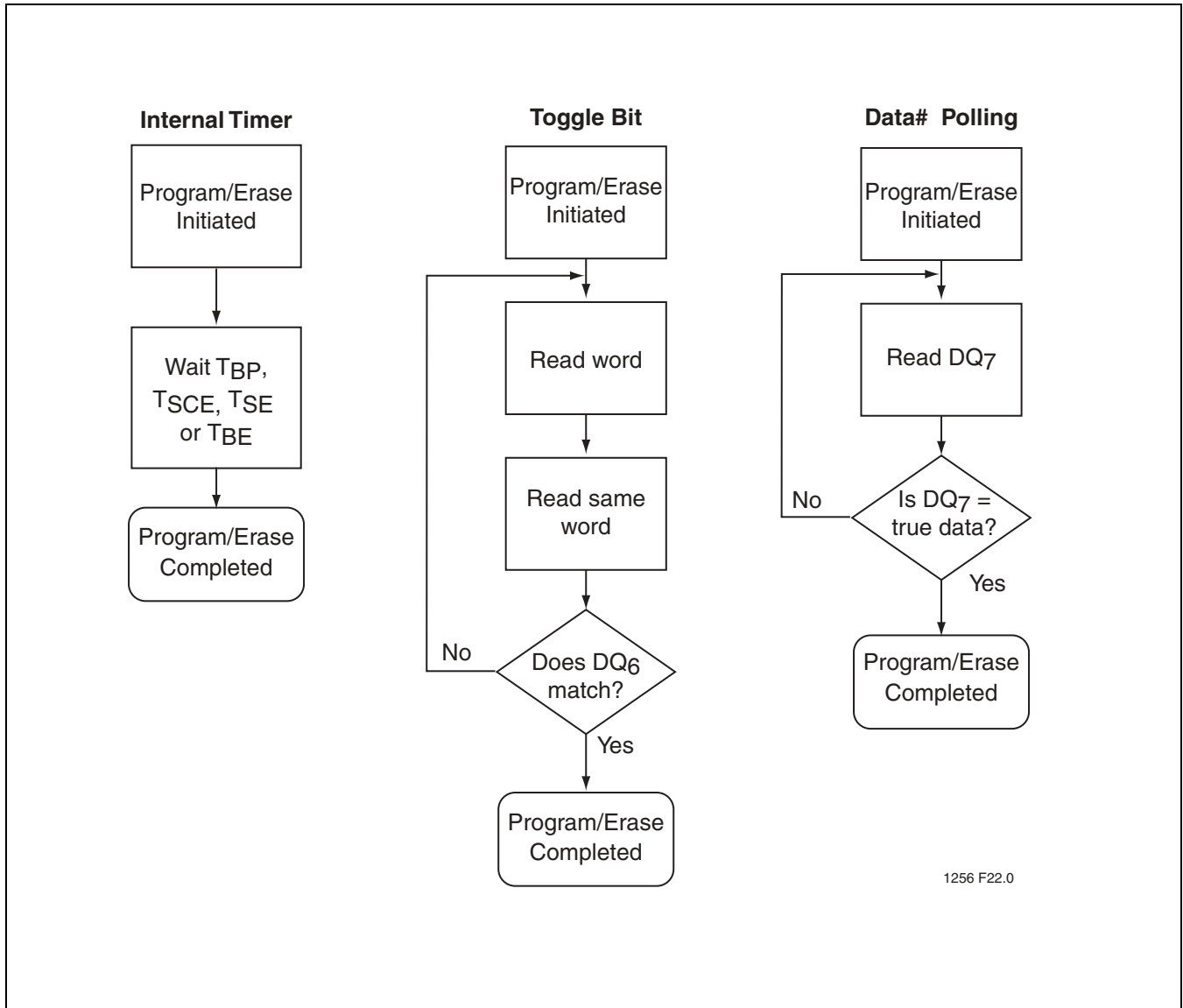


FIGURE 23: WAIT OPTIONS

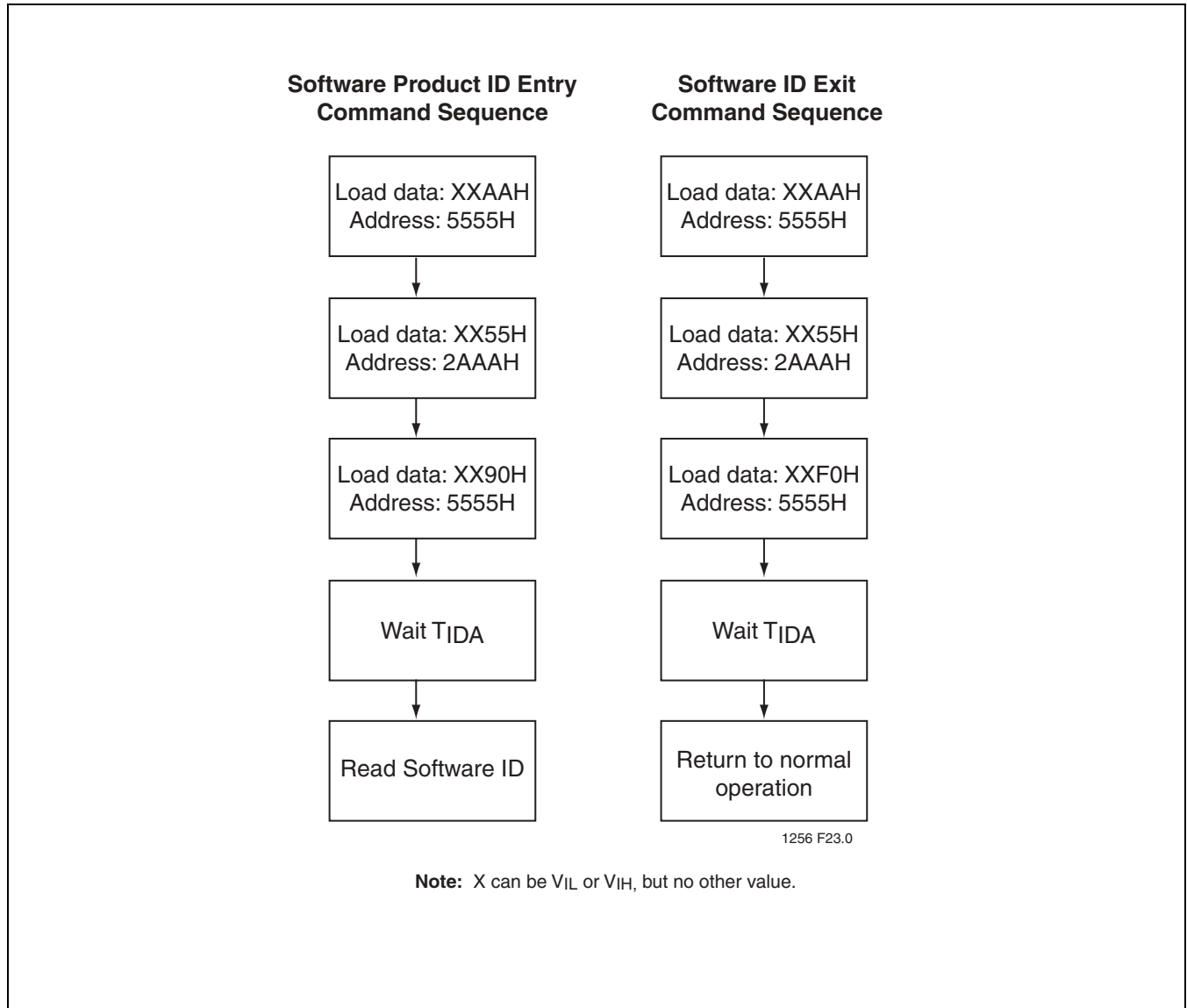


FIGURE 24: SOFTWARE PRODUCT ID COMMAND FLOWCHARTS



16 Mbit Concurrent SuperFlash + 2/4/8 Mbit SRAM ComboMemory
SST34HF1602C / SST34HF1622C / SST34HF1642C
SST34HF1642D / SST34HF1682D / SST34HF1622S / SST34HF1642S

Advance Information

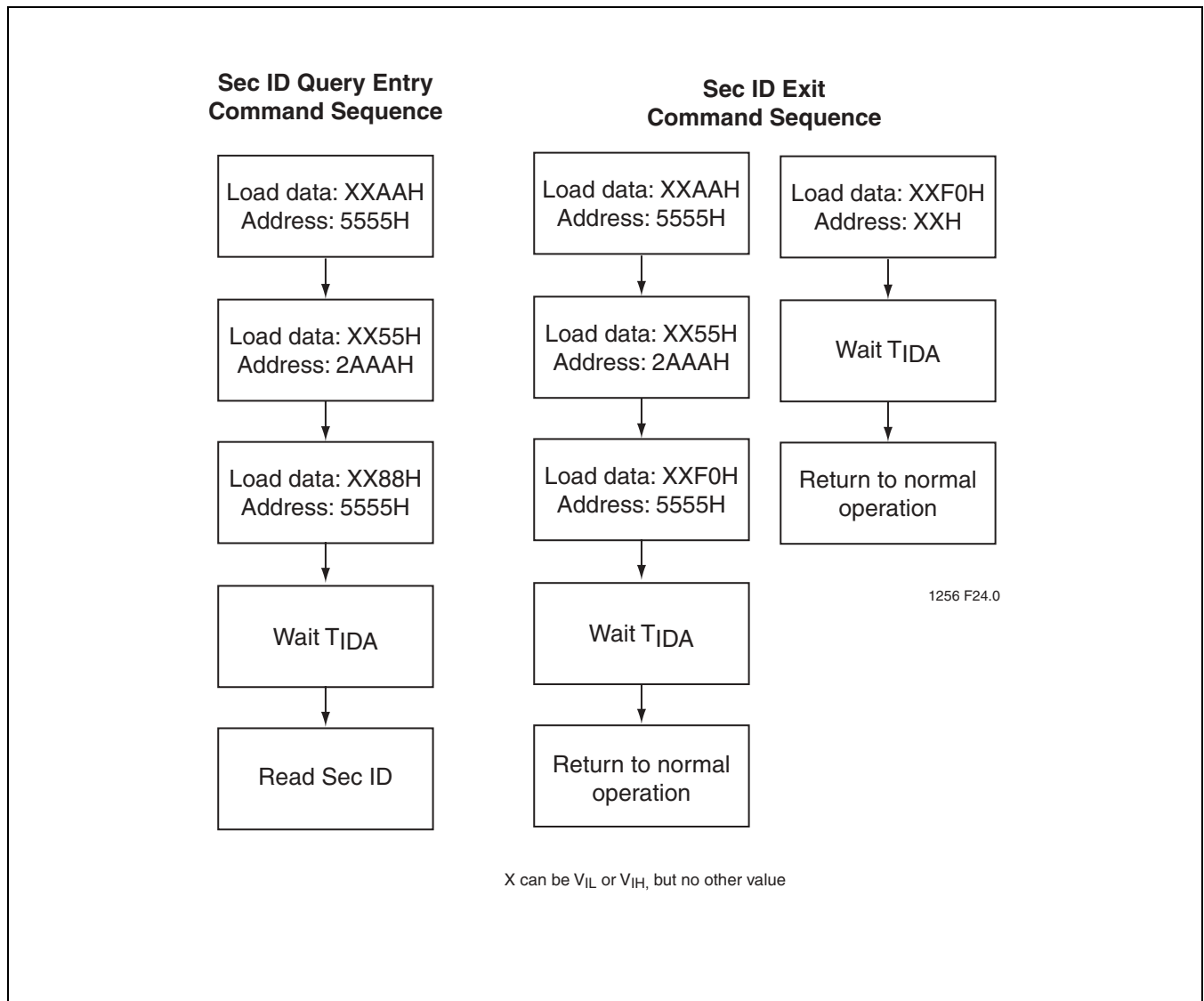


FIGURE 25: SOFTWARE SEC ID COMMAND FLOWCHARTS

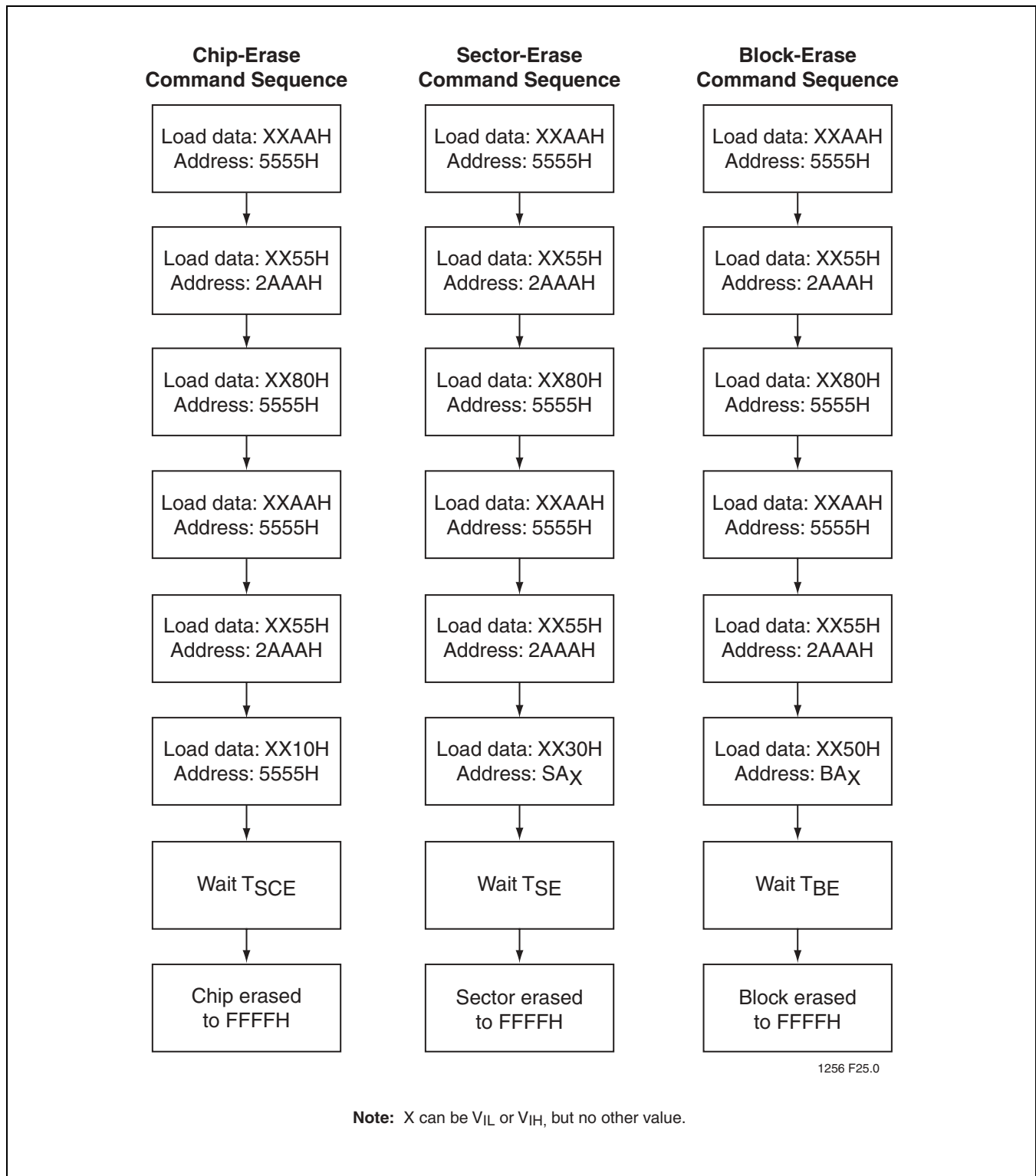


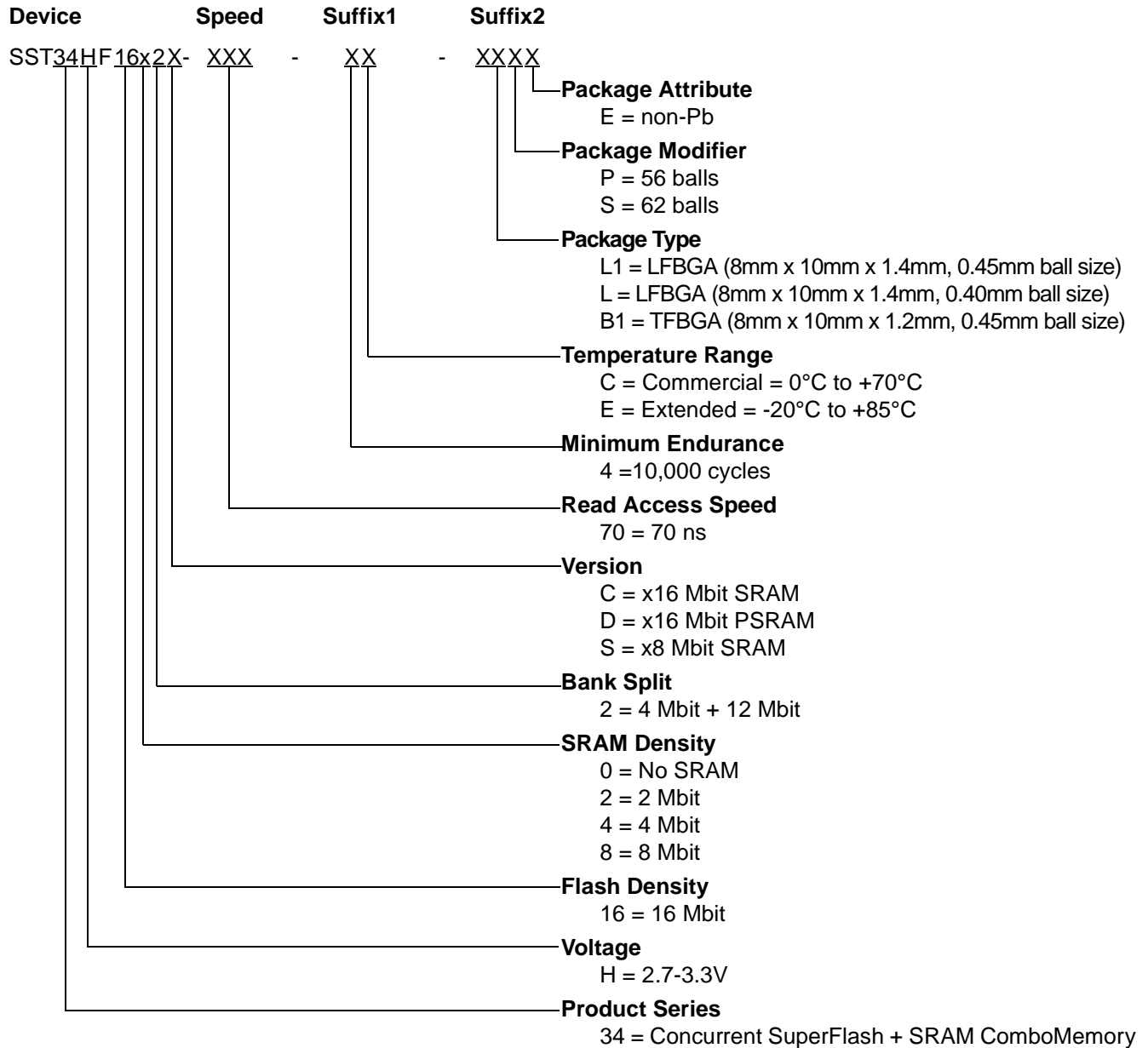
FIGURE 26: ERASE COMMAND SEQUENCE



16 Mbit Concurrent SuperFlash + 2/4/8 Mbit SRAM ComboMemory
SST34HF1602C / SST34HF1622C / SST34HF1642C
SST34HF1642D / SST34HF1682D / SST34HF1622S / SST34HF1642S

Advance Information

PRODUCT ORDERING INFORMATION



16 Mbit Concurrent SuperFlash + 2/4/8 Mbit SRAM ComboMemory
SST34HF1602C / SST34HF1622C / SST34HF1642C
SST34HF1642D / SST34HF1682D / SST34HF1622S / SST34HF1642S



Advance Information

Valid combinations for SST34HF1602C

SST34HF1602C-70-4C-L1P	SST34HF1602C-70-4C-LS	SST34HF1602C-70-4C-B1P
SST34HF1602C-70-4C-L1PE	SST34HF1602C-70-4C-LSE	SST34HF1602C-70-4C-B1PE
SST34HF1602C-70-4E-L1P	SST34HF1602C-70-4E-LS	SST34HF1602C-70-4E-B1P
SST34HF1602C-70-4E-L1PE	SST34HF1602C-70-4E-LSE	SST34HF1602C-70-4E-B1PE

Valid combinations for SST34HF1622C

SST34HF1622C-70-4C-L1P	SST34HF1622C-70-4C-LS
SST34HF1622C-70-4C-L1PE	SST34HF1622C-70-4C-LSE
SST34HF1622C-70-4E-L1P	SST34HF1622C-70-4E-LS
SST34HF1622C-70-4E-L1PE	SST34HF1622C-70-4E-LSE

Valid combinations for SST34HF1622S

SST34HF1622S-70-4C-L1P
SST34HF1622S-70-4C-L1PE
SST34HF1622S-70-4E-L1P
SST34HF1622S-70-4E-L1PE

Valid combinations for SST34HF1642C

SST34HF1642C-70-4C-L1P	SST34HF1642C-70-4C-LS
SST34HF1642C-70-4C-L1PE	SST34HF1642C-70-4C-LSE
SST34HF1642C-70-4E-L1P	SST34HF1642C-70-4E-LS
SST34HF1642C-70-4E-L1PE	SST34HF1642C-70-4E-LSE

Valid combinations for SST34HF1642D

SST34HF1642D-70-4C-L1P	SST34HF1642D-70-4C-LS
SST34HF1642D-70-4C-L1PE	SST34HF1642D-70-4C-LSE
SST34HF1642D-70-4E-L1P	SST34HF1642D-70-4E-LS
SST34HF1642D-70-4E-L1PE	SST34HF1642D-70-4E-LSE

Valid combinations for SST34HF1642S

SST34HF1642S-70-4C-L1P
SST34HF1642S-70-4C-L1PE
SST34HF1642S-70-4E-L1P
SST34HF1642S-70-4E-L1PE

Valid combinations for SST34HF1682D

SST34HF1682D-70-4C-L1P	SST34HF1682D-70-4C-LS
SST34HF1682D-70-4C-L1PE	SST34HF1682D-70-4C-LSE
SST34HF1682D-70-4E-L1P	SST34HF1682D-70-4E-LS
SST34HF1682D-70-4E-L1PE	SST34HF1682D-70-4E-LSE

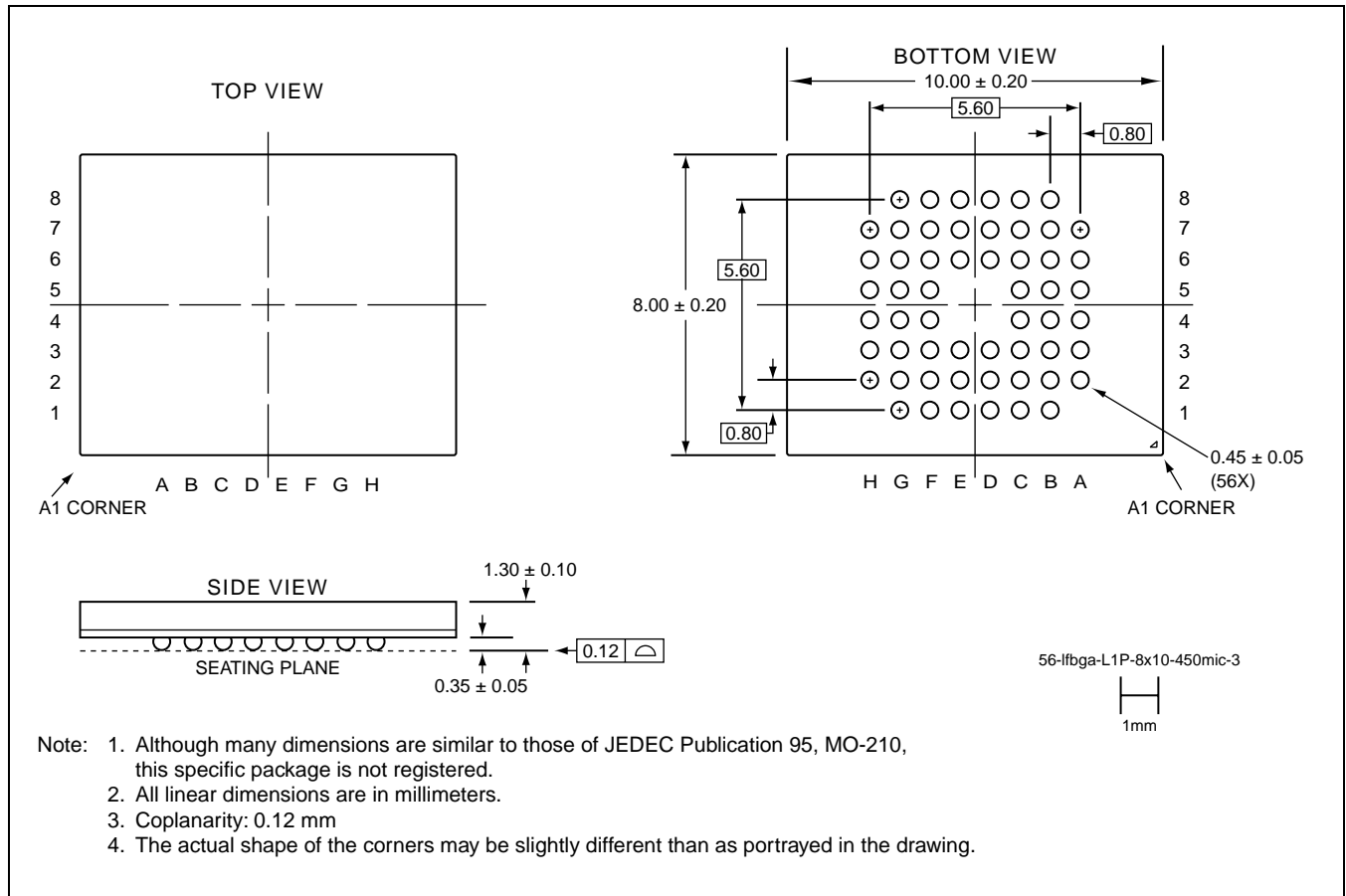
Note: Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.



16 Mbit Concurrent SuperFlash + 2/4/8 Mbit SRAM ComboMemory
SST34HF1602C / SST34HF1622C / SST34HF1642C
SST34HF1642D / SST34HF1682D / SST34HF1622S / SST34HF1642S

Advance Information

PACKAGING DIAGRAMS



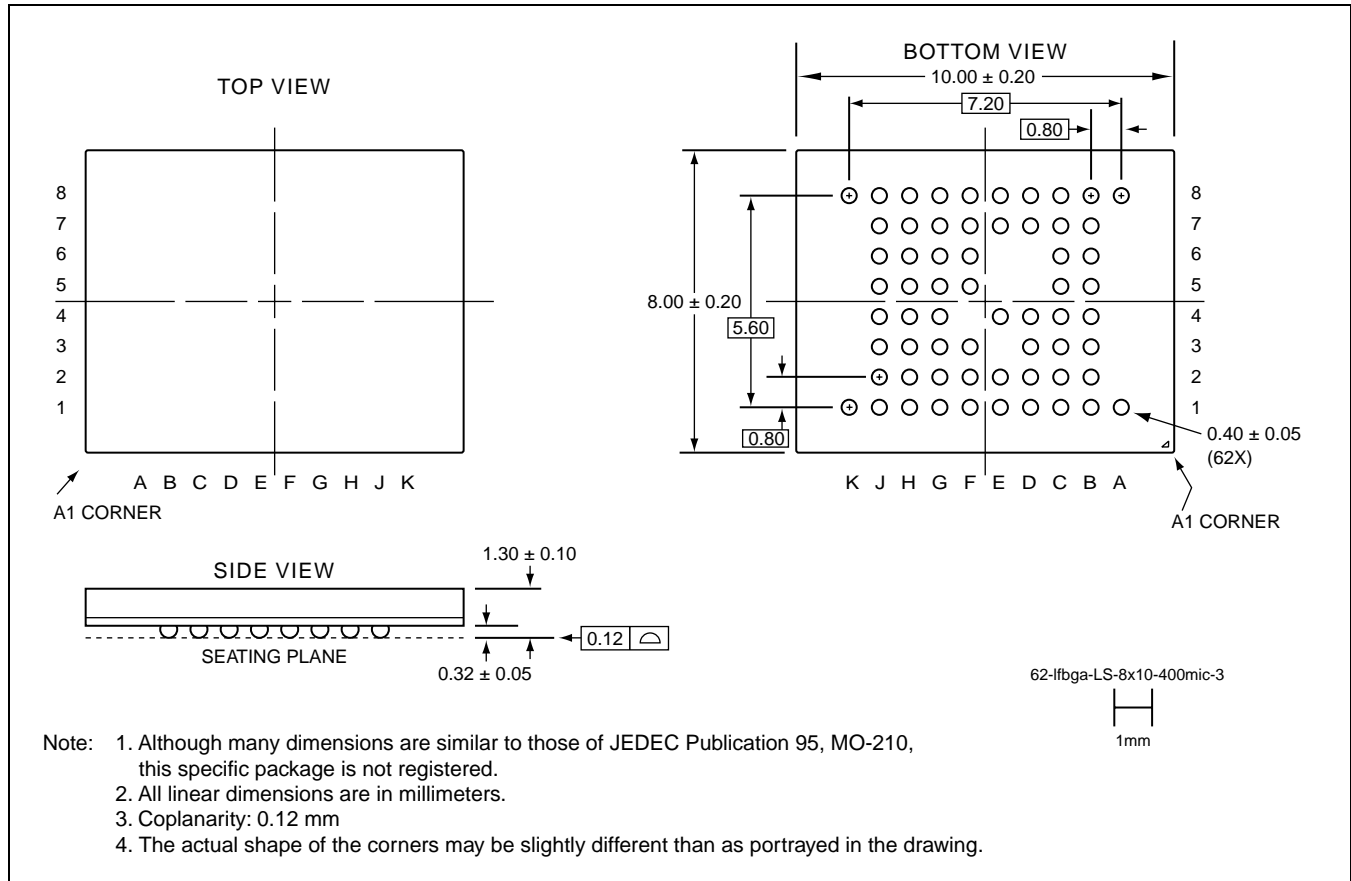
- Note:
1. Although many dimensions are similar to those of JEDEC Publication 95, MO-210, this specific package is not registered.
 2. All linear dimensions are in millimeters.
 3. Coplanarity: 0.12 mm
 4. The actual shape of the corners may be slightly different than as portrayed in the drawing.

56-BALL LOW-PROFILE, FINE-PITCH BALL GRID ARRAY (LFBGA) 8MM X 10MM
SST PACKAGE CODE: L1P

16 Mbit Concurrent SuperFlash + 2/4/8 Mbit SRAM ComboMemory
SST34HF1602C / SST34HF1622C / SST34HF1642C
SST34HF1642D / SST34HF1682D / SST34HF1622S / SST34HF1642S



Advance Information

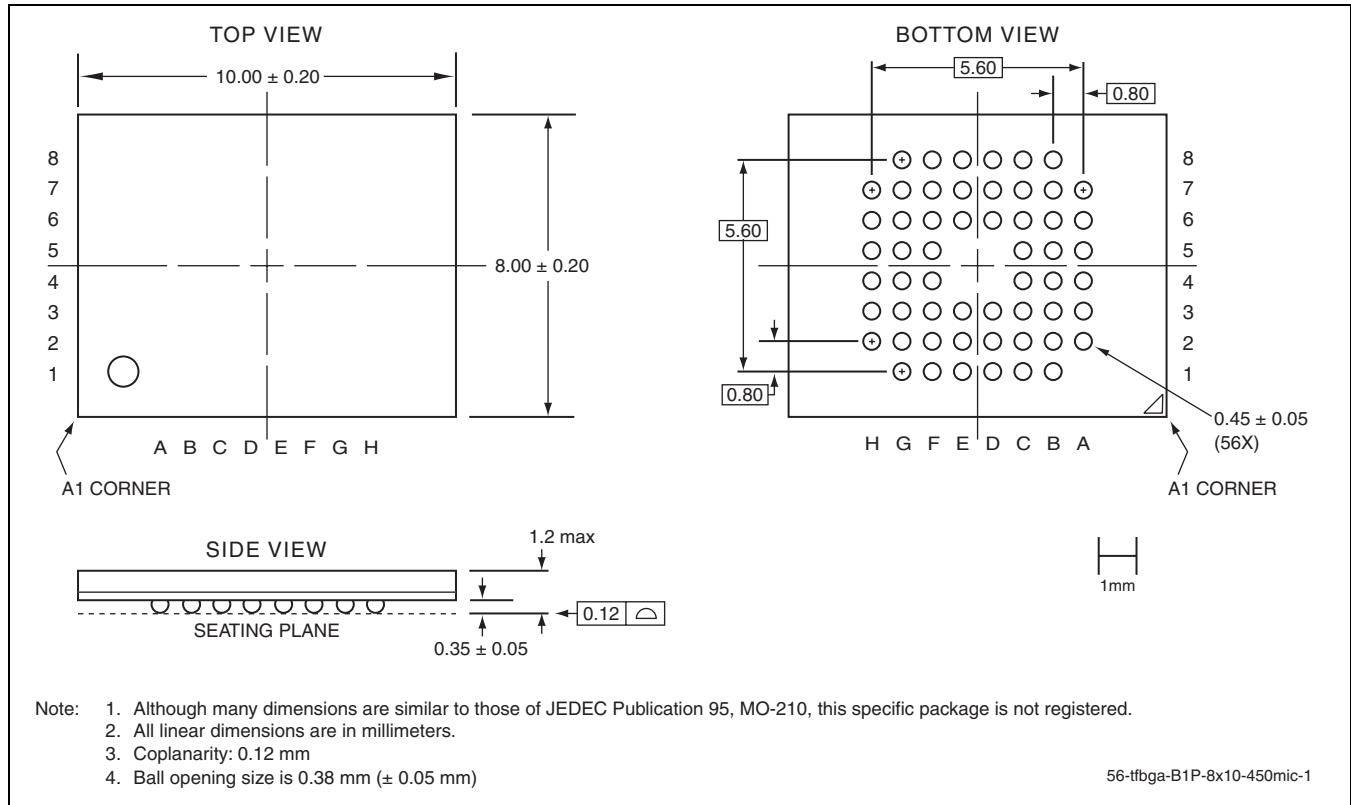


62-BALL LOW-PROFILE, FINE-PITCH BALL GRID ARRAY (LFBGA) 8MM X 10MM
SST PACKAGE CODE: LS



16 Mbit Concurrent SuperFlash + 2/4/8 Mbit SRAM ComboMemory
SST34HF1602C / SST34HF1622C / SST34HF1642C
SST34HF1642D / SST34HF1682D / SST34HF1622S / SST34HF1642S

Advance Information



56-BALL THIN-PROFILE, FINE-PITCH BALL GRID ARRAY (TFBGA) 8MM X 10MM
SST PACKAGE CODE: B1P

TABLE 16: REVISION HISTORY

Number	Description	Date
00	• Initial Release	Mar 2004