

- Member of the Texas Instruments Widebus™ Family
- High-Bandwidth Data Path (Up To 500 MHz†)
- 5-V Tolerant I/Os with Device Powered Up or Powered Down
- Low and Flat ON-State Resistance ( $r_{on}$ ) Characteristics Over Operating Range ( $r_{on} = 5 \Omega$  Typical)
- Rail-to-Rail Switching on Data I/O Ports
  - 0-V to 5-V Switching With 3.3-V  $V_{CC}$
  - 0-V to 3.3-V Switching With 2.5-V  $V_{CC}$
- Bidirectional Data Flow, With Near-Zero Propagation Delay
- Low Input/Output Capacitance Minimizes Loading and Signal Distortion ( $C_{io(OFF)} = 4 \text{ pF}$  Typical)
- Fast Switching Frequency ( $f_{OE} = 20 \text{ MHz}$  Max)
- Data and Control Inputs Provide Undershoot Clamp Diodes
- Low Power Consumption ( $I_{CC} = 1 \text{ mA}$  Typical)
- $V_{CC}$  Operating Range From 2.3 V to 3.6 V
- Data I/Os Support 0-V to 5-V Signaling Levels (0.8 V, 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V, 5 V)
- Control Inputs Can be Driven by TTL or 5-V/3.3-V CMOS Outputs
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
  - 2000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)
- Supports Both Digital and Analog Applications: PCI Interface, Differential Signal Interface, Memory Interleaving, Bus Isolation, Low-Distortion Signal Gating

DGG, DGV, OR DL PACKAGE  
(TOP VIEW)

NC	1	56	$\overline{1OE}$
1A1	2	55	$\overline{2OE}$
1A2	3	54	1B1
1A3	4	53	1B2
1A4	5	52	1B3
1A5	6	51	1B4
1A6	7	50	1B5
GND	8	49	GND
1A7	9	48	1B6
1A8	10	47	1B7
1A9	11	46	1B8
1A10	12	45	1B9
1A11	13	44	1B10
1A12	14	43	1B11
2A1	15	42	1B12
2A2	16	41	2B1
$V_{CC}$	17	40	2B2
2A3	18	39	2B3
GND	19	38	GND
2A4	20	37	2B4
2A5	21	36	2B5
2A6	22	35	2B6
2A7	23	34	2B7
2A8	24	33	2B8
2A9	25	32	2B9
2A10	26	31	2B10
2A11	27	30	2B11
2A12	28	29	2B12

NC – No internal connection

† For additional information regarding the performance characteristics of the CB3Q family, refer to the TI application report, *CBT-C*, *CB3T*, and *CB3Q Signal-Switch Families*, literature number SCDA008.

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# SN74CB3Q16211

## 24-BIT SWITCH

### 2.5-V/3.3-V LOW-VOLTAGE FET BUS SWITCH

SCDS167 – MAY 2004

#### description/ordering information

The SN74CB3Q16211 is a high-bandwidth FET bus switch utilizing a charge pump to elevate the gate voltage of the pass transistor, providing a low and flat ON-state resistance ( $r_{ON}$ ). The low and flat ON-state resistance allows for minimal propagation delay and supports rail-to-rail switching on the data input/output (I/O) ports. The device also features low data I/O capacitance to minimize capacitive loading and signal distortion on the data bus. Specifically designed to support high-bandwidth applications, the SN74CB3Q16211 provides an optimized interface solution ideally suited for broadband communications, networking, and data-intensive computing systems.

The SN74CB3Q16211 is organized as two 12-bit bus switches with separate output-enable ( $\overline{1OE}$ ,  $\overline{2OE}$ ) inputs. It can be used as two 12-bit bus switches or as one 24-bit bus switch. When  $\overline{OE}$  is low, the associated 12-bit bus switch is ON and the A port is connected to the B port, allowing bidirectional data flow between ports. When  $\overline{OE}$  is high, the associated 12-bit bus switch is OFF, and a high-impedance state exists between the A and B ports.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry prevents damaging current backflow through the device when it is powered down.

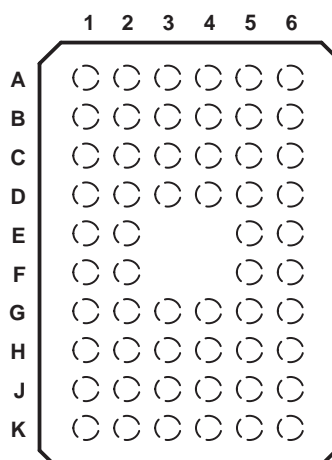
To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

#### ORDERING INFORMATION

$T_A$	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	SSOP – DL	Tube	SN74CB3Q16211DL	CB3Q16211
		Tape and reel	SN74CB3Q16211DLR	
	TSSOP – DGG	Tape and reel	SN74CB3Q16211DGGR	CB3Q16211
	TVSOP – DGV	Tape and reel	SN74CB3Q16211DGVR	BW211
	VFBGA – GQL	Tape and reel	SN74CB3Q16211GQLR	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

#### GQL PACKAGE (TOP VIEW)



#### terminal assignments

	1	2	3	4	5	6
A	1A2	1A1	NC	$\overline{1OE}$	$\overline{2OE}$	1B1
B	1A5	1A4	1A3	1B2	1B3	1B4
C	1A7	GND	1A6	1B5	GND	1B6
D	1A10	1A8	1A9	1B8	1B7	1B9
E	1A12	1A11			1B10	1B11
F	2A1	2A2			2B1	1B12
G	$V_{CC}$	GND	2A3	2B3	GND	2B2
H	2A4	2A5	2A6	2B6	2B5	2B4
J	2A7	2A8	2A9	2B9	2B8	2B7
K	2A10	2A11	2A12	2B12	2B11	2B10

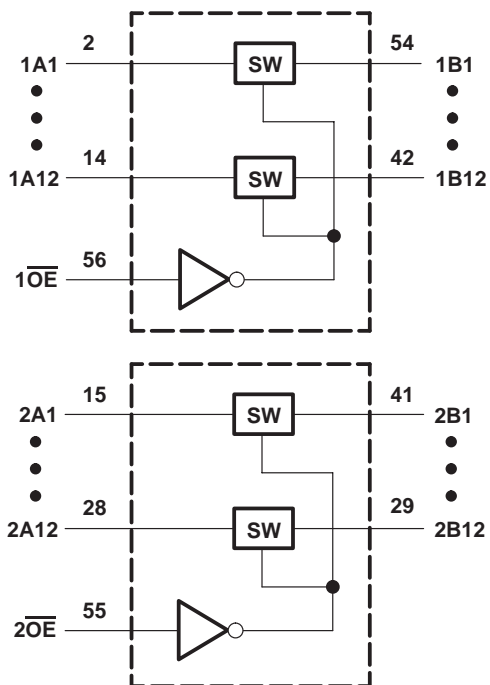
NC – No internal connection

**SN74CB3Q16211**  
**24-BIT SWITCH**  
**2.5-V/3.3-V LOW-VOLTAGE FET BUS SWITCH**  
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**FUNCTION TABLE**  
 (each 12-bit bus switch)

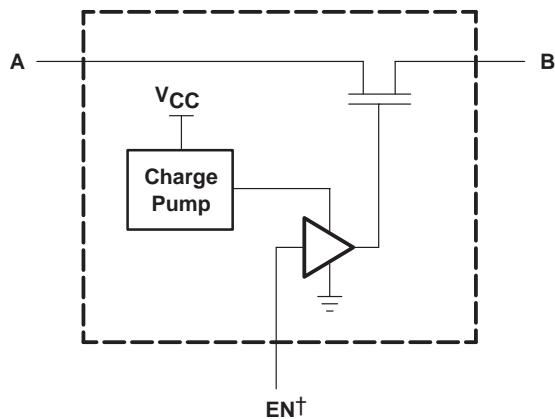
INPUT OE	INPUT/OUTPUT A	FUNCTION
L	B	A port = B port
H	Z	Disconnect

**logic diagram (positive logic)**



Pin numbers shown are for the DGG, DGV, and DL packages.

**simplified schematic, each FET switch (SW)**



† EN is the internal enable signal applied to the switch.



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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
$V_{IK}$		$V_{CC} = 3.6\text{ V}$ ,	$I_I = -18\text{ mA}$			-1.8	V
$I_{IN}$	Control inputs	$V_{CC} = 3.6\text{ V}$ ,	$V_{IN} = 0\text{ to }5.5\text{ V}$			$\pm 1$	$\mu\text{A}$
$I_{OZ}‡$		$V_{CC} = 3.6\text{ V}$ ,	$V_O = 0\text{ to }5.5\text{ V}$ , $V_I = 0$ , Switch OFF, $V_{IN} = V_{CC}\text{ or GND}$			$\pm 1$	$\mu\text{A}$
$I_{off}$		$V_{CC} = 0$ ,	$V_O = 0\text{ to }5.5\text{ V}$ , $V_I = 0$			1	$\mu\text{A}$
$I_{CC}$		$V_{CC} = 3.6\text{ V}$ ,	$I_{I/O} = 0$ , Switch ON or OFF, $V_{IN} = V_{CC}\text{ or GND}$		1	3	mA
$\Delta I_{CC}§$	Control inputs	$V_{CC} = 3.6\text{ V}$ ,	One input at 3 V, Other inputs at $V_{CC}\text{ or GND}$			30	$\mu\text{A}$
$I_{CCD}¶$	Per control input	$V_{CC} = 3.6\text{ V}$ ,	A and B ports open, Control input switching at 50% duty cycle		0.15	0.25	mA/MHz
$C_{in}$	Control inputs	$V_{CC} = 3.3\text{ V}$ ,	$V_{IN} = 5.5\text{ V}, 3.3\text{ V},\text{ or }0$		3.5	5	pF
$C_{iO(OFF)}$		$V_{CC} = 3.3\text{ V}$ ,	Switch OFF, $V_{IN} = V_{CC}\text{ or GND}$ , $V_{I/O} = 5.5\text{ V}, 3.3\text{ V},\text{ or }0$		4	5	pF
$C_{iO(ON)}$		$V_{CC} = 3.3\text{ V}$ ,	Switch ON, $V_{IN} = V_{CC}\text{ or GND}$ , $V_{I/O} = 5.5\text{ V}, 3.3\text{ V},\text{ or }0$		10	12.5	pF
$r_{on}^\#$	$V_{CC} = 2.3\text{ V}$ , TYP at $V_{CC} = 2.5\text{ V}$	$V_I = 0$ ,	$I_O = 30\text{ mA}$		5	8	$\Omega$
		$V_I = 1.7\text{ V}$ ,	$I_O = -15\text{ mA}$		5	9	
	$V_{CC} = 3\text{ V}$	$V_I = 0$ ,	$I_O = 30\text{ mA}$		5	6.5	
		$V_I = 2.4\text{ V}$ ,	$I_O = -15\text{ mA}$		5	8	

NOTE 7:  $V_{IN}$  and  $I_{IN}$  refer to control inputs.  $V_I$ ,  $V_O$ ,  $I_I$ , and  $I_O$  refer to data pins.

† All typical values are at  $V_{CC} = 3.3\text{ V}$  (unless otherwise noted),  $T_A = 25^\circ\text{C}$ .

‡ For I/O ports, the parameter  $I_{OZ}$  includes the input leakage current.

§ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than  $V_{CC}$  or GND.

¶ This parameter specifies the dynamic power-supply current associated with the operating frequency of a single control input (see Figure 2).

# Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

**switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	
$f_{OE}  $	$\overline{OE}$	A or B		10		20	MHz
$t_{pd}^*$	A or B	B or A		0.15		0.25	ns
$t_{en}$	$\overline{OE}$	A or B	1.5	8	1.5	8	ns
$t_{dis}$	$\overline{OE}$	A or B	1	7.5	1	7.5	ns

|| Maximum switching frequency for control input ( $V_O > V_{CC}$ ,  $V_I = 5\text{ V}$ ,  $R_L \geq 1\text{ M}\Omega$ ,  $C_L = 0$ )

\* The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

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**2.5-V/3.3-V LOW-VOLTAGE FET BUS SWITCH**  
 SCDS167 – MAY 2004

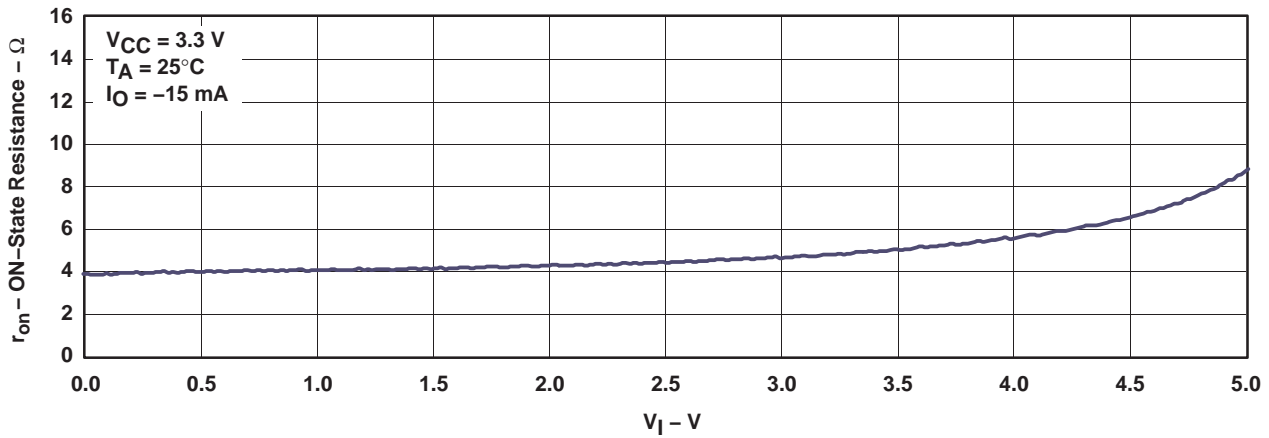


Figure 1. Typical  $r_{on}$  vs  $V_I$

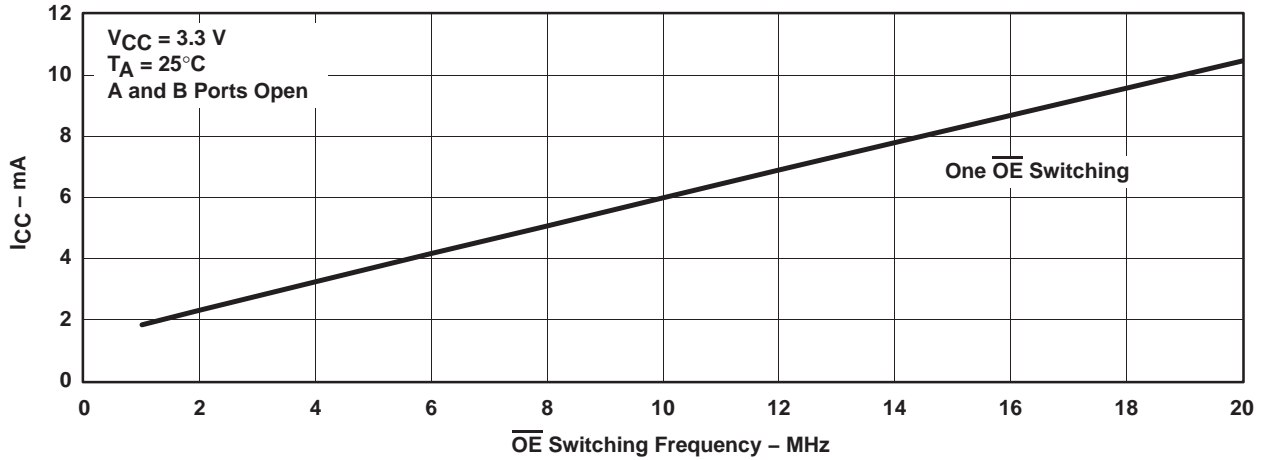
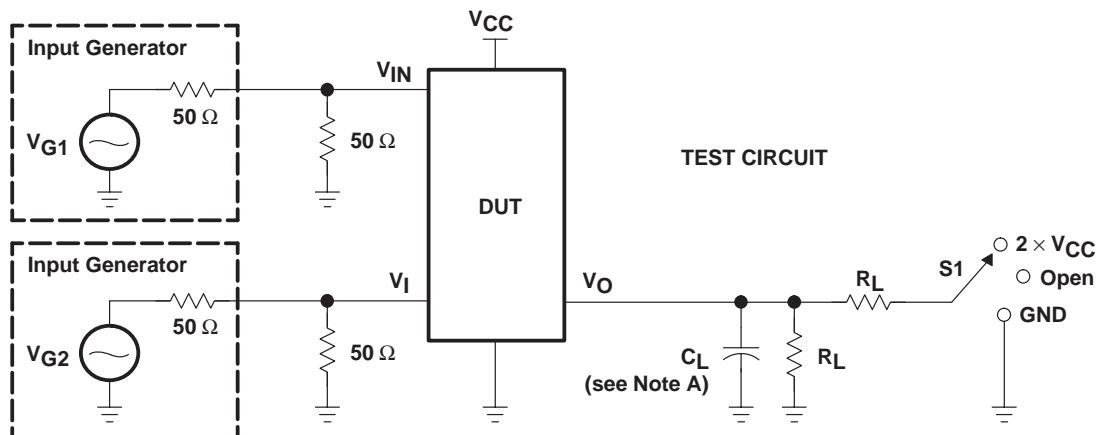
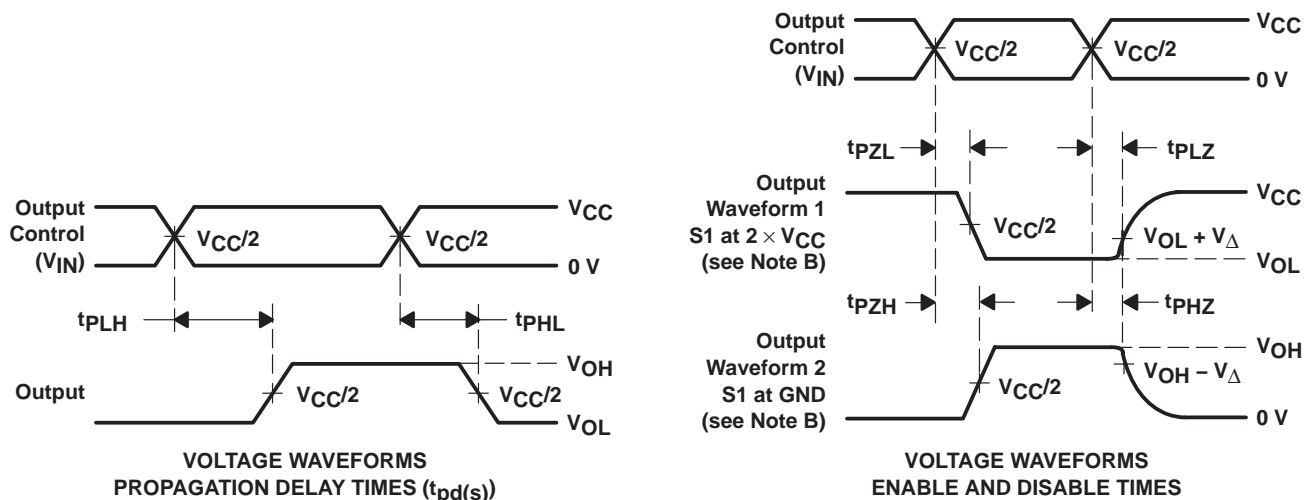


Figure 2. Typical  $I_{CC}$  vs  $\overline{OE}$  Switching Frequency

**PARAMETER MEASUREMENT INFORMATION**



TEST	V <sub>CC</sub>	S1	R <sub>L</sub>	V <sub>I</sub>	C <sub>L</sub>	V <sub>Δ</sub>
t <sub>pd</sub> (s)	2.5 V ± 0.2 V	Open	500 Ω	V <sub>CC</sub> or GND	30 pF	
	3.3 V ± 0.3 V	Open	500 Ω	V <sub>CC</sub> or GND	50 pF	
t <sub>PLZ</sub> /t <sub>PZL</sub>	2.5 V ± 0.2 V	2 × V <sub>CC</sub>	500 Ω	GND	30 pF	0.15 V
	3.3 V ± 0.3 V	2 × V <sub>CC</sub>	500 Ω	GND	50 pF	0.3 V
t <sub>PHZ</sub> /t <sub>PZH</sub>	2.5 V ± 0.2 V	GND	500 Ω	V <sub>CC</sub>	30 pF	0.15 V
	3.3 V ± 0.3 V	GND	500 Ω	V <sub>CC</sub>	50 pF	0.3 V



- NOTES:
- A. C<sub>L</sub> includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>O</sub> = 50 Ω, t<sub>r</sub> ≤ 2.5 ns, t<sub>f</sub> ≤ 2.5 ns.
  - D. The outputs are measured one at a time, with one transition per measurement.
  - E. t<sub>PLZ</sub> and t<sub>PHZ</sub> are the same as t<sub>dis</sub>.
  - F. t<sub>PZL</sub> and t<sub>PZH</sub> are the same as t<sub>en</sub>.
  - G. t<sub>PLH</sub> and t<sub>PHL</sub> are the same as t<sub>pd</sub>(s). The t<sub>pd</sub> propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
  - H. All parameters and waveforms are not applicable to all devices.

**Figure 3. Test Circuit and Voltage Waveforms**

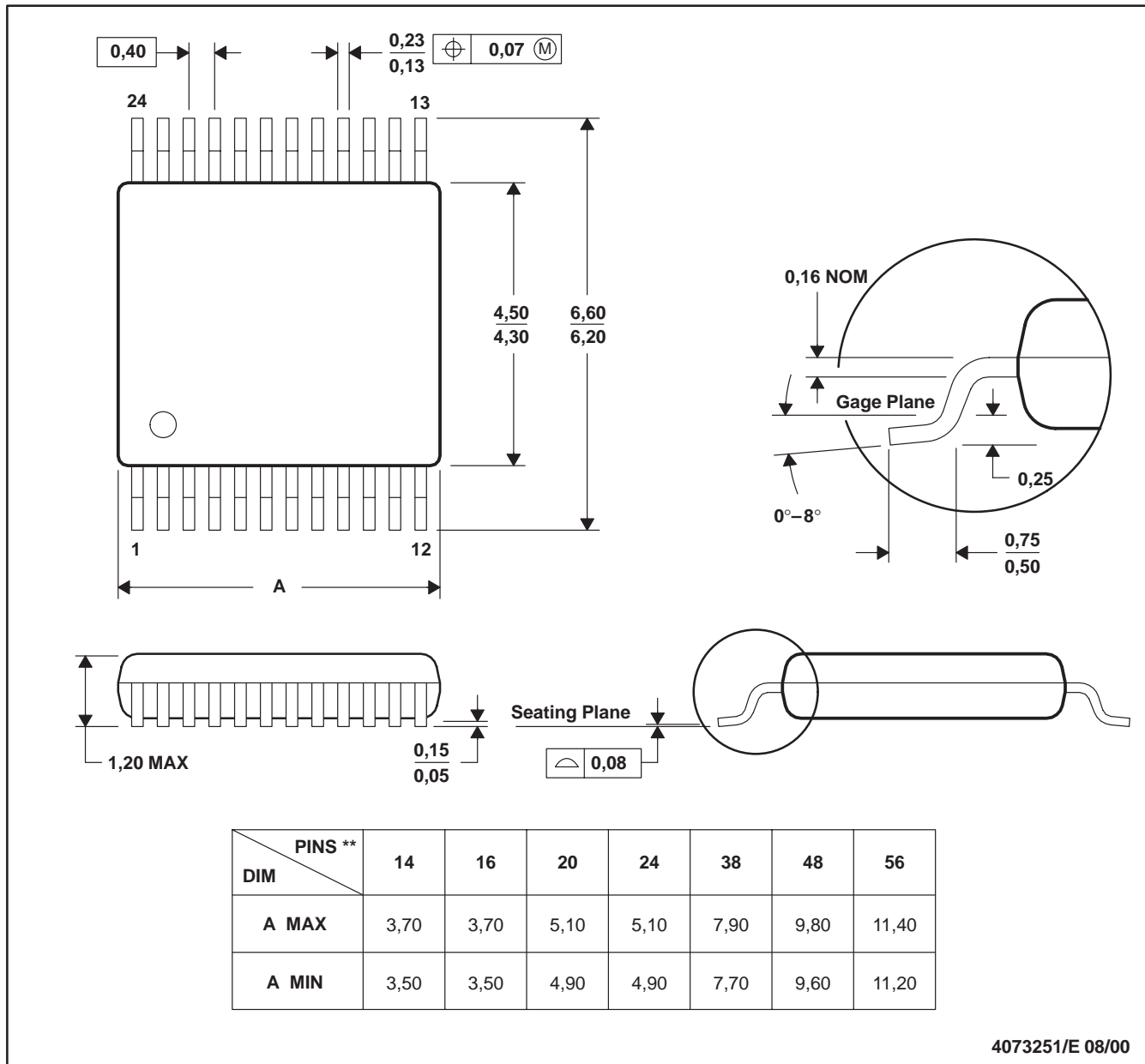
# MECHANICAL DATA

MPDS006C – FEBRUARY 1996 – REVISED AUGUST 2000

## DGV (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

24 PINS SHOWN



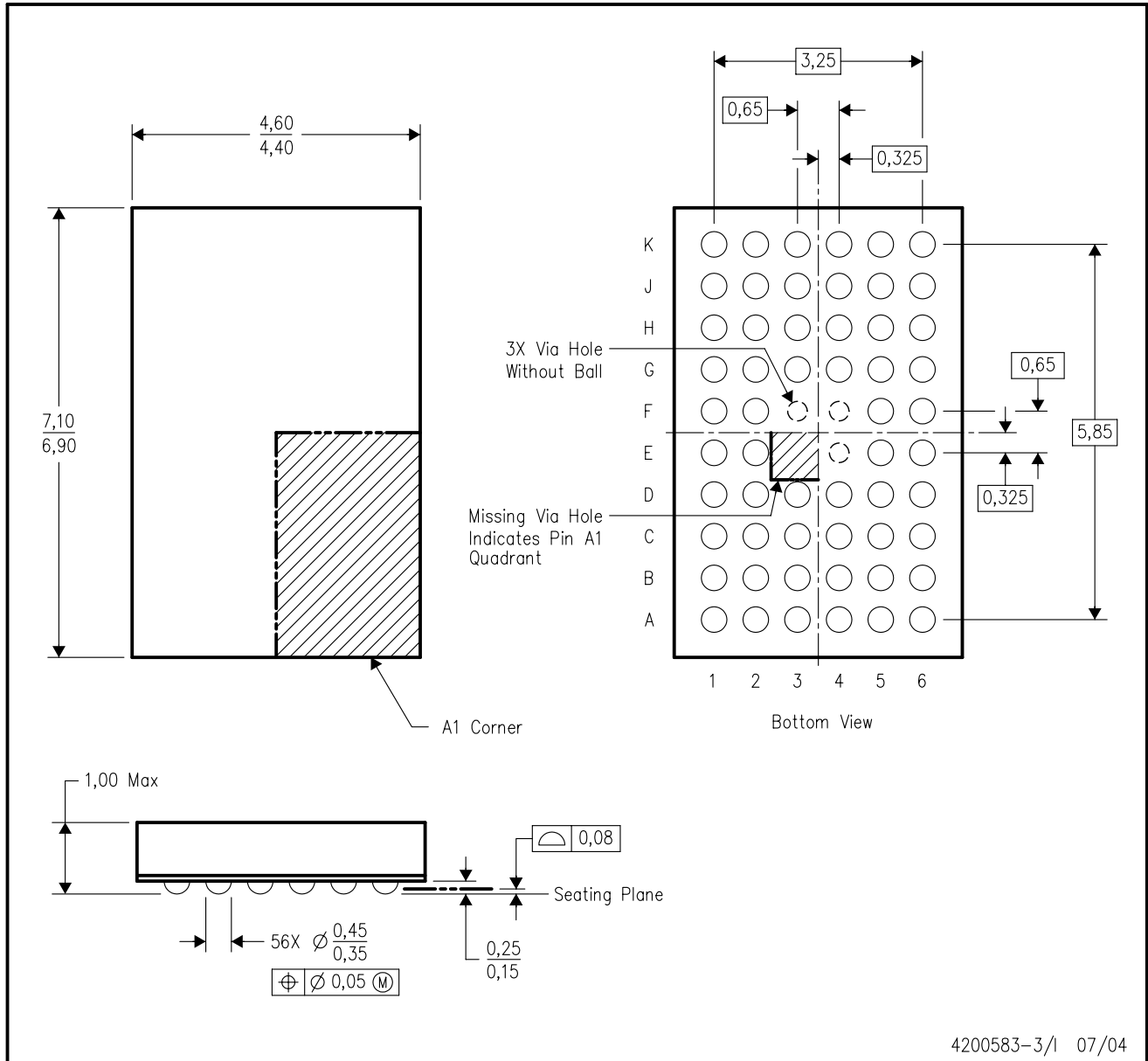
- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194



# MECHANICAL DATA

GQL (R-PBGA-N56)

PLASTIC BALL GRID ARRAY



4200583-3/1 07/04

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MO-225 variation BA.
  - D. This package is tin-lead (SnPb). Refer to the 56 ZQL package (drawing 4204437) for lead-free.

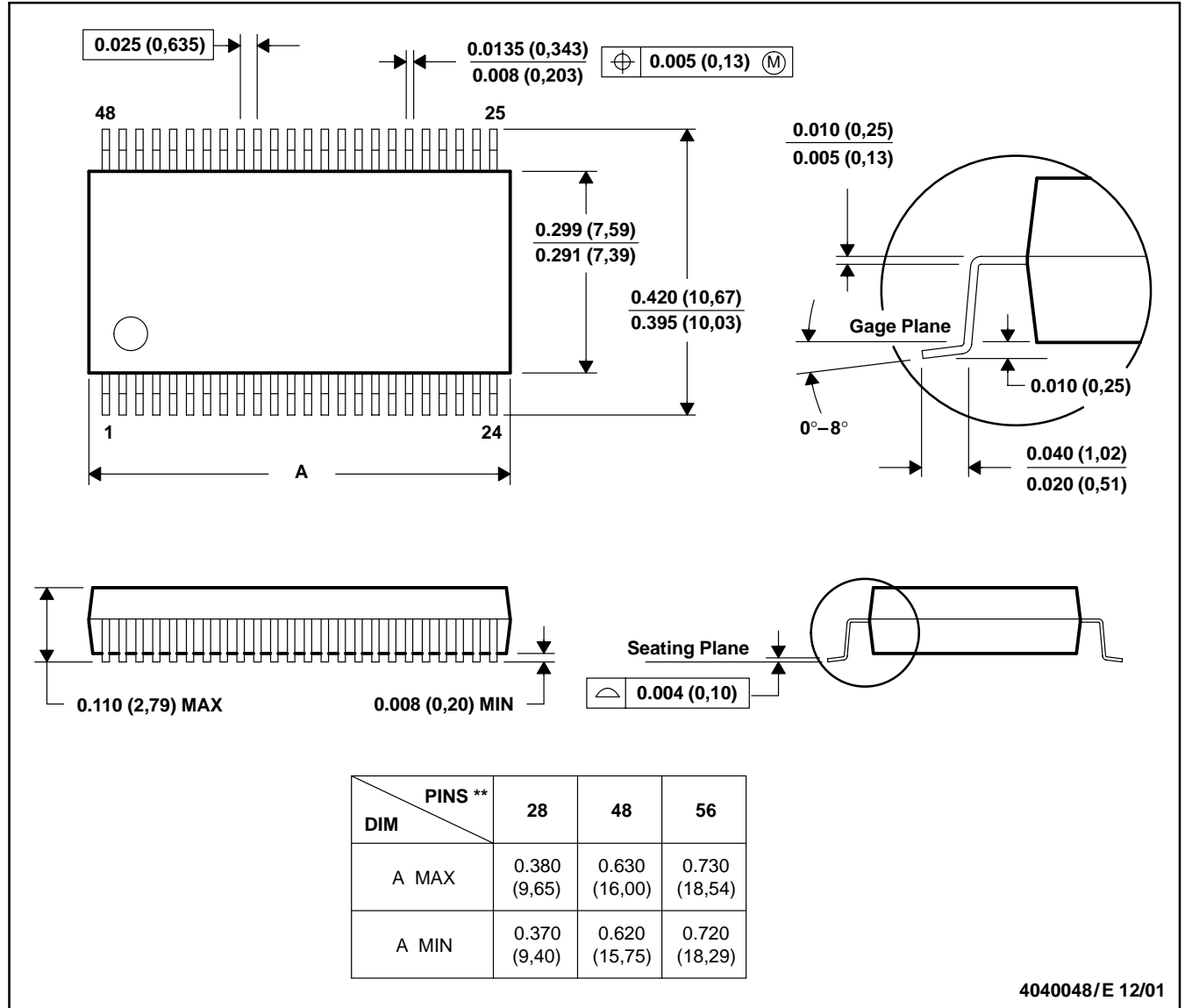
# MECHANICAL DATA

MSS0001C – JANUARY 1995 – REVISED DECEMBER 2001

DL (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).  
 D. Falls within JEDEC MO-118

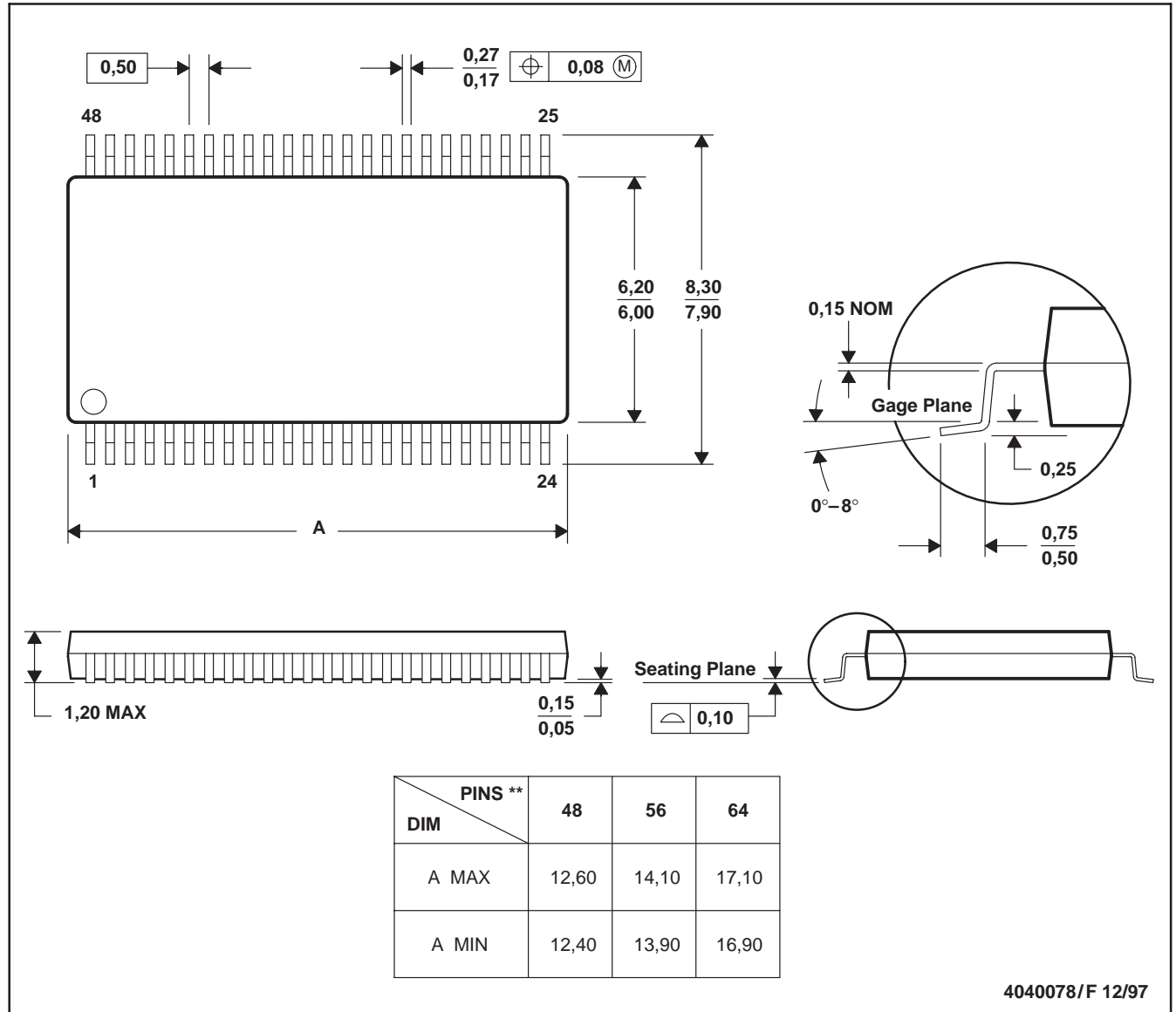
# MECHANICAL DATA

MTSS003D – JANUARY 1995 – REVISED JANUARY 1998

**DGG (R-PDSO-G\*\*)**

**PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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