38B4 Group

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

DESCRIPTION

The 38B4 group is the 8-bit microcomputer based on the 740 family core technology.

The 38B4 group has six 8-bit timers, a 16-bit timer, a fluorescent display automatic display circuit, 12-channel 10-bit A-D converter, a serial I/O with automatic transfer function, which are available for controlling musical instruments and household appliances.

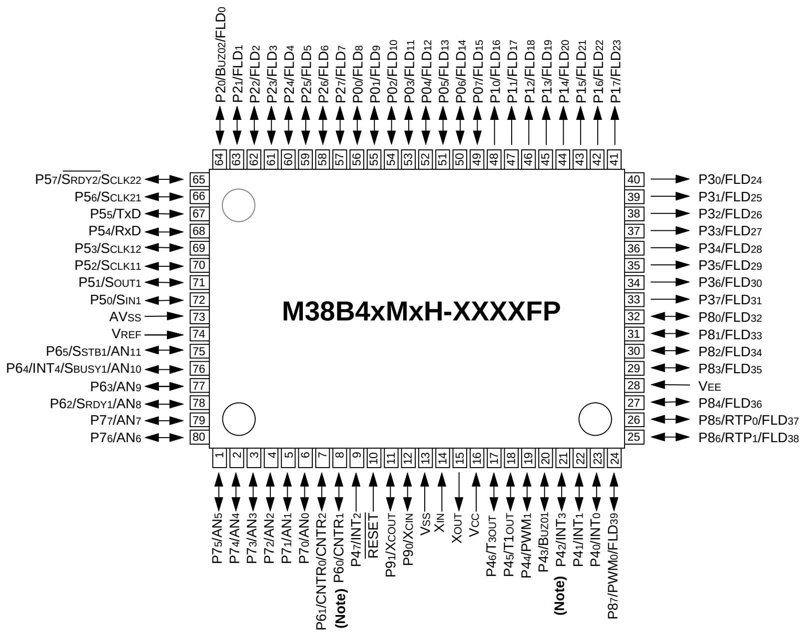
FEATURES

- Basic machine-language instructions 71
- Minimum instruction execution time .... 0.48 μs
  (at 4.2 MHz oscillation frequency)
- Memory size
  ROM .... 48K to 60K bytes
  RAM .... 1024 to 2048 bytes
- Programmable input/output ports 51
- High-breakdown-voltage output ports 36
- Software pull-up resistors (Ports P5, P61 to P65, P7, P84 to P87, P9)
- Interrupts .... 21 sources, 16 vectors
- Timers .... 8-bit × 6, 16-bit × 1
- Serial I/O1 (Clock-synchronized) .... 8-bit × 1
  .... (max. 256-byte automatic transfer function)
- Serial I/O2 (UART or Clock-synchronized) .... 8-bit × 1
- PWM .... 14-bit × 1
  8-bit × 1 (also functions as timer 6)
- A-D converter .... 10-bit × 12 channels
- Fluorescent display function .... Total 40 control pins
- Interrupt interval determination function 1
- Watchdog timer .... 20-bit × 1
- Buzzer output 1
- Clock generating circuit .... Built-in 2 circuits
  (connect to external ceramic resonator or quartz-crystal oscillator)
- Power source voltage
  In high-speed mode .... 4.0 to 5.5 V
  (at 4.2 MHz oscillation frequency)
  2.7 to 5.5 V
  (at 2.0 MHz oscillation frequency)
  In middle-speed mode .... 2.7 to 5.5 V
  (at 4.2 MHz oscillation frequency)
  In low-speed mode .... 2.7 to 5.5 V
  (at 32 kHz oscillation frequency)
- Power dissipation
  In high-speed mode .... 35 mW
  (at 4.2 MHz oscillation frequency)
  In low-speed mode .... 60 μW
  (at 32 kHz oscillation frequency, at 3 V power source voltage)
  In stop mode .... 1 μA
  (at clock stop)
- Operating temperature range .... –20 to 85 °C

APPLICATION

Musical instruments, VCR, household appliances, etc.

PIN CONFIGURATION (TOP VIEW)



Note: In the mask option type P, INT3 and CNTR1 cannot be used.

Package type : 80P6N-A
80-pin plastic-molded QFP

Fig. 1 Pin configuration of M38B4xMxH-XXXXFP

FUNCTIONAL BLOCK

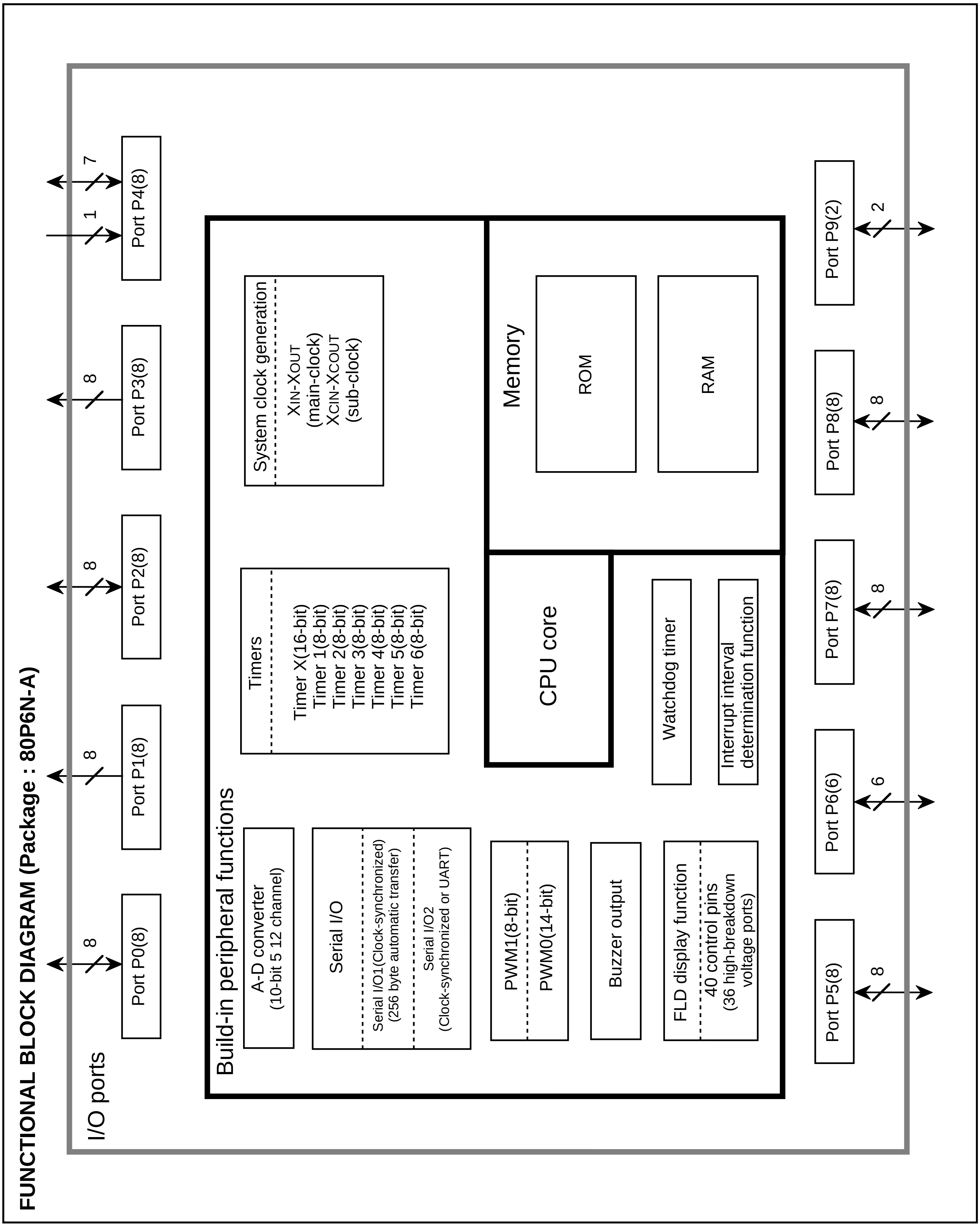


Fig. 2 Functional block diagram

PIN DESCRIPTION

Table 1 Pin description (1)

Pin	Name	Function	Function except a port function
V_{CC}, V_{SS}	Power source	• Apply voltage of 4.0–5.5 V to V_{CC}, and 0 V to V_{SS}.	
V_{EE}	Pull-down power source	• Apply voltage supplied to pull-down resistors of ports P0, P1, and P3.	
V_{REF}	Reference voltage	• Reference voltage input pin for A-D converter.	
AV_{SS}	Analog power source	• Analog power source input pin for A-D converter. • Connect to V_{SS}.	
$\overline{\text{RESET}}$	Reset input	• Reset input pin for active “L”.	
X_{IN}	Clock input	• Input and output pins for the main clock generating circuit. • Feedback resistor is built in between X_{IN} pin and X_{OUT} pin. • Connect a ceramic resonator or quartz-crystal oscillator between the X_{IN} and X_{OUT} pins to set the oscillation frequency. • When an external clock is used, connect the clock source to the X_{IN} pin and leave the X_{OUT} pin open. • The clock is used as the oscillating source of system clock.	
X_{OUT}	Clock output		
$P0_0/FLD_8$–$P0_7/FLD_{15}$	I/O port P0	• 8-bit I/O port. • I/O direction register allows each pin to be individually programmed as either input or output. • At reset, this port is set to input mode. • A pull-down resistor is built in between port P0 and the V_{EE} pin. • CMOS compatible input level. • High-breakdown-voltage P-channel open-drain output structure. • At reset, this port is set to V_{EE} level.	• FLD automatic display pins
$P1_0/FLD_{16}$–$P1_7/FLD_{23}$	Output port P1	• 8-bit output port. • A pull-down resistor is built in between port P1 and the V_{EE} pin. • High-breakdown-voltage P-channel open-drain output structure. • At reset, this port is set to V_{EE} level.	• FLD automatic display pins
$P2_0/B_{UZ02}/FLD_0$–$P2_7/FLD_7$	I/O port P2	• 8-bit I/O port with the same function as port P0. • Low-voltage input level. • High-breakdown-voltage P-channel open-drain output structure.	• FLD automatic display pins • Buzzer output pin ($P2_0$)
$P3_0/FLD_{24}$–$P3_7/FLD_{31}$	Output port P3	• 8-bit output port. • A pull-down resistor is built in between port P3 and the V_{EE} pin. • High-breakdown-voltage P-channel open-drain output structure. • At reset, this port is set to V_{EE} level.	• FLD automatic display pins
$P4_0/INT_0$, $P4_1/INT_1$, $P4_2/INT_3$	I/O port P4	• 7-bit I/O port with the same function as port P0. • CMOS compatible input level • N-channel open-drain output structure.	• Interrupt input pins In the mask option type P, INT_3 cannot be used.
$P4_3/B_{UZ01}$			• Buzzer output pin
$P4_4/PWM_1$			• PWM output pin (Timer output pin)
$P4_5/T_{1OUT}$, $P4_6/T_{3OUT}$			• Timer output pin
$P4_7/INT_2$	Input port P4	• 1-bit input port. • CMOS compatible input level.	• Interrupt input pin

Table 2 Pin description (2)

Pin	Name	Function	Function except a port function
$P5_0/S_{IN1}$, $P5_1/S_{OUT1}$, $P5_2/S_{CLK11}$, $P5_3/S_{CLK12}$	I/O port P5	• 8-bit CMOS I/O port with the same function as port P0. • CMOS compatible input level. • CMOS 3-state output structure.	• Serial I/O1 function pins
$P5_4/R_XD$, $P5_5/T_XD$, $P5_6/S_{CLK21}$, $P5_7/\overline{S_{RDY2}}/S_{CLK22}$			• Serial I/O2 function pins
$P6_0/CNTR_1$	I/O port P6	• 1-bit I/O port with the same function as port P0. • CMOS compatible input level. • N-channel open-drain output structure.	• Timer input pin In the mask option type P, $CNTR_1$ cannot be used.
$P6_1/CNTR_0/CNTR_2$		• 5-bit CMOS I/O port with the same function as port P0. • CMOS compatible input level. • CMOS 3-state output structure.	• Timer I/O pin
$P6_2/S_{RDY1}/AN_8$			• Serial I/O1 function pin • A-D conversion input pin
$P6_3/AN_9$			• A-D conversion input pin • Dimmer signal output pin
$P6_4/INT_4/S_{BUSY1}/AN_{10}$, $P6_5/S_{STB1}/AN_{11}$			• Serial I/O1 function pin • A-D conversion input pin • Interrupt input pin ($P6_4$)
$P7_0/AN_0$–$P7_7/AN_7$	I/O port P7	• 8-bit CMOS I/O port with the same function as port P0. • CMOS compatible input level. • CMOS 3-state output structure.	• A-D conversion input pin
$P8_0/FLD_{32}$–$P8_3/FLD_{35}$	I/O port P8	• 4-bit I/O port with the same function as port P0. • Low-voltage input level. • High-breakdown-voltage P-channel open-drain output structure.	• FLD automatic display pins
$P8_4/FLD_{36}$		• 4-bit CMOS I/O port with the same function as port P0. • Low-voltage input level. • CMOS 3-state output structure	
$P8_5/RTP_0/FLD_{37}$, $P8_6/RTP_1/FLD_{38}$			• FLD automatic display pins • Real time port output
$P8_7/PWM_0/FLD_{39}$			• FLD automatic display pins • 14-bit PWM output
$P9_0/X_{CIN}$, $P9_1/X_{COUT}$	I/O port P9	• 2-bit CMOS I/O port with the same function as port P0. • CMOS compatible input level. • CMOS 3-state output structure.	• I/O pins for sub-clock generating circuit (connect a ceramic resonator or a quarts-crystal oscillator)

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PART NUMBERING

Product M38B4 9 M F H - XXXX FP

Package type
FP : 80P6N-A package

ROM number

High-breakdown voltage pull-down option
Regarding option contents, refer to section "MASK OPTION OF PULL-DOWN RESISTOR".

ROM size
1 : 4096 bytes
2 : 8192 bytes
3 : 12288 bytes
4 : 16384 bytes
5 : 20480 bytes
6 : 24576 bytes
7 : 28672 bytes
8 : 32768 bytes
9 : 36864 bytes
A : 40960 bytes
B : 45056 bytes
C : 49152 bytes
D : 53248 bytes
E : 57344 bytes
F : 61440 bytes

The first 128 bytes and the last 2 bytes of ROM are reserved areas ; they cannot be used for users.

Memory type
M : Mask ROM version
E : EPROM or One Time PROM version

RAM size
0 : 192 bytes
1 : 256 bytes
2 : 384 bytes
3 : 512 bytes
4 : 640 bytes
5 : 768 bytes
6 : 896 bytes
7 : 1024 bytes
8 : 1536 bytes
9 : 2048 bytes

Fig. 3 Part numbering

GROUP EXPANSION

Mitsubishi plans to expand the 38B4 group as follows:

Memory Type

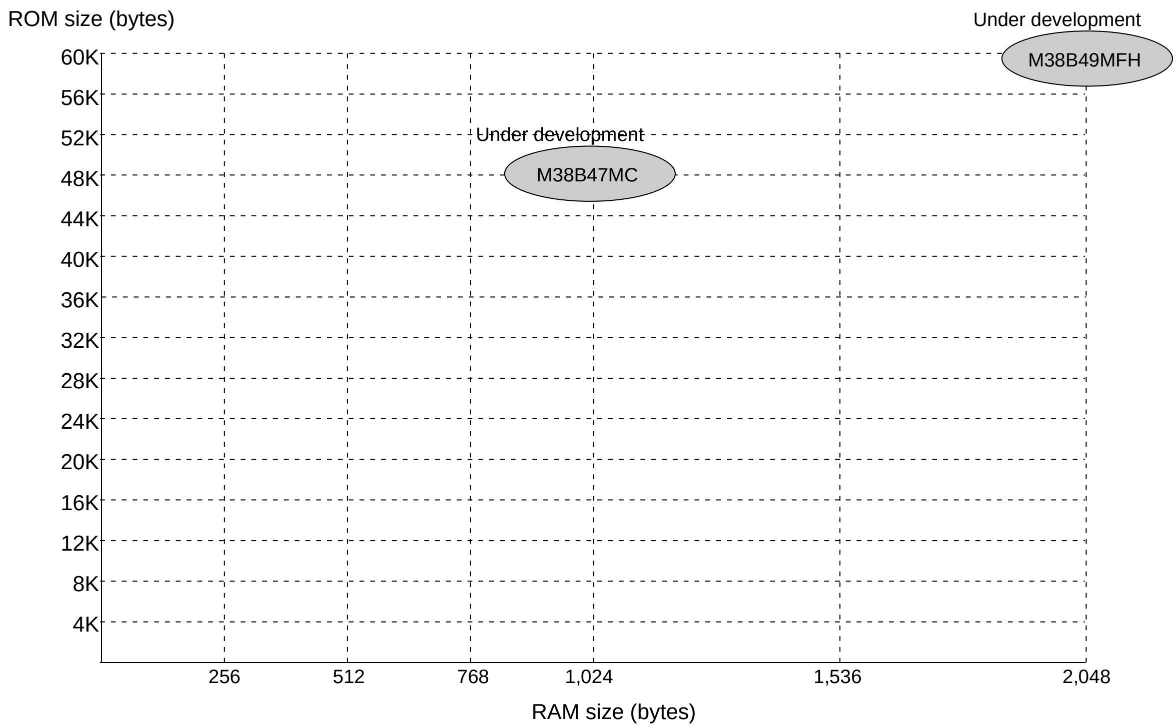
Support for Mask ROM version.

Memory Size

Mask ROM size .... 48K to 60K bytes
RAM size .... 1024 to 2048 bytes

Package

80P6N-A .... 0.8 mm-pitch plastic molded QFP



Note : Products under development or planning : the development schedule and specifications may be revised without notice.

Fig. 4 Memory expansion plan

Currently supported products are listed below.

Table 3 List of supported products **As of Mar. 2000**

Product	ROM size (bytes) ROM size for User ( )	RAM size (bytes)	Package	Remarks
M38B49MFH-XXXXFP	61440 (61310)	2048	80P6N-A	Mask ROM version
M38B47MCH-XXXXFP	49152 (49022)	1024	80P6N-A	Mask ROM version

FUNCTIONAL DESCRIPTION
Central Processing Unit (CPU)

The 38B4 group uses the standard 740 Family instruction set. Refer to the table of 740 Family addressing modes and machine instructions or the 740 Family Software Manual for details on the instruction set.

Machine-resident 740 Family instructions are as follows:
The FST and SLW instructions cannot be used.
The STP, WIT, MUL, and DIV instructions can be used.

[Accumulator (A)]

The accumulator is an 8-bit register. Data operations such as data transfer, etc., are executed mainly through the accumulator.

[Index Register X (X)]

The index register X is an 8-bit register. In the index addressing modes, the value of the OPERAND is added to the contents of register X and specifies the real address.

[Index Register Y (Y)]

The index register Y is an 8-bit register. In partial instruction, the value of the OPERAND is added to the contents of register Y and specifies the real address.

[Stack Pointer (S)]

The stack pointer is an 8-bit register used during subroutine calls and interrupts. This register indicates start address of stored area (stack) for storing registers during subroutine calls and interrupts.

The low-order 8 bits of the stack address are determined by the contents of the stack pointer. The high-order 8 bits of the stack address are determined by the stack page selection bit. If the stack page selection bit is “0” , the high-order 8 bits becomes “00_{16}”. If the stack page selection bit is “1”, the high-order 8 bits becomes “01_{16}”.

The operations of pushing register contents onto the stack and popping them from the stack are shown in Figure 6.

Store registers other than those described in Figure 6 with program when the user needs them during interrupts or subroutine calls (see Table 4).

[Program Counter (PC)]

The program counter is a 16-bit counter consisting of two 8-bit registers PC_H and PC_L. It is used to indicate the address of the next instruction to be executed.

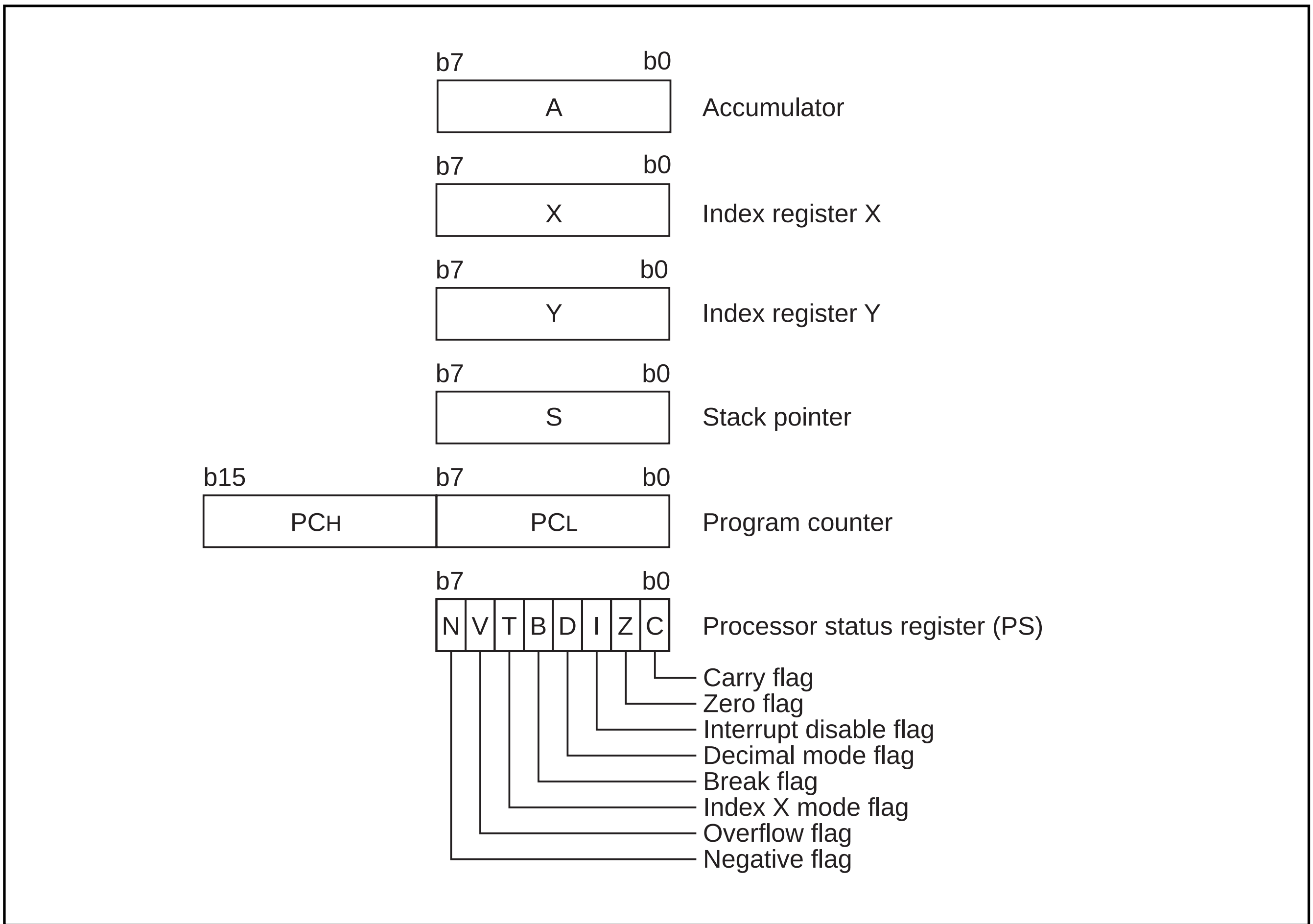


Fig. 5 740 Family CPU register structure

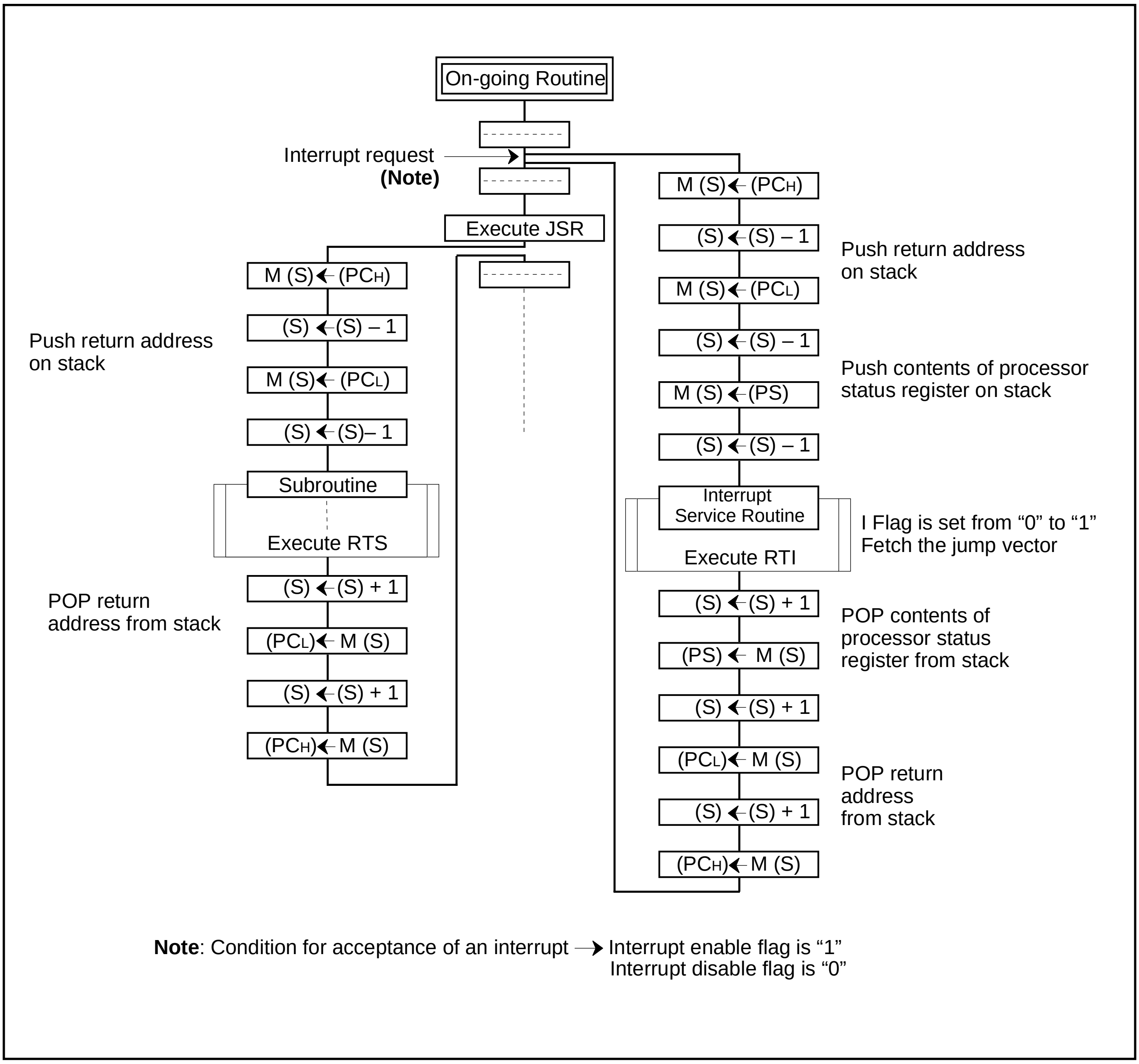


Fig. 6 Register push and pop at interrupt generation and subroutine call

Table 4 Push and pop instructions of accumulator or processor status register

	Push instruction to stack	Pop instruction from stack
Accumulator	PHA	PLA
Processor status register	PHP	PLP

[Processor Status Register (PS)]

The processor status register is an 8-bit register consisting of 5 flags which indicate the status of the processor after an arithmetic operation and 3 flags which decide MCU operation. Branch operations can be performed by testing the Carry (C) flag , Zero (Z) flag, Overflow (V) flag, or the Negative (N) flag. In decimal mode, the Z, V, N flags are not valid.

•Bit 0: Carry flag (C)
The C flag contains a carry or borrow generated by the arithmetic logic unit (ALU) immediately after an arithmetic operation. It can also be changed by a shift or rotate instruction.

•Bit 1: Zero flag (Z)
The Z flag is set if the result of an immediate arithmetic operation or a data transfer is “0”, and cleared if the result is anything other than “0”.

•Bit 2: Interrupt disable flag (I)
The I flag disables all interrupts except for the interrupt generated by the BRK instruction.
Interrupts are disabled when the I flag is “1”.

•Bit 3: Decimal mode flag (D)
The D flag determines whether additions and subtractions are executed in binary or decimal. Binary arithmetic is executed when this flag is “0”; decimal arithmetic is executed when it is “1”. Decimal correction is automatic in decimal mode. Only the ADC and SBC instructions can be used for decimal arithmetic.

•Bit 4: Break flag (B)
The B flag is used to indicate that the current interrupt was generated by the BRK instruction. The BRK flag in the processor status register is always “0”. When the BRK instruction is used to generate an interrupt, the processor status register is pushed onto the stack with the break flag set to “1”.

•Bit 5: Index X mode flag (T)
When the T flag is “0”, arithmetic operations are performed between accumulator and memory. When the T flag is “1”, direct arithmetic operations and direct data transfers are enabled between memory locations.

•Bit 6: Overflow flag (V)
The V flag is used during the addition or subtraction of one byte of signed data. It is set if the result exceeds +127 to -128. When the BIT instruction is executed, bit 6 of the memory location operated on by the BIT instruction is stored in the overflow flag.

•Bit 7: Negative flag (N)
The N flag is set if the result of an arithmetic operation or data transfer is negative. When the BIT instruction is executed, bit 7 of the memory location operated on by the BIT instruction is stored in the negative flag.

Table 5 Set and clear instructions of each bit of processor status register

	C flag	Z flag	I flag	D flag	B flag	T flag	V flag	N flag
Set instruction	SEC	–	SEI	SED	–	SET	–	–
Clear instruction	CLC	–	CLI	CLD	–	CLT	CLV	–

[CPU Mode Register (CPUM)] $003B_{16}$

The CPU mode register contains the stack page selection bit and the internal system clock selection bit etc.
The CPU mode register is allocated at address $003B_{16}$.

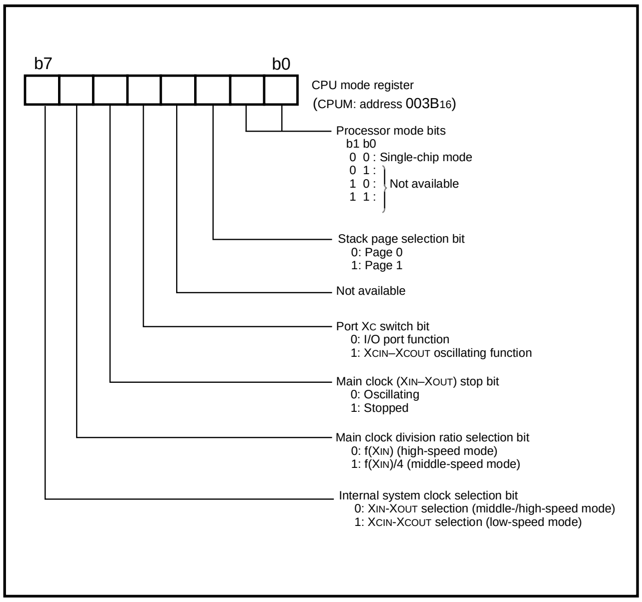


Fig. 7 Structure of CPU mode register

MEMORY

Special Function Register (SFR) Area

The special function register (SFR) area in the zero page contains control registers such as I/O ports and timers.

RAM

RAM is used for data storage and for stack area of subroutine calls and interrupts.

ROM

The first 128 bytes and the last 2 bytes of ROM are reserved for device testing, and the other areas are user areas for storing programs.

Interrupt Vector Area

The interrupt vector area contains reset and interrupt vectors.

Zero Page

The 256 bytes from addresses 0000_{16} to $00FF_{16}$ are called the zero page area. The internal RAM and the special function registers (SFR) are allocated to this area.

The zero page addressing mode can be used to specify memory and register addresses in the zero page area. Access to this area with only 2 bytes is possible in the zero page addressing mode.

Special Page

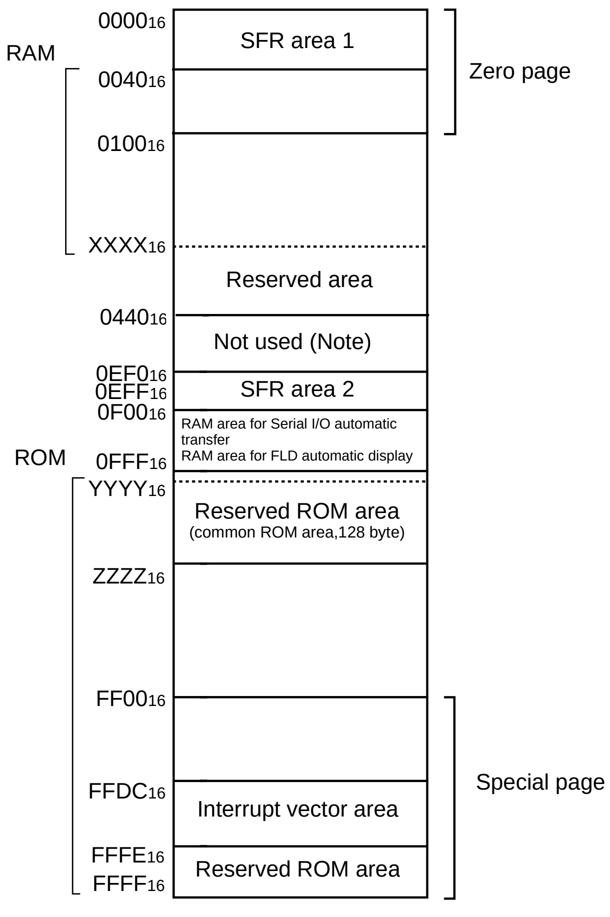
The 256 bytes from addresses $FF00_{16}$ to $FFFF_{16}$ are called the special page area. The special page addressing mode can be used to specify memory addresses in the special page area. Access to this area with only 2 bytes is possible in the special page addressing mode.

RAM area

RAM size (byte)	Address $XXXX_{16}$
192	$00FF_{16}$
256	$013F_{16}$
384	$01BF_{16}$
512	$023F_{16}$
640	$02BF_{16}$
768	$033F_{16}$
896	$03BF_{16}$
1024	$043F_{16}$
1536	$063F_{16}$
2048	$083F_{16}$

ROM area

ROM size (byte)	Address $YYYY_{16}$	Address $ZZZZ_{16}$
4096	$F000_{16}$	$F080_{16}$
8192	$E000_{16}$	$E080_{16}$
12288	$D000_{16}$	$D080_{16}$
16384	$C000_{16}$	$C080_{16}$
20480	$B000_{16}$	$B080_{16}$
24576	$A000_{16}$	$A080_{16}$
28672	9000_{16}	9080_{16}
32768	8000_{16}	8080_{16}
36864	7000_{16}	7080_{16}
40960	6000_{16}	6080_{16}
45056	5000_{16}	5080_{16}
49152	4000_{16}	4080_{16}
53248	3000_{16}	3080_{16}
57344	2000_{16}	2080_{16}
61440	1000_{16}	1080_{16}



Note: When 1024 bytes or more are used as RAM area, this area can be used.

Fig. 8 Memory map diagram

Address	Register	Address	Register
0000_{16}	Port P0 (P0)	0020_{16}	Timer 1 (T1)
0001_{16}	Port P0 direction register (P0D)	0021_{16}	Timer 2 (T2)
0002_{16}	Port P1 (P1)	0022_{16}	Timer 3 (T3)
0003_{16}		0023_{16}	Timer 4 (T4)
0004_{16}	Port P2 (P2)	0024_{16}	Timer 5 (T5)
0005_{16}	Port P2 direction register (P2D)	0025_{16}	Timer 6 (T6)
0006_{16}	Port P3 (P3)	0026_{16}	PWM control register (PWMCON)
0007_{16}		0027_{16}	Timer 6 PWM register (T6PWM)
0008_{16}	Port P4 (P4)	0028_{16}	Timer 12 mode register (T12M)
0009_{16}	Port P4 direction register (P4D)	0029_{16}	Timer 34 mode register (T34M)
$000A_{16}$	Port P5 (P5)	$002A_{16}$	Timer 56 mode register (T56M)
$000B_{16}$	Port P5 direction register (P5D)	$002B_{16}$	Watchdog timer control register (WDTCON)
$000C_{16}$	Port P6 (P6)	$002C_{16}$	Timer X (low-order) (TXL)
$000D_{16}$	Port P6 direction register (P6D)	$002D_{16}$	Timer X (high-order) (TXH)
$000E_{16}$	Port P7 (P7)	$002E_{16}$	Timer X mode register 1 (TXM1)
$000F_{16}$	Port P7 direction register (P7D)	$002F_{16}$	Timer X mode register 2 (TXM2)
0010_{16}	Port P8 (P8)	0030_{16}	Interrupt interval determination register (IID)
0011_{16}	Port P8 direction register (P8D)	0031_{16}	Interrupt interval determination control register (IIDCON)
0012_{16}	Port P9 (P9)	0032_{16}	A-D control register (ADCON)
0013_{16}	Port P9 direction register (P9D)	0033_{16}	A-D conversion register (low-order) (ADL)
0014_{16}	PWM register (high-order) (PWMH)	0034_{16}	A-D conversion register (high-order) (ADH)
0015_{16}	PWM register (low-order) (PWM L)	0035_{16}	
0016_{16}	Baud rate generator (BRG)	0036_{16}	
0017_{16}	UART control register (UARTCON)	0037_{16}	
0018_{16}	Serial I/O1 automatic transfer data pointer (SIO1DP)	0038_{16}	
0019_{16}	Serial I/O1 control register 1 (SIO1CON1)	0039_{16}	Interrupt source switch register (IFR)
$001A_{16}$	Serial I/O1 control register 2 (SIO1CON2)	$003A_{16}$	Interrupt edge selection register (INTEDGE)
$001B_{16}$	Serial I/O1 register/Transfer counter (SIO1)	$003B_{16}$	CPU mode register (CPUM)
$001C_{16}$	Serial I/O1 control register 3 (SIO1CON3)	$003C_{16}$	Interrupt request register 1(IREQ1)
$001D_{16}$	Serial I/O2 control register (SIO2CON)	$003D_{16}$	Interrupt request register 2(IREQ2)
$001E_{16}$	Serial I/O2 status register (SIO2STS)	$003E_{16}$	Interrupt control register 1(ICON1)
$001F_{16}$	Serial I/O2 transmit/receive buffer register (TB/RB)	$003F_{16}$	Interrupt control register 2(ICON2)

Address	Register	Address	Register
$0EF0_{16}$	Pull-up control register 1 (PULL1)	$0EF8_{16}$	FLD data pointer (FLDDP)
$0EF1_{16}$	Pull-up control register 2 (PULL2)	$0EF9_{16}$	Port P0FLD/port switch register (P0FPR)
$0EF2_{16}$		$0EFA_{16}$	Port P2FLD/port switch register (P2FPR)
$0EF3_{16}$		$0EFB_{16}$	Port P8FLD/port switch register (P8FPR)
$0EF4_{16}$	FLDC mode register (FLDM)	$0EFC_{16}$	Port P8FLD output control register (P8FLDCON)
$0EF5_{16}$	Tdisp time set register (TDISP)	$0EFD_{16}$	Buzzer output control register (BUZCON)
$0EF6_{16}$	Toff1 time set register (TOFF1)	$0EFE_{16}$	
$0EF7_{16}$	Toff2 time set register (TOFF2)	$0EFF_{16}$	

Fig. 9 Memory map of special function register (SFR)

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I/O PORTS
[Direction Registers] PiD

The 38B4 group has 51 programmable I/O pins arranged in eight individual I/O ports (P0, P2, $P4_0$–$P4_6$, and P5–P9). The I/O ports have direction registers which determine the input/output direction of each individual pin. Each bit in a direction register corresponds to one pin, and each pin can be set to be input port or output port. When “0” is written to the bit corresponding to a pin, that pin becomes an input pin. When “1” is written to that pin, that pin becomes an output pin. If data is read from a pin set to output, the value of the port output latch is read, not the value of the pin itself. Pins set to input (the bit corresponding to that pin must be set to “0”) are floating and the value of that pin can be read. If a pin set to input is written to, only the port output latch is written to and the pin remains floating.

[High-Breakdown-Voltage Output Ports]

The 38B4 group has 5 ports with high-breakdown-voltage pins (ports P0–P3 and $P8_0$–$P8_3$). The high-breakdown-voltage ports have P-channel open-drain output with Vcc- 45 V of breakdown voltage. Each pin in ports P0, P1, and P3 has an internal pull-down resistor connected to V_{EE}. At reset, the P-channel output transistor of each port latch is turned off, so that it goes to V_{EE} level (“L”) by the pull-down resistor.
Writing “1” (weak drivability) to bit 7 of the FLDC mode register (address $0EF4_{16}$) shows the rising transition of the output transistors for reducing transient noise. At reset, bit 7 of the FLDC mode register is set to “0” (strong drivability).

[Pull-up Control Register] PULL

Ports P5, $P6_1$–$P6_5$, P7, $P8_4$–$P8_7$ and P9 have built-in programmable pull-up resistors. The pull-up resistors are valid only in the case that the each control bit is set to “1” and the corresponding port direction registers are set to input mode.

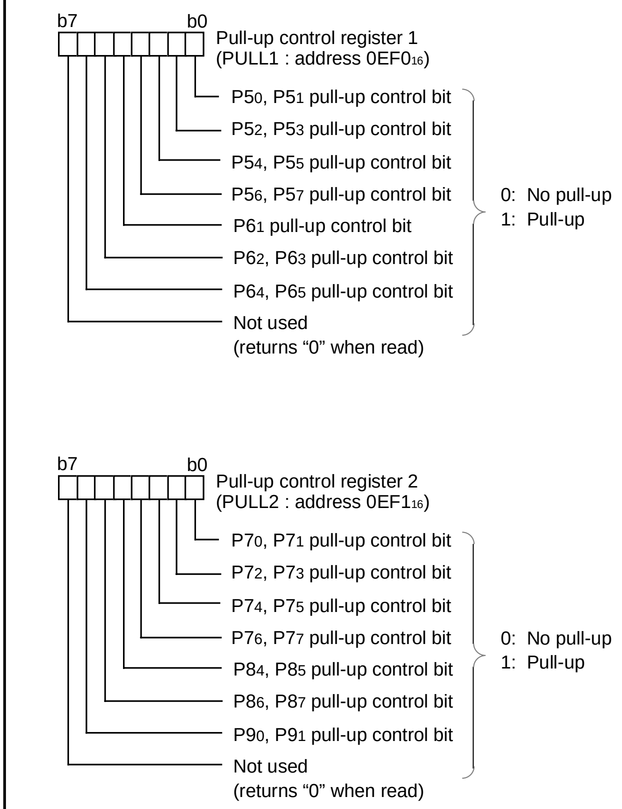


Fig. 10 Structure of pull-up control registers (PULL1 and PULL2)

Table 6 List of I/O port functions (1)

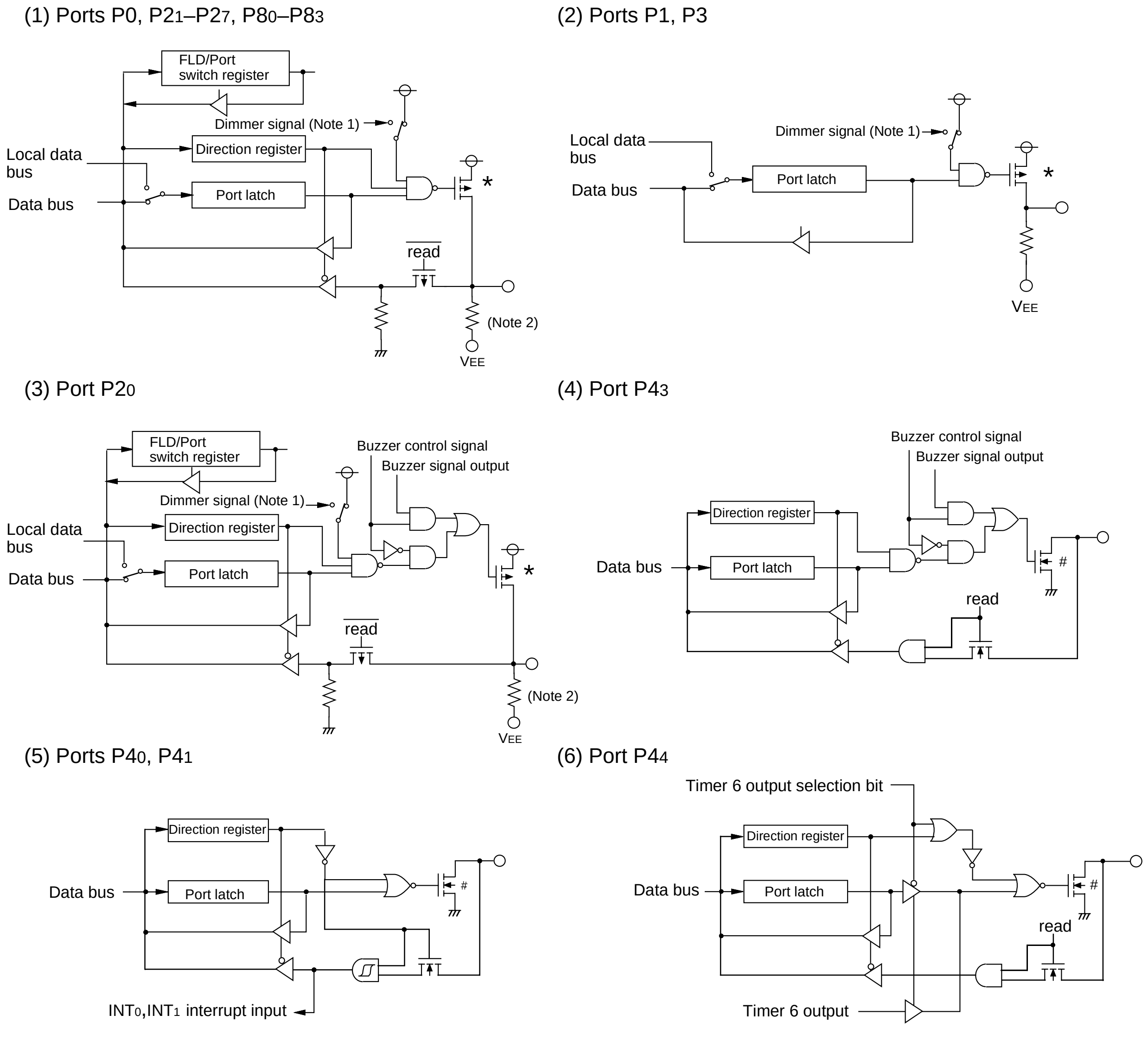
zPin	Name	Input/Output	I/O Format	Non-Port Function	Related SFRs	Ref.No.
$P0_0$/FLD_8– $P0_7$/FLD_{15}	Port P0	Input/output, individual bits	CMOS compatible input level High-breakdown voltage P-channel open-drain output with pull-down resistor	FLD automatic display function	FLDC mode register Port P0FLD/port switch register	(1)
$P1_0$/FLD_{16}– $P1_7$/FLD_{23}	Port P1	Output	High-breakdown voltage P-channel open-drain output with pull-down resistor		FLDC mode register	(2)
$P2_0$/BUZ_{02}/ FLD_0	Port P2	Input/output, individual bits	Low-voltage input level High-breakdown voltage P-channel open-drain output	Buzzer output ($P2_0$) FLD automatic display function	FLDC mode register Port P2FLD/port switch register Buzzer output control register	(3)
$P2_1$/FLD_1– $P2_7$/FLD_7				FLD automatic display function		(1)
$P3_0$/FLD_{24}– $P3_7$/FLD_{31}	Port P3	Output	High-breakdown voltage P-channel open-drain output with pull-down resistor		FLDC mode register	(2)
$P4_0$/INT_0, $P4_1$/INT_1	Port P4	Input/output, individual bits	CMOS compatible input level N-channel open-drain output	External interrupt input In the mask option type P, INT_3 cannot be used.	Interrupt edge selection register	(5)
$P4_2$/INT_3						(7-1) (7-2)
$P4_3$/BUZ_{01}				Buzzer output	Buzzer output control register	(4)
$P4_4$/PWM_1				PWM output	Timer 56 mode register	(6)
$P4_5$/T_{1OUT}				Timer output	Timer 12 mode register	(8-1)
$P4_6$/T_{3OUT}				Timer output	Timer 34 mode register	(8-2)
$P4_7$/INT_2		Input	CMOS compatible input level	External interrput input	Interrupt edge selection register Interrupt interval determination control register	(9)
$P5_0$/S_{IN1}	Port P5	Input/output, individual bits	CMOS compatible input level CMOS 3-state output	Serial I/O1 function I/O	Serial I/O1 control register 1, 2	(10)
$P5_1$/S_{OUT1}, $P5_2$/S_{CLK11}, $P5_3$/S_{CLK12}						(11)
$P5_4$/R_XD				Serial I/O2 function I/O	Serial I/O2 control register UART control register	(10)
$P5_5$/T_XD, $P5_6$/S_{CLK21}						(11)
$P5_7$/$\overline{S_{RDY2}}$/ S_{CLK22}						(12)
$P6_0$/$CNTR_1$	Port P6		CMOS compatible input level N-channel open-drain output	External count input In the mask option type P, $CNTR_1$ cannot be used.	Interrupt edge selection register	(7-1) (7-2)
$P6_1$/$CNTR_0$/ $CNTR_2$			CMOS compatible input level CMOS 3-state output			(13)
$P6_2$/S_{RDY1}/ AN_8				Serial I/O1 function I/O A-D conversion input	Serial I/O1 control register 1, 2 A-D control register	(14)
$P6_3$/AN_9				A-D conversion input Dimmer signal output	A-D control register P8FLD output control bit	(15)
$P6_4$/INT_4/ S_{BUSY1}/AN_{10}				Serial I/O1 function I/O A-D conversion input External interrupt input	Serial I/O1 control register 1, 2 A-D control register Interrupt edge selection register	(16)
$P6_5$/S_{STB1}/ AN_{11}				Serial I/O1 function I/O A-D conversion input	Serial I/O1 control register 1, 2 A-D control register	(17)
$P7_0$/AN_0– $P7_7$/AN_7	Port P7			A-D conversion input	A-D control register	(15)

Table 7 List of I/O port functions (2)

Pin	Name	Input/Output	I/O Format	Non-Port Function	Related SFRs	Ref.No.
$P8_0$/FLD_{32}–$P8_3$/FLD_{35}	Port P8	Input/output, individual bits	Low-voltage input level High-breakdown voltage P-channel open-drain output	FLD automatic display function	FLDC mode register Port P8FLD/port switch register	(1)
$P8_4$/FLD_{36}			Low-voltage input level CMOS 3-state output			(18)
$P8_5$/RTP_0/FLD_{37}, $P8_6$/RTP_1/FLD_{38}				FLD automatic display function Real time port output	FLDC mode register Port P8FLD/port switch register Timer X mode register 2	(19)
$P8_7$/PWM_0/FLD_{39}				FLD automatic display function PWM output	FLDC mode register Port P8FLD/port switch register PWM control register	(20)
$P9_0$/X_{CIN}	Port P9		CMOS compatible input level CMOS 3-state output	Sub-clock generating circuit I/O	CPU mode register	(21)
$P9_1$/X_{COUT}						(22)

Notes 1 : Make sure that the input level at each pin is either 0 V or Vcc during execution of the STP instruction.
When an input level is at an intermediate potential, a current will flow from Vcc to Vss through the input-stage gate.

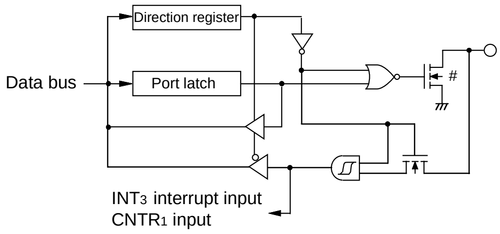
2 : How to use double-function ports as function I/O ports, refer to the applicable sections.



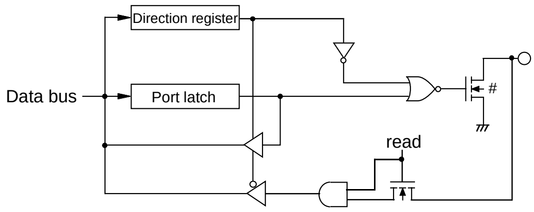
* High-breakdown-voltage P-channel transistor
\# Middle-breakdown-voltage N-channel transistor
Notes 1: The dimmer signal sets the Toff timing.
2: A pull-down resistor is not built in to ports P2 and P8.

Fig. 11 Port block diagram (1)

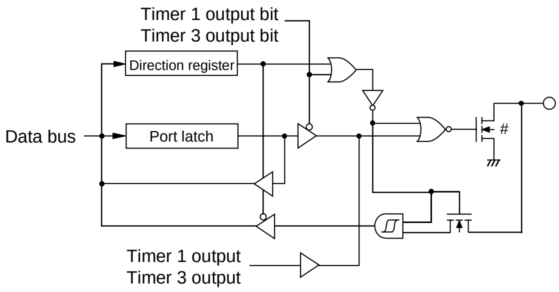
(7-1) Ports $P4_2$, $P6_0$



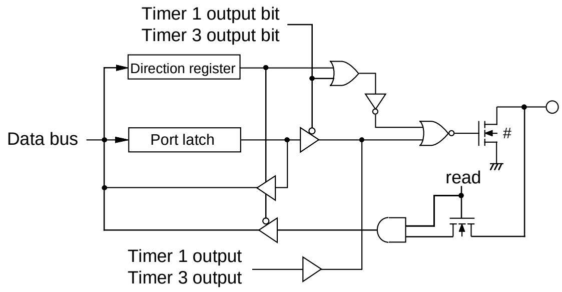
(7-2) Ports $P4_2$, $P6_0$ (mask option type P)



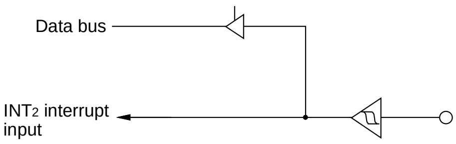
(8-1) Ports $P4_5$, $P4_6$



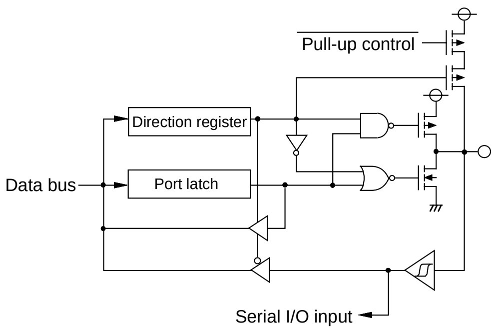
(8-2) Ports $P4_5$, $P4_6$ (mask option type P)



(9) Port $P4_7$



(10) Ports $P5_0$, $P5_4$



Middle-breakdown-voltage N-channel transistor

Fig. 12 Port block diagram (2)

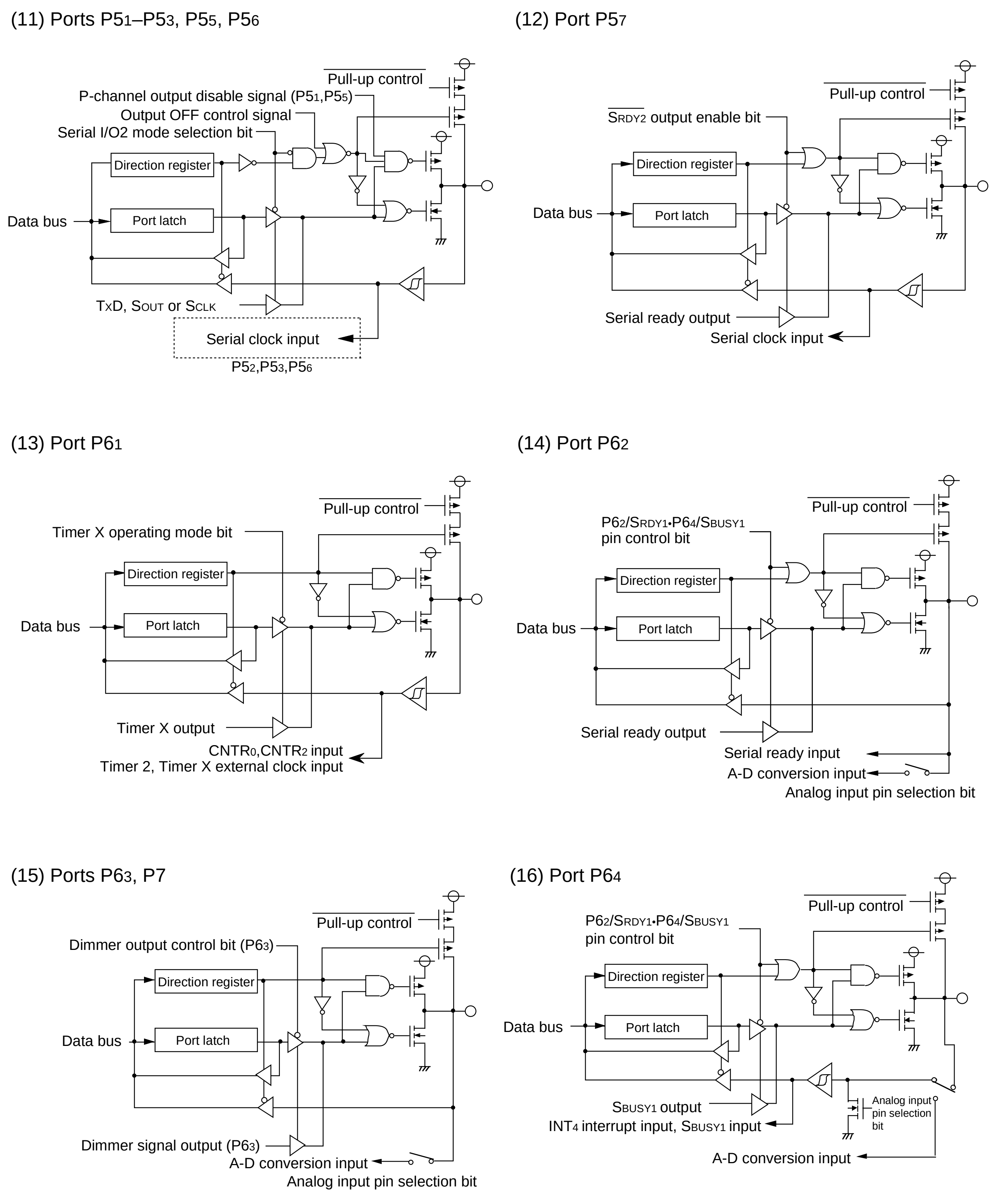


Fig. 13 Port block diagram (3)

MITSUBISHI ELECTRIC

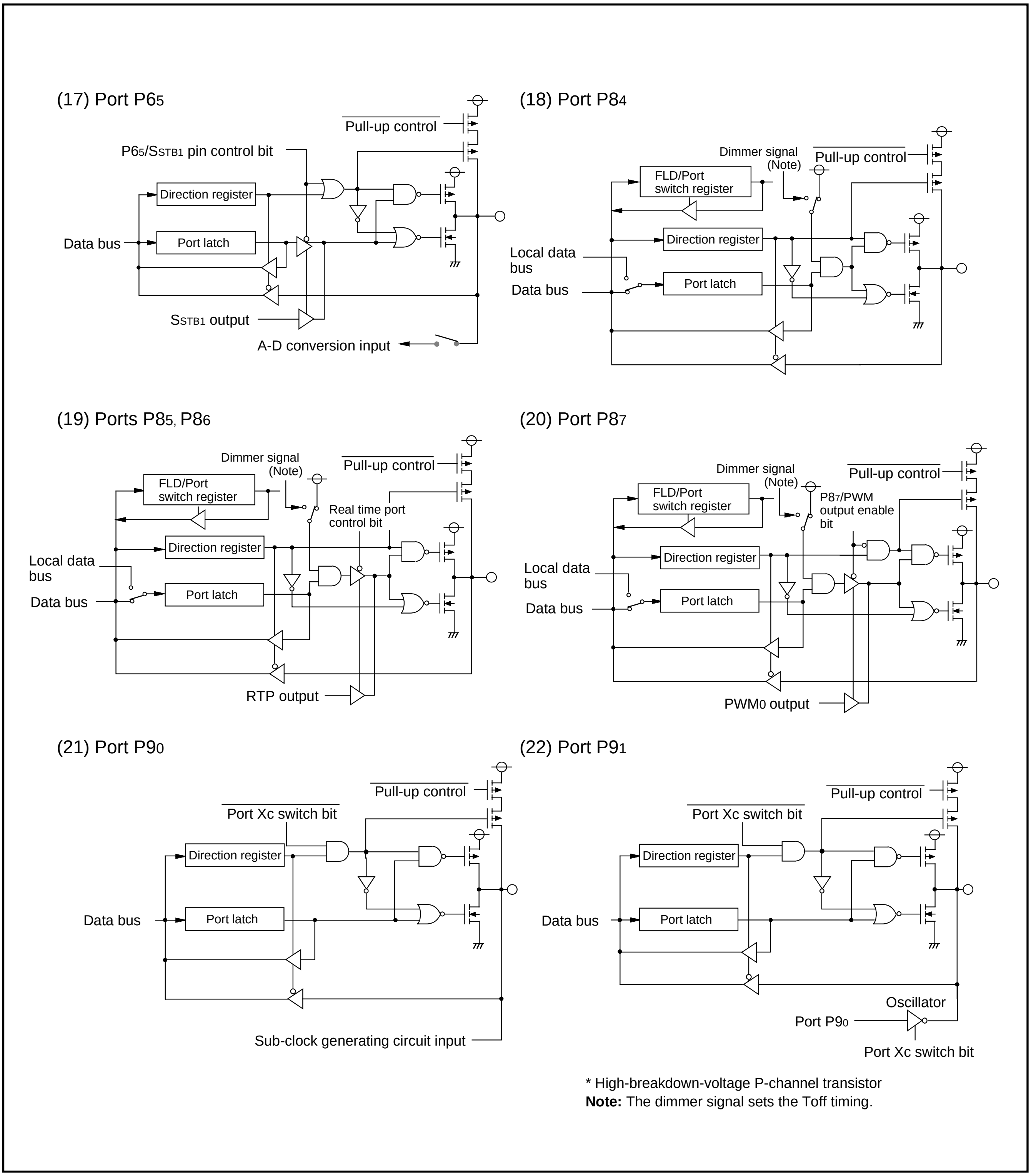


Fig. 14 Port block diagram (4)

INTERRUPTS

Interrupts occur by twenty one sources: five external, fifteen internal, and one software.

Interrupt Control

Each interrupt except the BRK instruction interrupt have both an interrupt request bit and an interrupt enable bit, and is controlled by the interrupt disable flag. An interrupt occurs if the corresponding interrupt request and enable bits are “1” and the interrupt disable flag is “0”. Interrupt enable bits can be set or cleared by software. Interrupt request bits can be cleared by software, but cannot be set by software. The BRK instruction interrupt and reset cannot be disabled with any flag or bit. The I flag disables all interrupts except the BRK instruction interrupt and reset. If several interrupts requests occurs at the same time the interrupt with highest priority is accepted first.

Interrupt Operation

Upon acceptance of an interrupt the following operations are automatically performed:

1. The contents of the program counter and processor status register are automatically pushed onto the stack.
2. The interrupt disable flag is set and the corresponding interrupt request bit is cleared.
3. The interrupt jump destination address is read from the vector table into the program counter.

■Notes on Use

When the active edge of an external interrupt (INT_0–INT_4) is set or when switching interrupt sources in the same vector address, the corresponding interrupt request bit may also be set. Therefore, please take following sequence:

(1) Disable the external interrupt which is selected.
(2) Change the active edge in interrupt edge selection register
(3) Clear the set interrupt request bit to “0”.
(4) Enable the external interrupt which is selected.

Table 8 Interrupt vector addresses and priority

Interrupt Source	Priority	Vector Addresses (Note 1) High	Vector Addresses (Note 1) Low	Interrupt Request Generating Conditions	Remarks
Reset **(Note 2)**	1	$FFFD_{16}$	$FFFC_{16}$	At reset	Non-maskable
INT_0	2	$FFFB_{16}$	$FFFA_{16}$	At detection of either rising or falling edge of INT_0 input	External interrupt (active edge selectable)
INT_1	3	$FFF9_{16}$	$FFF8_{16}$	At detection of either rising or falling edge of INT_1 input	External interrupt (active edge selectable)
INT_2	4	$FFF7_{16}$	$FFF6_{16}$	At detection of either rising or falling edge of INT_2 input	External interrupt (active edge selectable)
Remote control/ counter overflow				At 8-bit counter overflow	Valid when interrupt interval determination is operating
Serial I/O1	5	$FFF5_{16}$	$FFF4_{16}$	At completion of data transfer	Valid when serial I/O ordinary mode is selected
Serial I/O auto-matic transfer				At completion of the last data transfer	Valid when serial I/O automatic transfer mode is selected
Timer X	6	$FFF3_{16}$	$FFF2_{16}$	At timer X underflow	
Timer 1	7	$FFF1_{16}$	$FFF0_{16}$	At timer 1 underflow	
Timer 2	8	$FFEF_{16}$	$FFEE_{16}$	At timer 2 underflow	STP release timer underflow
Timer 3	9	$FFED_{16}$	$FFEC_{16}$	At timer 3 underflow	
Timer 4	10	$FFEB_{16}$	$FFEA_{16}$	At timer 4 underflow	**(Note 3)**
Timer 5	11	$FFE9_{16}$	$FFE8_{16}$	At timer 5 underflow	
Timer 6	12	$FFE7_{16}$	$FFE6_{16}$	At timer 6 underflow	
Serial I/O2 receive	13	$FFE5_{16}$	$FFE4_{16}$	At completion of serial I/O2 data receive	
INT_3	14	$FFE3_{16}$	$FFE2_{16}$	At detection of either rising or falling edge of INT_3 input	External interrupt **(Note 4)** (active edge selectable)
Serial I/O2 transmit				At completion of serial I/O2 data transmit	
INT_4	15	$FFE1_{16}$	$FFE0_{16}$	At detection of either rising or falling edge of INT_4 input	External interrupt (active edge selectable) Valid when INT_4 interrupt is selected
A-D conversion				At completion of A-D conversion	Valid when A-D conversion is selected
FLD blanking	16	$FFDF_{16}$	$FFDE_{16}$	At falling edge of the last timing immediately before blanking period starts	Valid when FLD blanking interrupt is selected
FLD digit				At rising edge of digit (each timing)	Valid when FLD digit interrupt is selected
BRK instruction	17	$FFDD_{16}$	$FFDC_{16}$	At BRK instruction execution	Non-maskable software interrupt

Notes 1 : Vector addresses contain interrupt jump destination addresses.
2 : Reset function in the same way as an interrupt with the highest priority.
3 : In the mask option type P, timer 4 interrupt whose count source is $CNTR_1$ input cannot be used.
4 : In the mask option type P, INT_3 interrupt cannot be used.

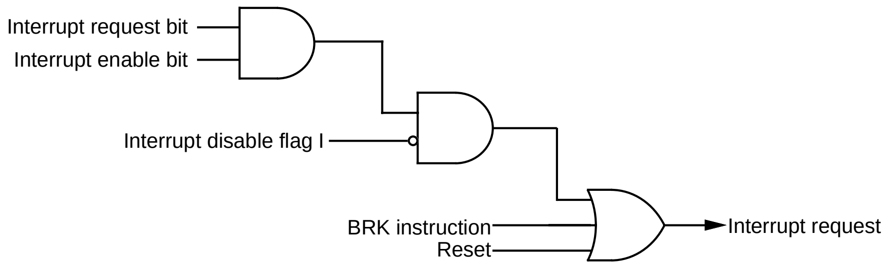
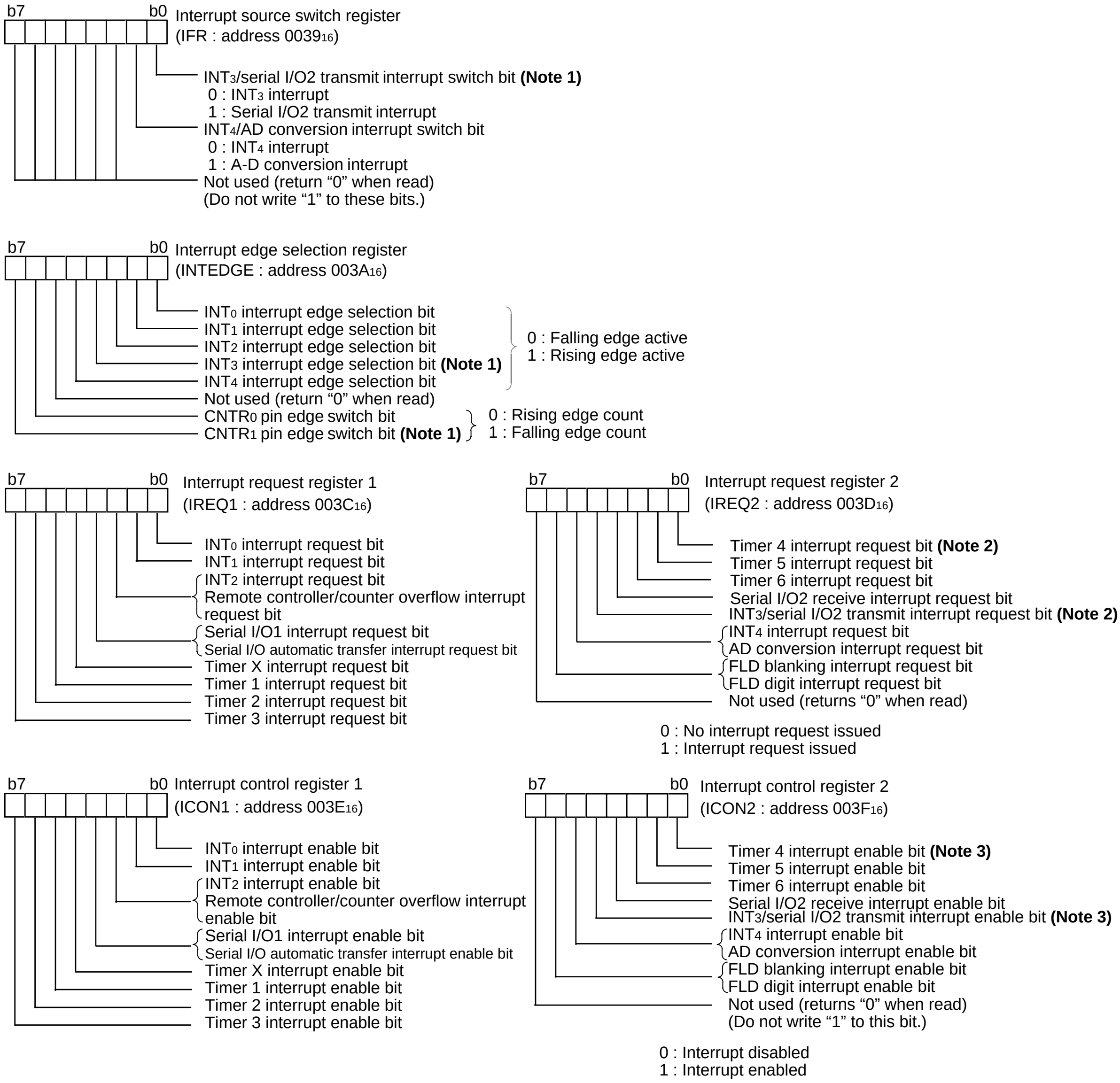


Fig. 15 Interrupt control



Notes 1: In the mask option type P, these bits are not available because CNTR$_1$ function and INT$_3$ function cannot be used.
2: In the mask option type P, if timer 4 interrupt whose count source is CNTR$_1$ input and INT$_3$ interrupt are selected, these bits do not become "1".
3: In the mask option type P, timer 4 interrupt whose count source is CNTR$_1$ input and INT$_3$ interrupt are not available.

Fig. 16 Structure of interrupt related registers

TIMERS
8-Bit Timer

The 38B4 group has six built-in timers : Timer 1, Timer 2, Timer 3, Timer 4, Timer 5, and Timer 6.

Each timer has the 8-bit timer latch. All timers are down-counters. When the timer reaches "00_{16}", an underflow occurs with the next count pulse. Then the contents of the timer latch is reloaded into the timer and the timer continues down-counting. When a timer underflows, the interrupt request bit corresponding to that timer is set to "1".

The count can be stopped by setting the stop bit of each timer to "1". The internal system clock can be set to either the high-speed mode or low-speed mode with the CPU mode register. At the same time, timer internal count source is switched to either $f(X_{IN})$ or $f(X_{CIN})$.

●Timer 1, Timer 2

The count sources of timer 1 and timer 2 can be selected by setting the timer 12 mode register. A rectangular waveform of timer 1 underflow signal divided by 2 can be output from the $P4_5/T_{1OUT}$ pin. The active edge of the external clock $CNTR_0$ can be switched with the bit 6 of the interrupt edge selection register.

At reset or when executing the STP instruction, all bits of the timer 12 mode register are cleared to "0", timer 1 is set to "FF_{16}", and timer 2 is set to "01_{16}".

●Timer 3, Timer 4

The count sources of timer 3 and timer 4 can be selected by setting the timer 34 mode register. A rectangular waveform of timer 3 underflow signal divided by 2 can be output from the $P4_6/T_{3OUT}$ pin. The active edge of the external clock $CNTR_1$ **(Note)** can be switched with the bit 7 of the interrupt edge selection register.

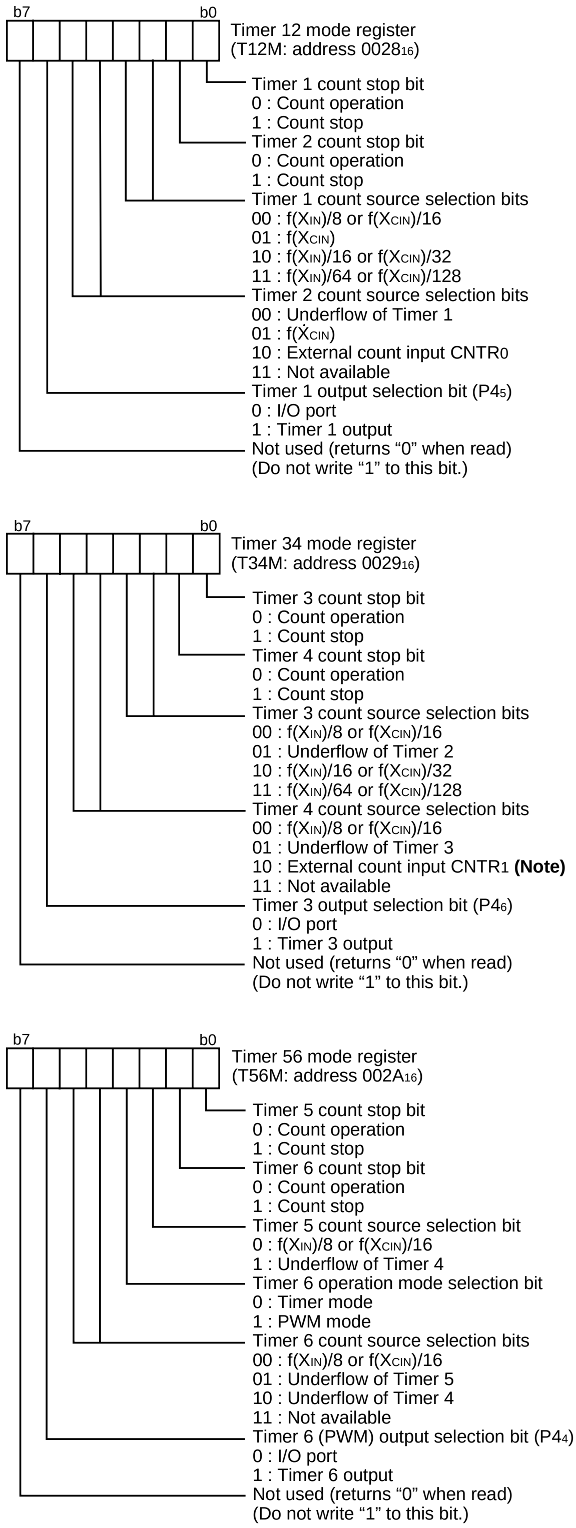
Note: In the mask option type P, $CNTR_1$ function cannot be used.

●Timer 5, Timer 6

The count sources of timer 5 and timer 6 can be selected by setting the timer 56 mode register. A rectangular waveform of timer 6 underflow signal divided by 2 can be output from the $P4_4/PWM_1$ pin.

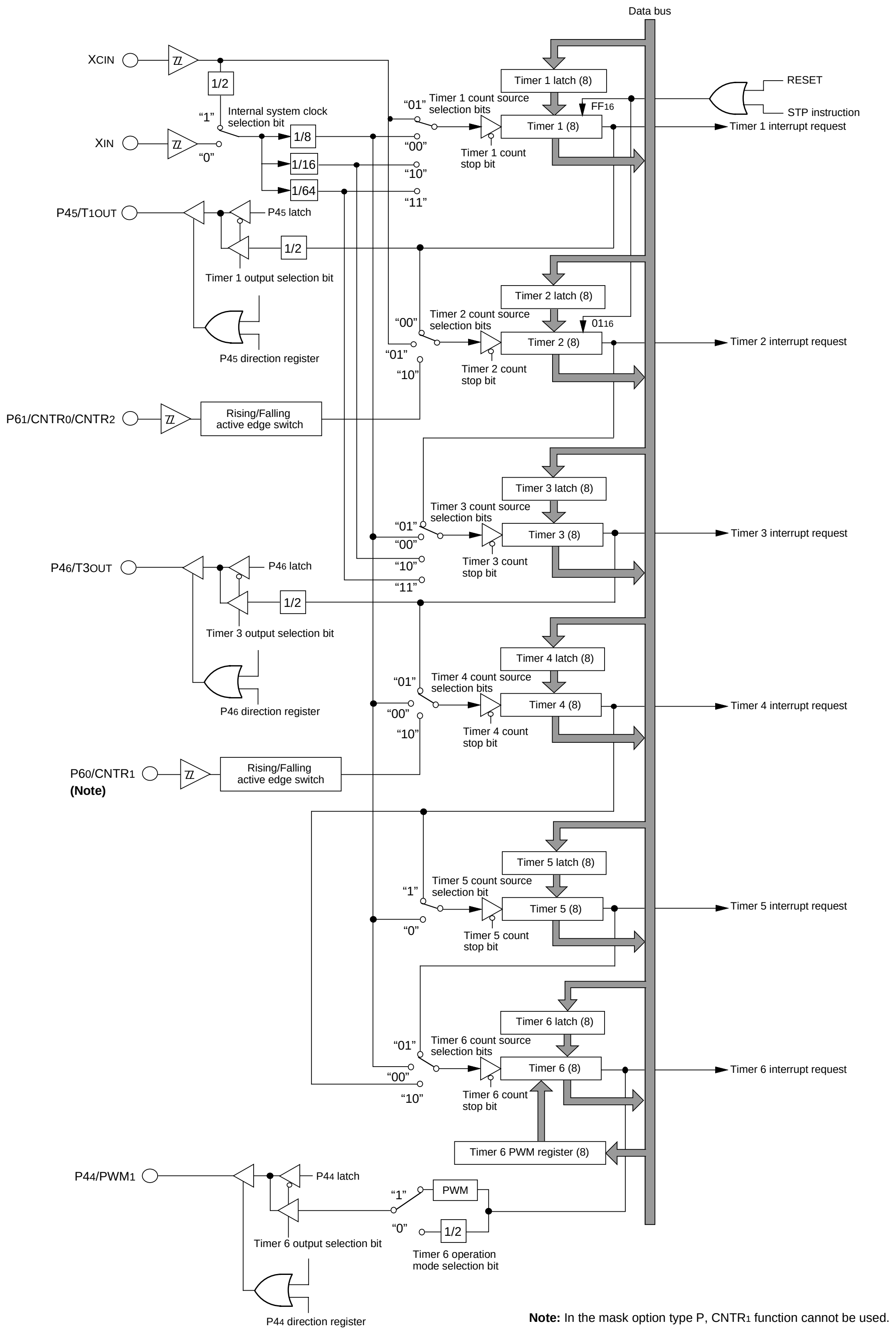
(1) Timer 6 PWM_1 mode

Timer 6 can output a PWM rectangular waveform with "H" duty cycle n/(n+m) from the $P4_4/PWM_1$ pin by setting the timer 56 mode register (refer to Figure 19). The n is the value set in timer 6 latch (address 0025_{16}) and m is the value in the timer 6 PWM register (address 0027_{16}). If n is "0", the PWM output is "L", if m is "0", the PWM output is "H" (n = 0 is prior than m = 0). In the PWM mode, interrupts occur at the rising edge of the PWM output.



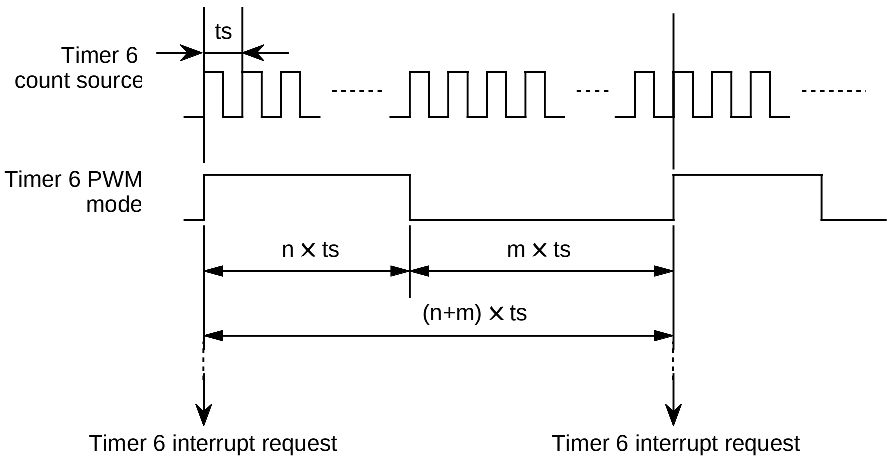
Note: In the mask option type P, $CNTR_1$ function cannot be used.

Fig. 17 Structure of timer related register



Note: In the mask option type P, CNTR1 function cannot be used.

Fig. 18 Block diagram of timer



Note: PWM waveform (duty : n/(n + m) and period: (n + m) × ts) is output.
n : setting value of Timer 6
m: setting value of Timer 6 PWM register
ts: period of Timer 6 count source

Fig. 19 Timing chart of timer 6 PWM$_1$ mode

16-Bit Timer

Timer X is a 16-bit timer that can be selected in one of four modes by the Timer X mode registers 1, 2 and can be controlled the timer X write and the real time port by setting the timer X mode registers.
Read and write operation on 16-bit timer must be performed for both high- and low-order bytes. When reading a 16-bit timer, read from the high-order byte first. When writing to 16-bit timer, write to the low-order byte first. The 16-bit timer cannot perform the correct operation when reading during write operation, or when writing during read operation.

●Timer X

Timer X is a down-counter. When the timer reaches "0000_{16}", an underflow occurs with the next count pulse. Then the contents of the timer latch is reloaded into the timer and the timer continues down-counting. When a timer underflows, the interrupt request bit corresponding to that timer is set to "1".

(1) Timer mode

A count source can be selected by setting the Timer X count source selection bits (bits 1 and 2) of the Timer X mode register 1.

(2) Pulse output mode

Each time the timer underflows, a signal output from the $CNTR_2$ pin is inverted. Except for this, the operation in pulse output mode is the same as in timer mode. When using a timer in this mode, set the port shared with the $CNTR_2$ pin to output.

(3) Event counter mode

The timer counts signals input through the $CNTR_2$ pin. Except for this, the operation in event counter mode is the same as in timer mode. When using a timer in this mode, set the port shared with the $CNTR_2$ pin to input.

(4) Pulse width measurement mode

A count source can be selected by setting the Timer X count source selection bits (bits 1 and 2) of the Timer X mode register 1. When $CNTR_2$ active edge switch bit is "0", the timer counts while the input signal of the $CNTR_2$ pin is at "H". When it is "1", the timer counts while the input signal of the $CNTR_2$ pin is at "L". When using a timer in this mode, set the port shared with the $CNTR_2$ pin to input.

■ Note

•Timer X Write Control

If the timer X write control bit is "0", when the value is written in the address of timer X, the value is loaded in the timer X and the latch at the same time.
If the timer X write control bit is "1", when the value is written in the address of timer X, the value is loaded only in the latch. The value in the latch is loaded in timer X after timer X underflows.
When the value is written in latch only, unexpected value may be set in the high-order counter if the writing in high-order latch and the underflow of timer X are performed at the same timing.

•Real Time Port Control

While the real time port function is valid, data for the real time port are output from ports $P8_5$ and $P8_6$ each time the timer X underflows. (However, if the real time port control bit is changed from "0" to "1", data are output without the timer X.) When the data for the real time port is changed while the real time port function is valid, the changed data are output at the next underflow of timer X.
Before using this function, set the corresponding port direction registers to output mode.

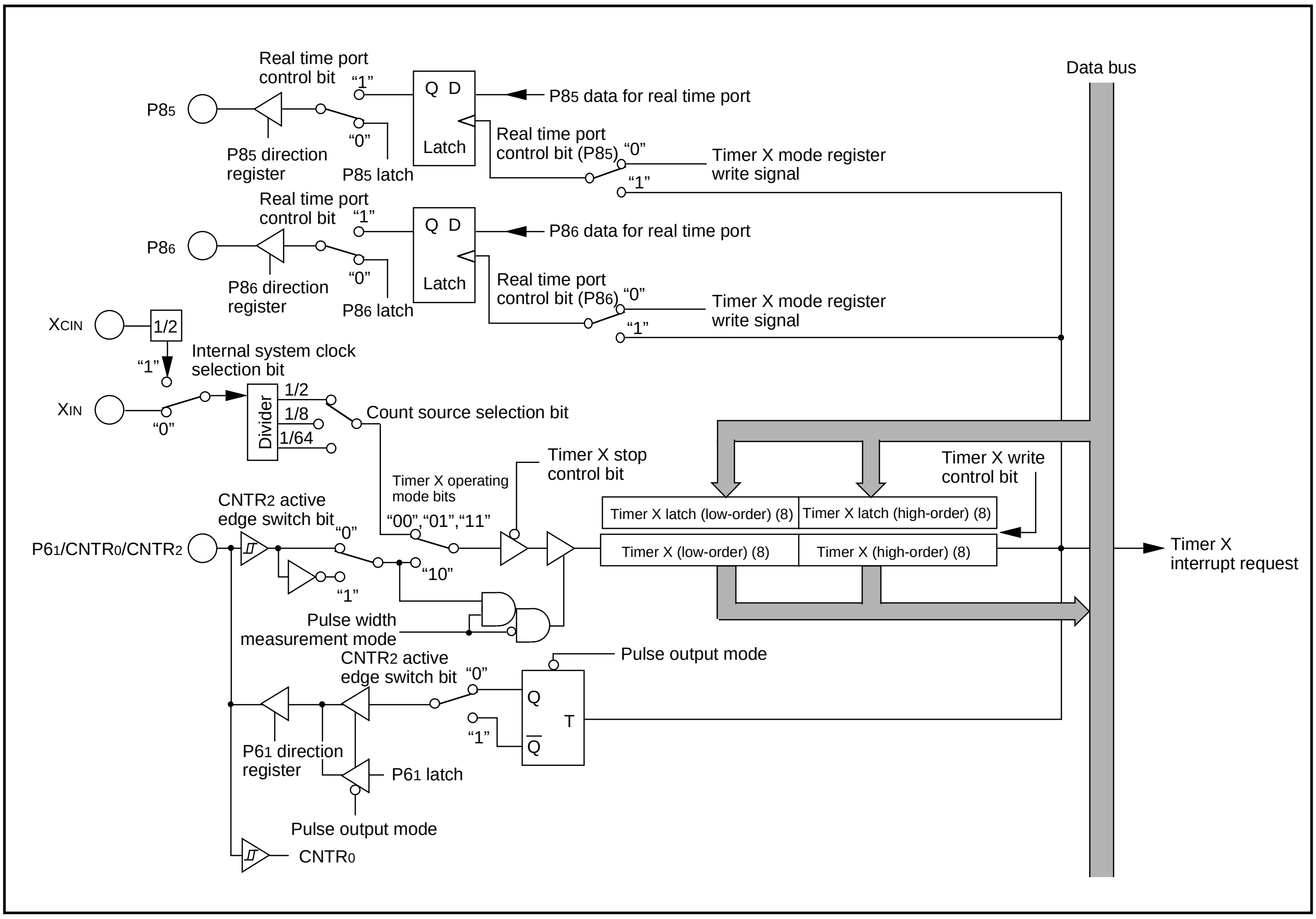


Fig. 20 Block diagram of timer X

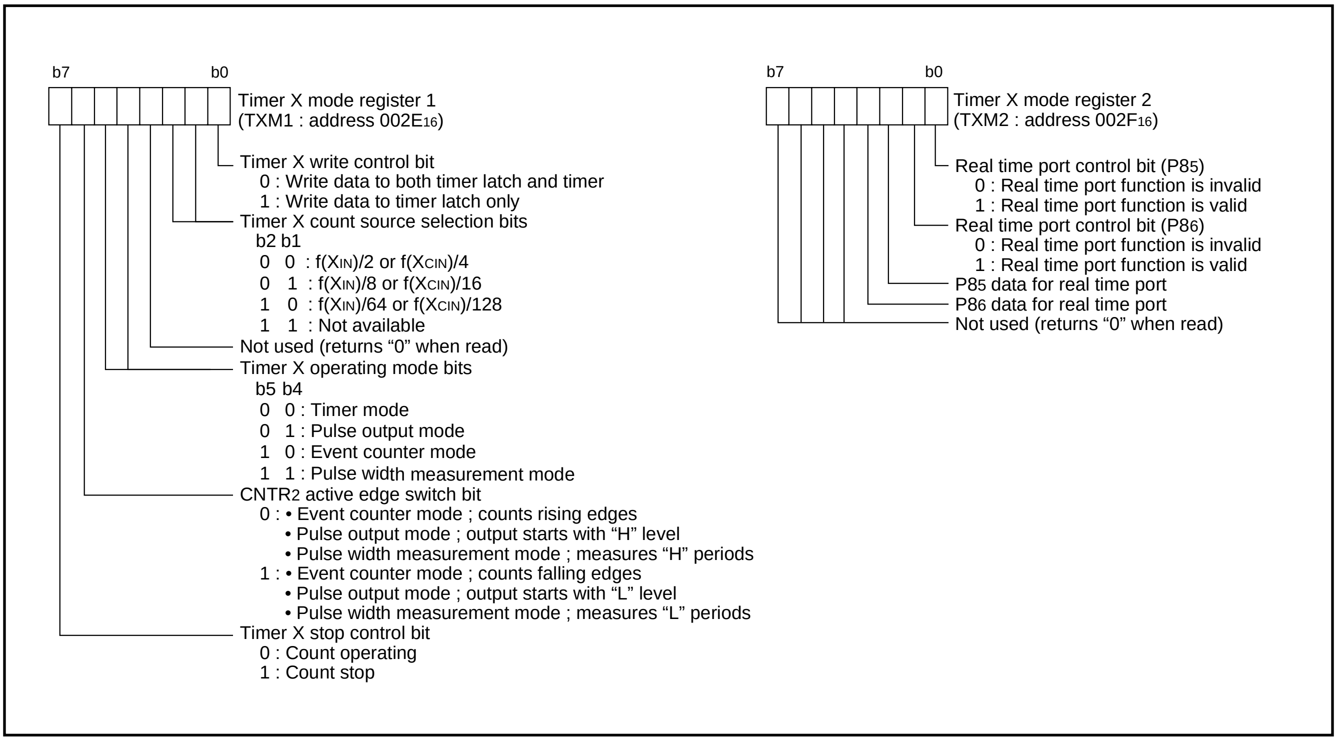


Fig. 21 Structure of timer X related registers

SERIAL I/O
Serial I/O1

Serial I/O1 is used as the clock synchronous serial I/O and has an ordinary mode and an automatic transfer mode. In the automatic transfer mode, serial transfer is performed through the serial I/O automatic transfer RAM which has up to 256 bytes (addresses $0F00_{16}$ to $0FFF_{16}$: addresses $0F60_{16}$ to $0FFF_{16}$ are also used as FLD automatic display RAM).

The $P6_2/S_{RDY1}/AN_8$, $P6_4/INT_4/S_{BUSY1}/AN_{10}$, and $P6_5/S_{STB1}/AN_{11}$ pins each have a handshake I/O signal function and can select either "H" active or "L" active for active logic.

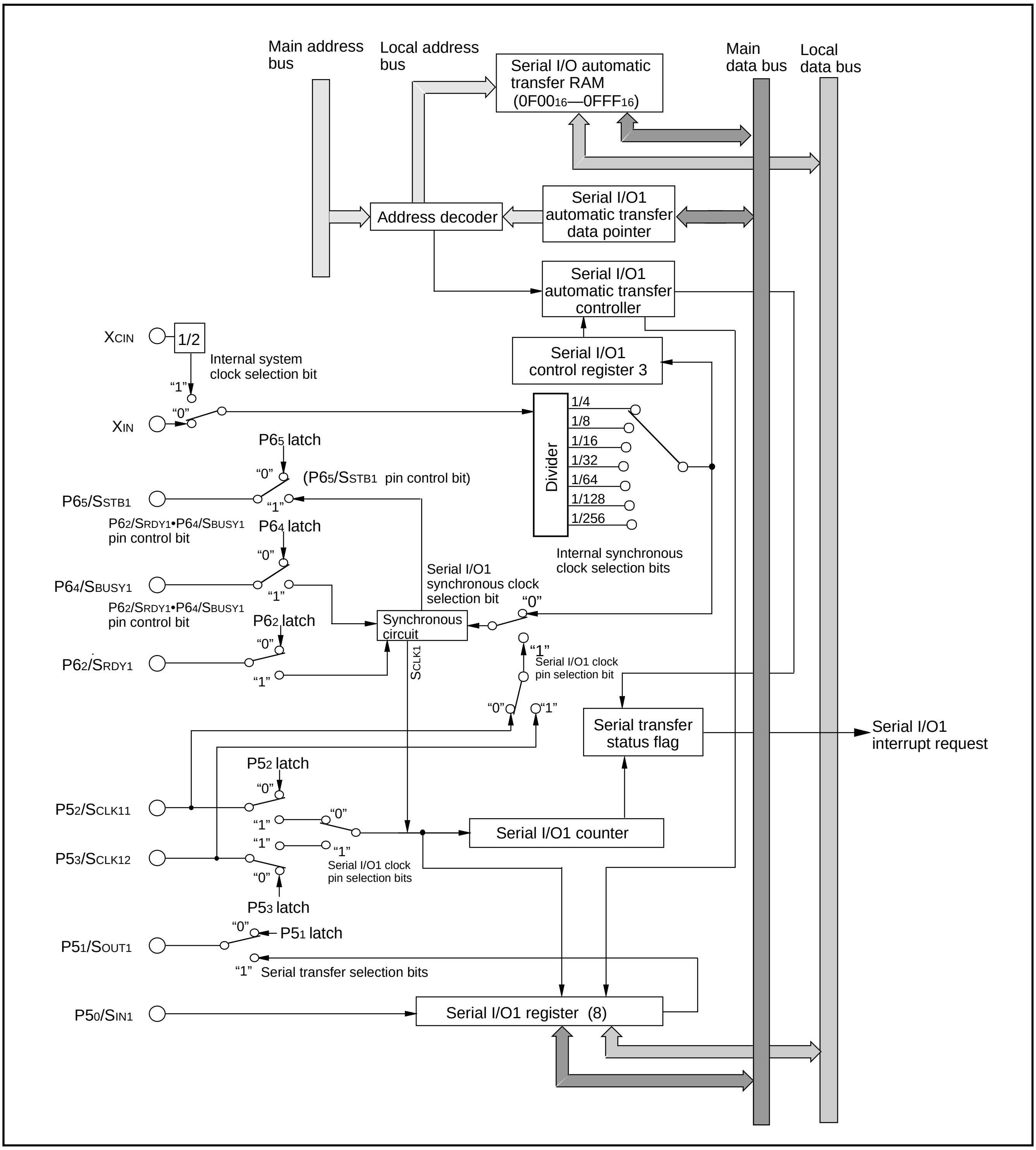


Fig. 22 Block diagram of serial I/O1

b7 b0

Serial I/O1 control register 1
(SIO1CON1 (SC11) : address 0019_{16})

Serial transfer selection bits
- 00: Serial I/O disabled (pins P62,P64,P65,and P50—P53 are I/O ports)
- 01: 8-bit serial I/O
- 10: Not available
- 11: Automatic transfer serial I/O (8-bits)

Serial I/O1 synchronous clock selection bits (P65/SSTB1 pin control bits)
- 00: Internal synchronous clock (P65 pin is an I/O port.)
- 01: External synchronous clock (P65 pin is an I/O port.)
- 10: Internal synchronous clock (P65 pin is an $\overline{\text{SSTB1}}$ output.)
- 11: Internal synchronous clock (P65 pin is an SSTB1 output.)

Serial I/O initialization bit
- 0: Serial I/O initialization
- 1: Serial I/O enabled

Transfer mode selection bit
- 0: Full duplex (transmit and receive) mode (P50 pin is an SIN1 input.)
- 1: Transmit-only mode (P50 pin is an I/O port.)

Transfer direction selection bit
- 0: LSB first
- 1: MSB first

Serial I/O1 clock pin selection bit
- 0:SCLK11 (P53/SCLK12 pin is an I/O port.)
- 1:SCLK12 (P52/SCLK11 pin is an I/O port.)

b7 b0

Serial I/O1 control register 2
(SIO1CON2 (SC12): address $001A_{16}$)

P62/SRDY1 • P64/SBUSY1 pin control bits
- 0000: Pins P62 and P64 are I/O ports
- 0001: Not used
- 0010: P62 pin is an $\overline{\text{SRDY1}}$ output, P64 pin is an I/O port.
- 0011: P62 pin is an SRDY1 output, P64 pin is an I/O port.
- 0100: P62 pin is an I/O port, P64 pin is an $\overline{\text{SBUSY1}}$ input.
- 0101: P62 pin is an I/O port, P64 pin is an SBUSY1 input.
- 0110: P62 pin is an I/O port, P64 pin is an $\overline{\text{SBUSY1}}$ output.
- 0111: P62 pin is an I/O port, P64 pin is an SBUSY1 output.
- 1000: P62 pin is an $\overline{\text{SRDY1}}$ input, P64 pin is an $\overline{\text{SBUSY1}}$ output.
- 1001: P62 pin is an $\overline{\text{SRDY1}}$ input, P64 pin is an SBUSY1 output.
- 1010: P62 pin is an SRDY1 input, P64 pin is an $\overline{\text{SBUSY1}}$ output.
- 1011: P62 pin is an SRDY1 input, P64 pin is an SBUSY1 output.
- 1100: P62 pin is an $\overline{\text{SRDY1}}$ output, P64 pin is an $\overline{\text{SBUSY1}}$ input.
- 1101: P62 pin is an $\overline{\text{SRDY1}}$ output, P64 pin is an SBUSY1 input.
- 1110: P62 pin is an SRDY1 output, P64 pin is an $\overline{\text{SBUSY1}}$ input.
- 1111: P62 pin is an SRDY1 output, P64 pin is an SBUSY1 input.

SBUSY1 output • SSTB1 output function selection bit
(Valid in automatic transfer mode)
- 0: Functions as each 1-byte signal
- 1: Functions as signal for all transfer data

Serial transfer status flag
- 0: Serial transfer completion
- 1: Serial transferring

SOUT1 pin control bit (at no-transfer serial data)
- 0: Output active
- 1: Output high-impedance

P51/SOUT1 P-channel output disable bit
- 0: CMOS 3-state (P-channel output is valid.)
- 1: N-channel open-drain (P-channel output is invalid.)

Fig. 23 Structure of serial I/O1 control registers 1, 2

●Serial I/O1 operation

Either the internal synchronous clock or external synchronous clock can be selected by the serial I/O1 synchronous clock selection bits (b2 and b3 of address 0019_{16}) of serial I/O1 control register 1 as synchronous clock for serial transfer.

The internal synchronous clock has a built-in dedicated divider where 7 different clocks are selected by the internal synchronous clock selection bits (b5, b6 and b7 of address $001C_{16}$) of serial I/O1 control register 3.

The $P6_2$/SRDY1/AN_8, $P6_4$/INT_4/SBUSY1/AN_{10}, and $P6_5$/SSTB1/AN_{11} pins each select either I/O port or handshake I/O signal by the serial I/O1 synchronous clock selection bits (b2 and b3 of address 0019_{16}) of serial I/O1 control register 1 as well as the $P6_2$/SRDY1 • $P6_4$/SBUSY1 pin control bits (b0 to b3 of address $001A_{16}$) of serial I/O1 control register 2.

For the SOUT1 being used as an output pin, either CMOS output or N-channel open-drain output is selected by the $P5_1$/SOUT1 P-channel output disable bit (b7 of address $001A_{16}$) of serial I/O1 control register 2.

Either output active or high-impedance can be selected as a SOUT1 pin state at serial non-transfer by the SOUT1 pin control bit (b6 of address $001A_{16}$) of serial I/O1 control register 2. However, when the external synchronous clock is selected, perform the following setup to put the SOUT1 pin into a high-impedance state.

When the SCLK1 input is “H” after completion of transfer, set the SOUT1 pin control bit to “1”.

When the SCLK1 input goes to “L” after the start of the next serial transfer, the SOUT1 pin control bit is automatically reset to “0” and put into an output active state.

Regardless of whether the internal synchronous clock or external synchronous clock is selected, the full duplex mode and the transmit-only mode are available for serial transfer, one of which is selected by the transfer mode selection bit (b5 of address 0019_{16}) of serial I/O1 control register 1.

Either LSB first or MSB first is selected for the I/O sequence of the serial transfer bit strings by the transfer direction selection bit (b6 of address 0019_{16}) of serial I/O1 control register 1.

When using serial I/O1, first select either 8-bit serial I/O or automatic transfer serial I/O by the serial transfer selection bits (b0 and b1 of address 0019_{16}) of serial I/O1 control register 1, after completion of the above bit setup. Next, set the serial I/O initialization bit (b4 of address 0019_{16}) of serial I/O1 control register 1 to “1” (Serial I/O enable) .

When stopping serial transfer while data is being transferred, regardless of whether the internal or external synchronous clock is selected, reset the serial I/O initialization bit (b4) to “0”.

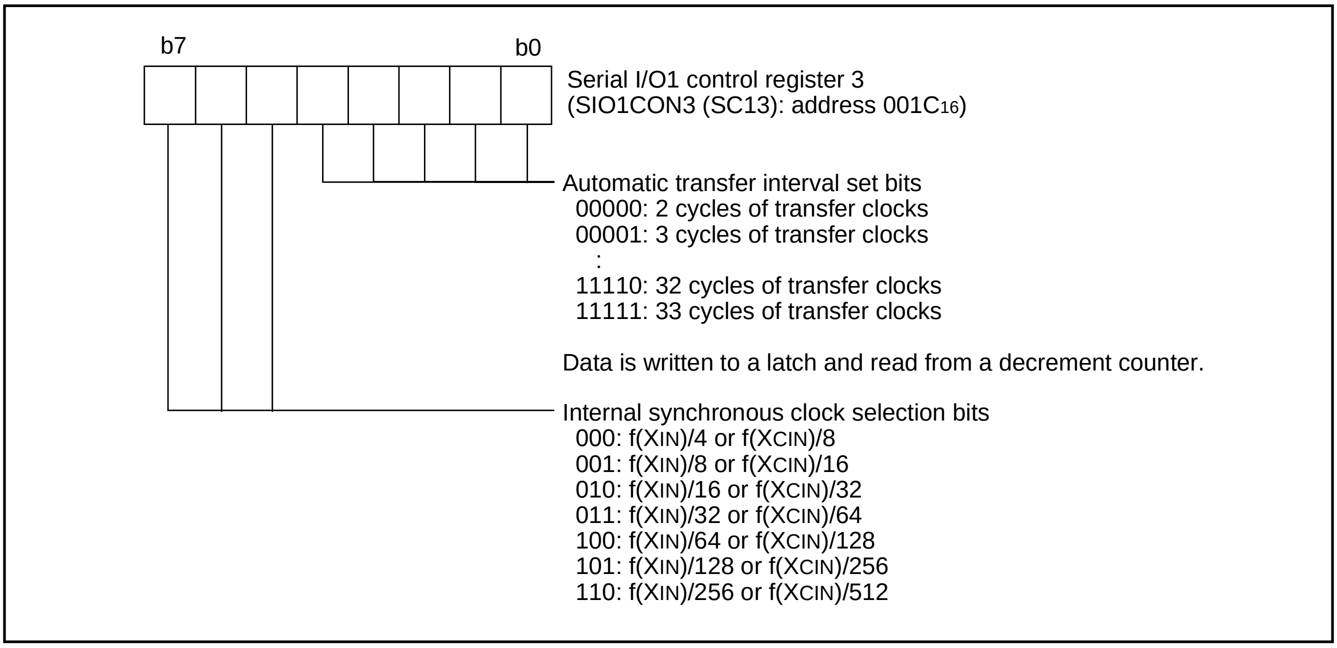


Fig. 24 Structure of serial I/O1 control register 3

(1) 8-bit serial I/O mode

Address 001B$_{16}$ is assigned to the serial I/O1 register.

When the internal synchronous clock is selected, a serial transfer of the 8-bit serial I/O is started by a write signal to the serial I/O1 register (address 001B$_{16}$).

The serial transfer status flag (b5 of address 001A$_{16}$) of serial I/O1 control register 2 indicates the shift register status of serial I/O1, and is set to “1” by writing into the serial I/O1 register, which becomes a transfer start trigger and reset to “0” after completion of 8-bit transfer. At the same time, a serial I/O1 interrupt request occurs.

When the external synchronous clock is selected, the contents of the serial I/O1 register are continuously shifted while transfer clocks are input to S_{CLK1}. Therefore, the clock needs to be controlled externally.

(2) Automatic transfer serial I/O mode

The serial I/O1 automatic transfer controller controls the write and read operations of the serial I/O1 register, so the function of address 001B$_{16}$ is used as a transfer counter (1-byte units).

When performing serial transfer through the serial I/O automatic transfer RAM (addresses 0F00$_{16}$ to 0FFF$_{16}$), it is necessary to set the serial I/O1 automatic transfer data pointer (address 0018$_{16}$) beforehand.

Input the low-order 8 bits of the first data store address to be serially transferred to the automatic transfer data pointer set bits.

When the internal synchronous clock is selected, the transfer interval for each 1-byte data can be set by the automatic transfer interval set bits (b0 to b4 of address 001C$_{16}$) of serial I/O1 control register 3 in the following cases:

1. When using no handshake signal
2. When using the S_{RDY1} output, S_{BUSY1} output, and S_{STB1} output of the handshake signal independently
3. When using a combination of S_{RDY1} output and S_{STB1} output or a combination of S_{BUSY1} output and S_{STB1} output of the handshake signal

It is possible to select one of 32 different values, namely 2 to 33 cycles of the transfer clock, as a setting value.

When using the S_{BUSY1} output and selecting the S_{BUSY1} output • S_{STB1} output function selection bit (b4 of address 001A$_{16}$) of serial I/O1 control register 2 as the signal for all transfer data, provided that the automatic transfer interval setting is valid, a transfer interval is placed before the start of transmission/reception of the first data and after the end of transmission/reception of the last data.

For S_{STB1} output, regardless of the contents of the S_{BUSY1} output • S_{STB1} output function selection bit (b4), the transfer interval for each 1-byte data is longer than the set value by 2 cycles.

Furthermore, when using a combination of S_{BUSY1} output and S_{STB1} output as a signal for all transfer data, the transfer interval after the end of transmission/reception of the last data is longer than the set value by 2 cycles.

When the external synchronous clock is selected, automatic transfer interval setting is disabled.

After completion of the above bit setup, if the internal synchronous clock is selected, automatic serial transfer is started by writing the value of “number of transfer bytes - 1” into the transfer counter (address 001B$_{16}$).

When the external synchronous clock is selected, write the value of “number of transfer bytes - 1” into the transfer counter and input an internal system clock interval of 5 cycles or more. After that, input transfer clock to S_{CLK1}.

As a transfer interval for each 1-byte data transfer, input an internal system clock interval of 5 cycles or more from the clock rise time of the last bit.

Regardless of whether the internal or external synchronous clock is selected, the automatic transfer data pointer and the transfer counter are decremented after each 1-byte data is received and then written into the automatic transfer RAM. The serial transfer status flag (b5 of address 001A$_{16}$) is set to “1” by writing data into the transfer counter. Writing data becomes a transfer start trigger, and the serial transfer status flag is reset to “0” after the last data is written into the automatic transfer RAM. At the same time, a serial I/O1 interrupt request occurs.

The values written in the automatic transfer data pointer set bits (b0 to b7 of address 0018$_{16}$) and the automatic transfer interval set bits (b0 to b4 of address 001C$_{16}$) are held in the latch.

When data is written into the transfer counter, the values latched in the automatic transfer data pointer set bits (b0 to b7) and the automatic transfer interval set bits (b0 to b4) are transferred to the decrement counter.

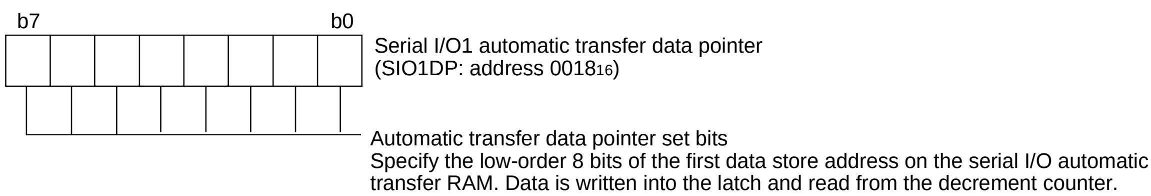


Fig. 25 Structure of serial I/O1 automatic transfer data pointer

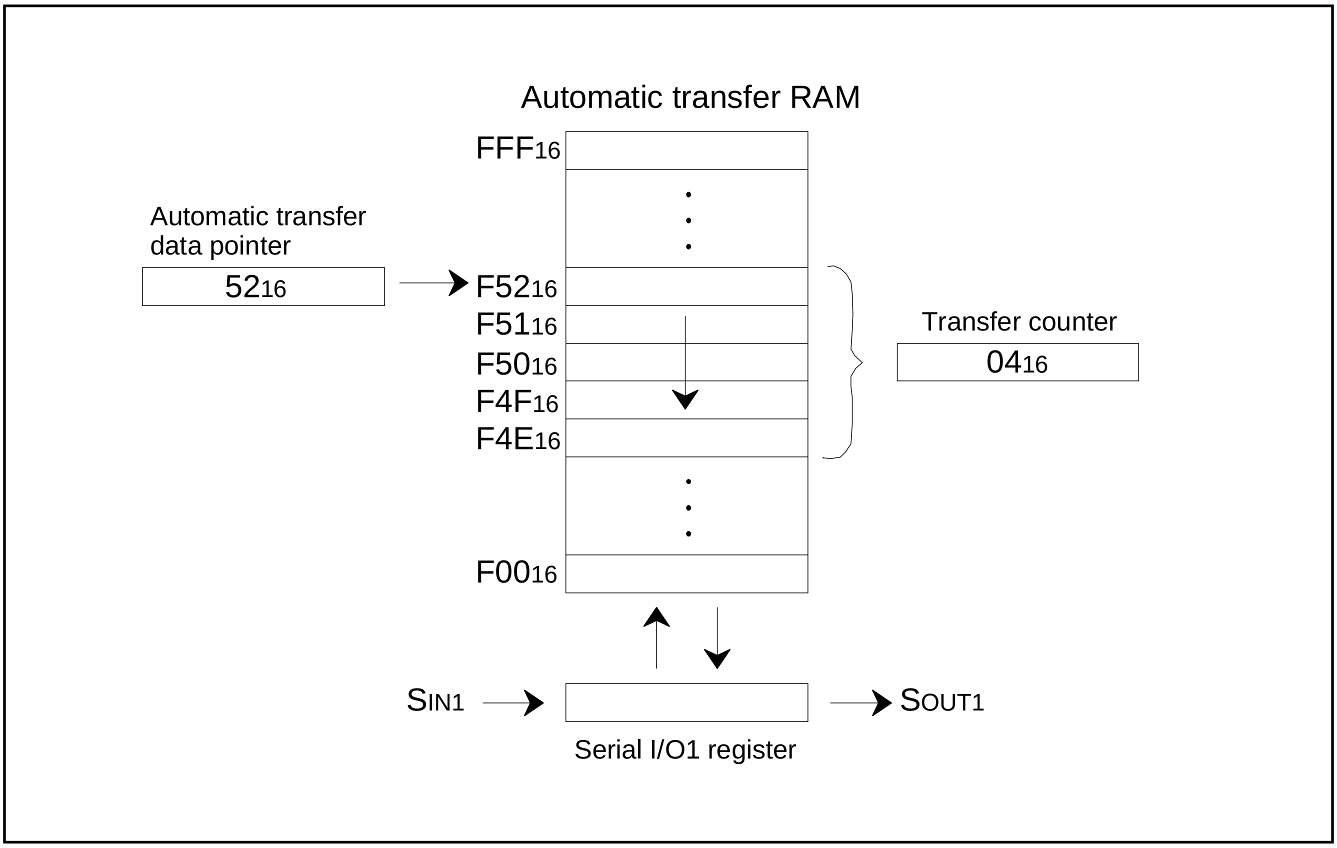


Fig. 26 Automatic transfer serial I/O operation

●Handshake signal

1. SSTB1 output signal

The SSTB1 output is a signal to inform an end of transmission/reception to the serial transfer destination. The SSTB1 output signal can be used only when the internal synchronous clock is selected. In the initial status, namely, in the status in which the serial I/O initialization bit (b4) is reset to “0”, the SSTB1 output goes to “L”, or the $\overline{\text{SSTB1}}$ output goes to “H”.

At the end of transmit/receive operation, when the data of the serial I/O1 register is all output from SOUT1, pulses are output in the period of 1 cycle of the transfer clock so as to cause the SSTB1 output to go “H” or the $\overline{\text{SSTB1}}$ output to go “L.” After that, each pulse is returned to the initial status in which SSTB1 output goes to “L” or the $\overline{\text{SSTB1}}$ output goes to “H”.

Furthermore, after 1 cycle, the serial transfer status flag (b5) is reset to “0”.

In the automatic transfer serial I/O mode, whether the SSTB1 output is to be active at an end of each 1-byte data or after completion of transfer of all data can be selected by the SBUSY1 output • SSTB1 output function selection bit (b4 of address 001A16) of serial I/O1 control register 2.

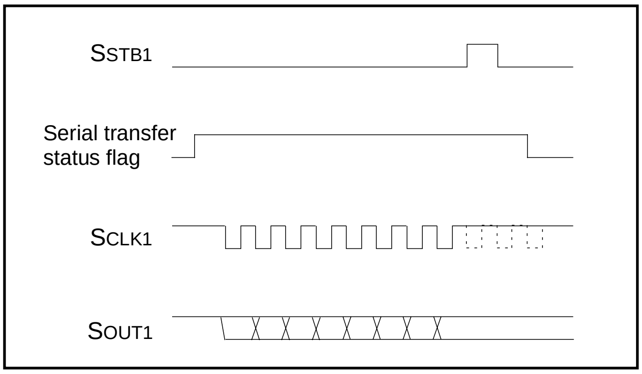


Fig. 27 SSTB1 output operation

2. SBUSY1 input signal

The SBUSY1 input is a signal which receives a request for a stop of transmission/reception from the serial transfer destination.

When the internal synchronous clock is selected, input an “H” level signal into the SBUSY1 input and an “L” level signal into the $\overline{\text{SBUSY1}}$ input in the initial status in which transfer is stopped.

When starting a transmit/receive operation, input an “L” level signal into the SBUSY1 input and an “H” level signal into the $\overline{\text{SBUSY1}}$ input in the period of 1.5 cycles or more of the transfer clock. Then, transfer clocks are output from the SCLK1 output.

When an “H” level signal is input into the SBUSY1 input and an “L” level signal into the $\overline{\text{SBUSY1}}$ input after a transmit/receive operation is started, this transmit/receive operation are not stopped immediately and the transfer clocks from the SCLK1 output is not stopped until the specified number of bits are transmitted and received.

The handshake unit of the 8-bit serial I/O is 8 bits and that of the automatic transfer serial I/O is 8 bits.

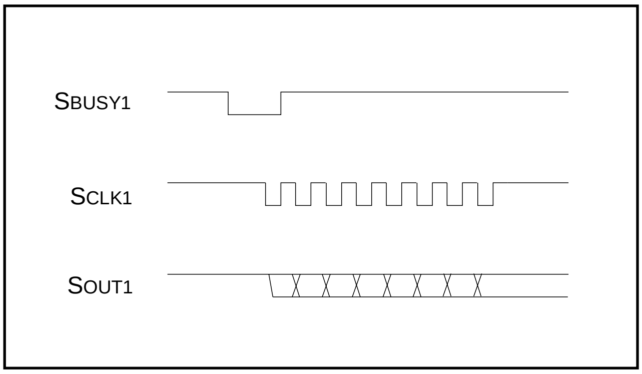


Fig. 28 SBUSY1 input operation (internal synchronous clock)

When the external synchronous clock is selected, input an “H” level signal into the SBUSY1 input and an “L” level signal into the $\overline{\text{SBUSY1}}$ input in the initial status in which transfer is stopped. At this time, the transfer clocks to be input in SCLK1 become invalid.

During serial transfer, the transfer clocks to be input in SCLK1 become valid, enabling a transmit/receive operation, while an “L” level signal is input into the SBUSY1 input and an “H” level signal is input into the $\overline{\text{SBUSY1}}$ input.

When changing the input values in the SBUSY1 input and the $\overline{\text{SBUSY1}}$ input at these operations, change them when the SCLK1 input is in a high state.

When the high impedance of the SOUT1 output is selected by the SOUT1 pin control bit (b6), the SOUT1 output becomes active, enabling serial transfer by inputting a transfer clock to SCLK1, while an “L” level signal is input into the SBUSY1 input and an “H” level signal is input into the $\overline{\text{SBUSY1}}$ input.

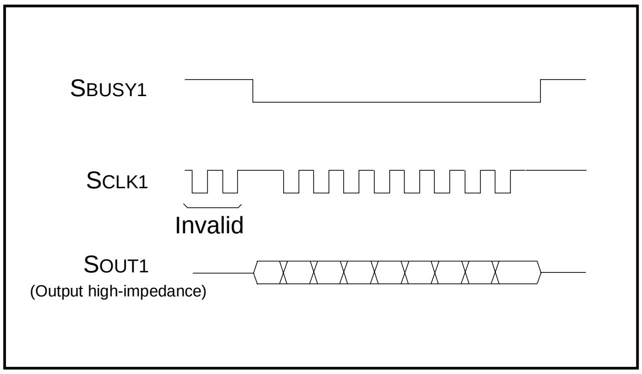


Fig. 29 SBUSY1 input operation (external synchronous clock)

3. SBUSY1 output signal

The SBUSY1 output is a signal which requests a stop of transmission/reception to the serial transfer destination. In the automatic transfer serial I/O mode, regardless of the internal or external synchronous clock, whether the SBUSY1 output is to be active at transfer of each 1-byte data or during transfer of all data can be selected by the SBUSY1 output • SSTB1 output function selection bit (b4).

In the initial status, the status in which the serial I/O initialization bit (b4) is reset to “0”, the SBUSY1 output goes to “H” and the $\overline{\text{SBUSY1}}$ output goes to “L”.

When the internal synchronous clock is selected, in the 8-bit serial I/O mode and the automatic transfer serial I/O mode (SBUSY1 output function outputs in 1-byte units), the SBUSY1 output goes to "L" and the $\overline{\text{SBUSY1}}$ output goes to "H" before 0.5 cycle (transfer clock) of the timing at which the transfer clock from the SCLK1 output goes to "L" at a start of transmit/receive operation.
In the automatic transfer serial I/O mode (the SBUSY1 output function outputs all transfer data), the SBUSY1 output goes to "L" and the $\overline{\text{SBUSY1}}$ output goes to "H" when the first transmit data is written into the serial I/O1 register (address $001B_{16}$).
When the external synchronous clock is selected, the SBUSY1 output goes to "L" and the $\overline{\text{SBUSY1}}$ output goes to "H" when transmit data is written into the serial I/O1 register to start a transmit operation, regardless of the serial I/O transfer mode.
At termination of transmit/receive operation, the SBUSY1 output returns to "H" and the $\overline{\text{SBUSY1}}$ output returns to "L", the initial status, when the serial transfer status flag is set to "0", regardless of whether the internal or external synchronous clock is selected.
Furthermore, in the automatic transfer serial I/O mode (SBUSY1 output function outputs in 1-byte units), the SBUSY1 output goes to "H" and the $\overline{\text{SBUSY1}}$ output goes to "L" each time 1-byte of receive data is written into the automatic transfer RAM.

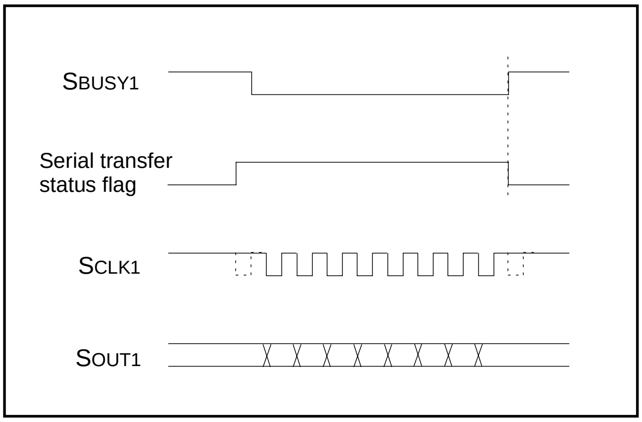


Fig. 30 SBUSY1 output operation (internal synchronous clock, 8-bits serial I/O)

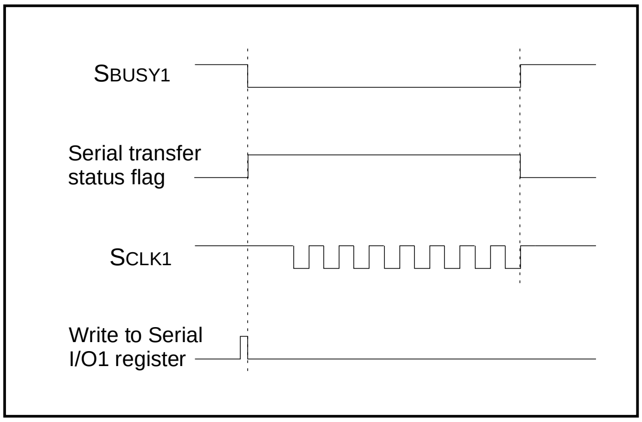


Fig. 31 SBUSY1 output operation (external synchronous clock, 8-bits serial I/O)

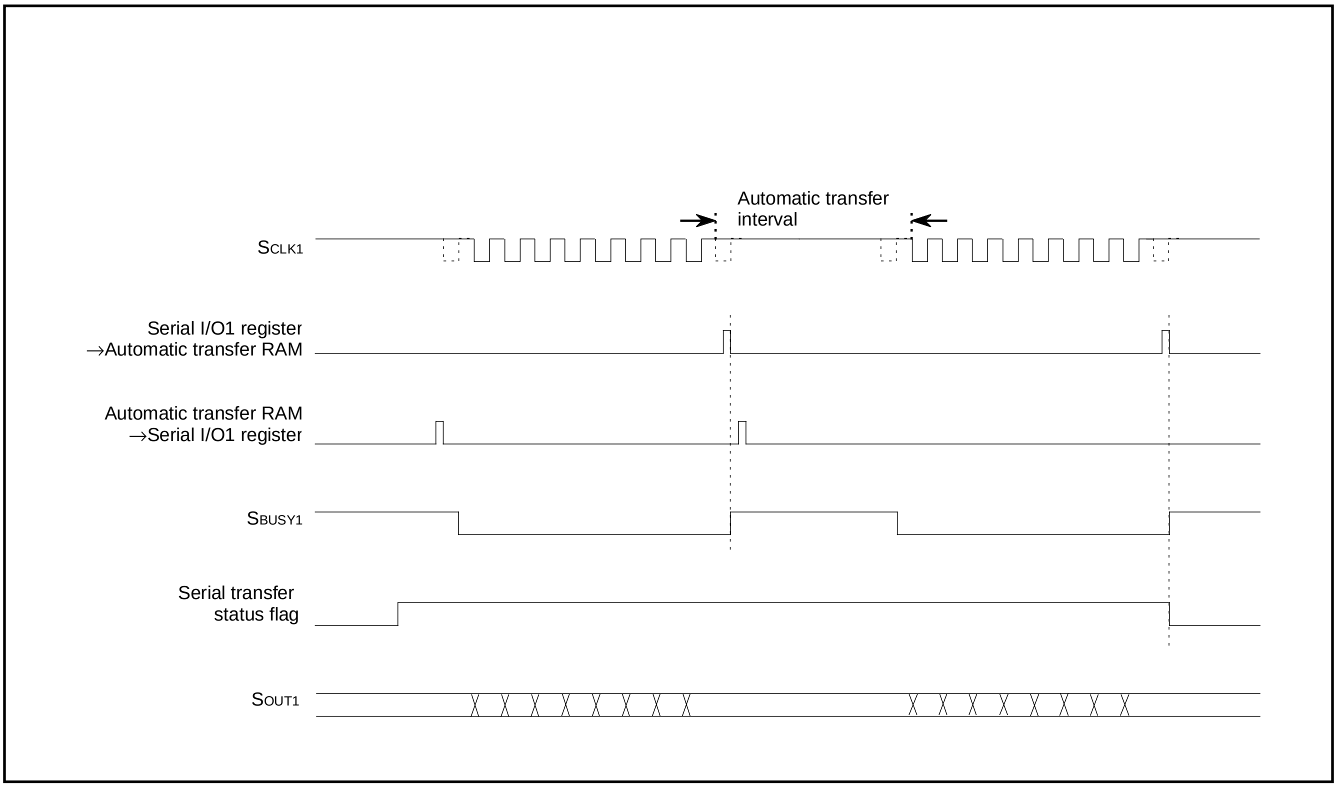


Fig. 32 SBUSY1 output operation in automatic transfer serial I/O mode (internal synchronous clock, SBUSY1 output function outputs each 1-byte)

4. SRDY1 output signal

The SRDY1 output is a transmit/receive enable signal which informs the serial transfer destination that transmit/receive is ready. In the initial status, when the serial I/O initialization bit (b4) is reset to “0”, the SRDY1 output goes to “L” and the $\overline{\text{SRDY1}}$ output goes to “H”. After transmitted data is stored in the serial I/O1 register (address $001B_{16}$) and a transmit/receive operation becomes ready, the SRDY1 output goes to “H” and the $\overline{\text{SRDY1}}$ output goes to “L”. When a transmit/receive operation is started and the transfer clock goes to “L”, the SRDY1 output goes to “L” and the $\overline{\text{SRDY1}}$ output goes to “H”.

5. SRDY1 input signal

The SRDY1 input signal becomes valid only when the SRDY1 input and the SBUSY1 output are used. The SRDY1 input is a signal for receiving a transmit/receive ready completion signal from the serial transfer destination.

When the internal synchronous clock is selected, input a low level signal into the SRDY1 input and a high level signal into the $\overline{\text{SRDY1}}$ input in the initial status in which the transfer is stopped.

When an “H” level signal is input into the SRDY1 input and an “L” level signal is input into the $\overline{\text{SRDY1}}$ input for a period of 1.5 cycles or more of transfer clock, transfer clocks are output from the SCLK1 output and a transmit/receive operation is started.

After the transmit/receive operation is started and an “L” level signal is input into the SRDY1 input and an “H” level signal into the $\overline{\text{SRDY1}}$ input, this operation cannot be immediately stopped.

After the specified number of bits are transmitted and received, the transfer clocks from the SCLK1 output is stopped. The handshake unit of the 8-bit serial I/O and that of the automatic transfer serial I/O are of 8 bits.

When the external synchronous clock is selected, the SRDY1 input becomes one of the triggers to output the SBUSY1 signal.

To start a transmit/receive operation (SBUSY1 output: “L”, $\overline{\text{SBUSY1}}$ output: “H”), input an “H” level signal into the SRDY1 input and an “L” level signal into the $\overline{\text{SRDY1}}$ input, and also write transmit data into the serial I/O1 register.

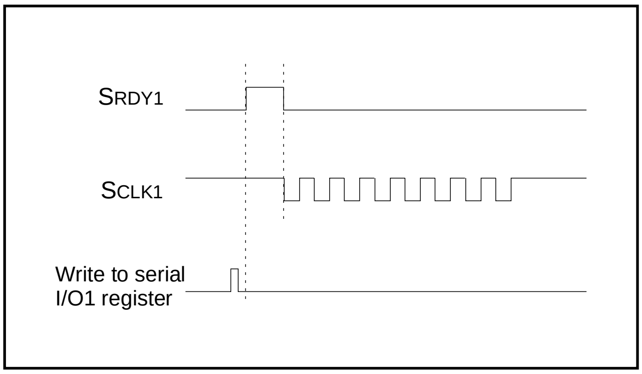


Fig. 33 SRDY1 output operation

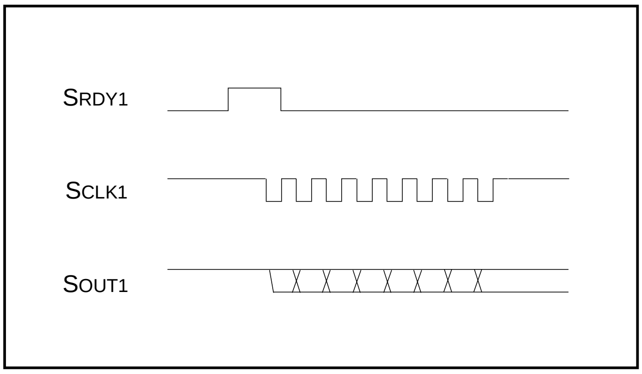


Fig. 34 SRDY1 input operation (internal synchronous clock)

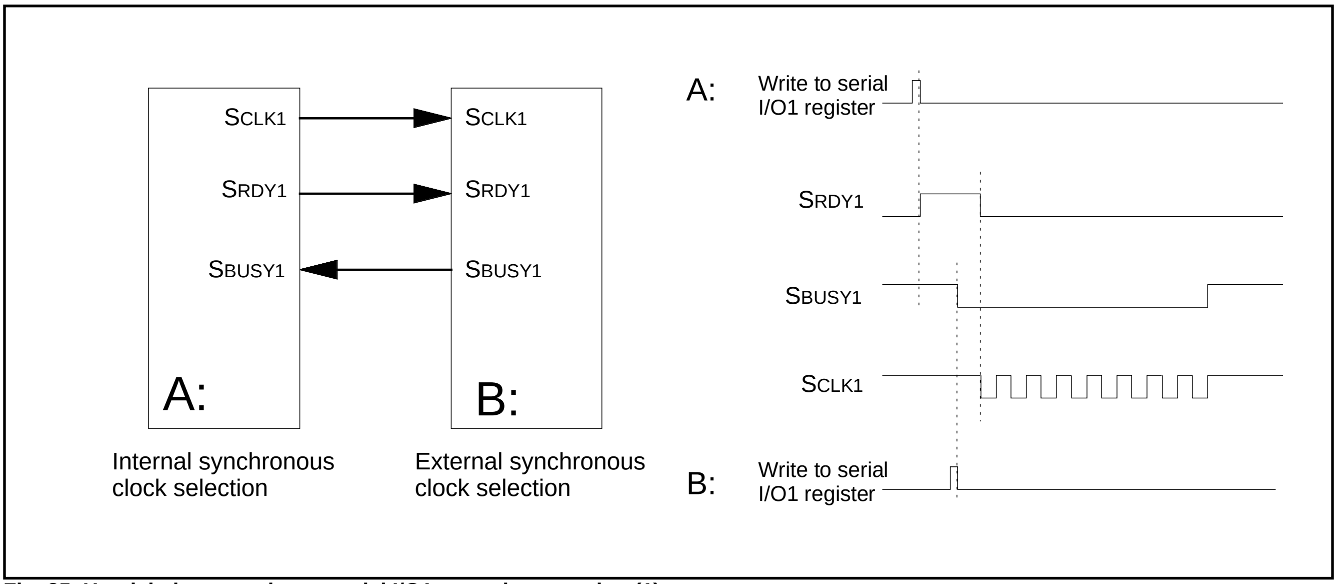


Fig. 35 Handshake operation at serial I/O1 mutual connecting (1)

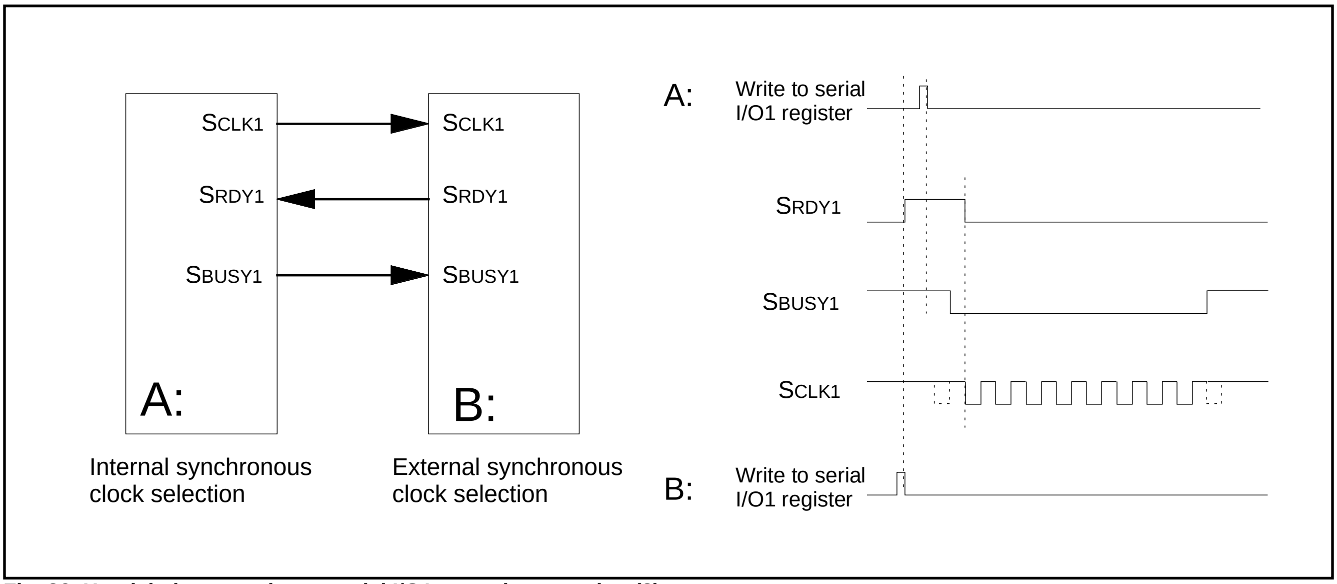


Fig. 36 Handshake operation at serial I/O1 mutual connecting (2)

Serial I/O2

Serial I/O2 can be used as either clock synchronous or asynchronous (UART) serial I/O. A dedicated timer (baud rate generator) is also provided for baud rate generation during serial I/O2 operation.

(1) Clock synchronous serial I/O mode

The clock synchronous serial I/O mode can be selected by setting the serial I/O2 mode selection bit (b6) of the serial I/O2 control register (address 001D16) to "1". For clock synchronous serial I/O, the transmitter and the receiver must use the same clock for serial I/O2 operation. If an internal clock is used, transmit/receive is started by a write signal to the serial I/O2 transmit/receive buffer register (TB/RB) (address 001F16).

When P57 (SCLK22) is selected as a clock I/O pin, $\overline{\text{SRDY2}}$ output function is invalid, and P56 (SCLK21) is used as an I/O port.

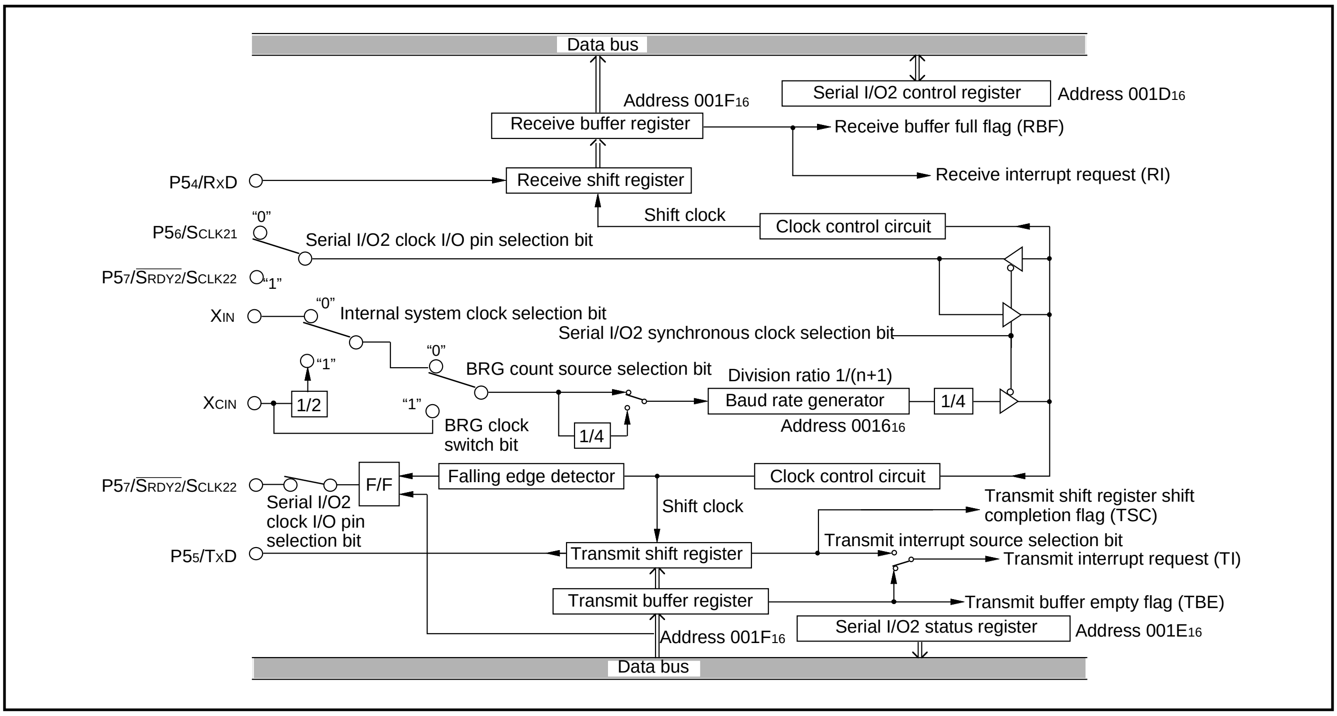
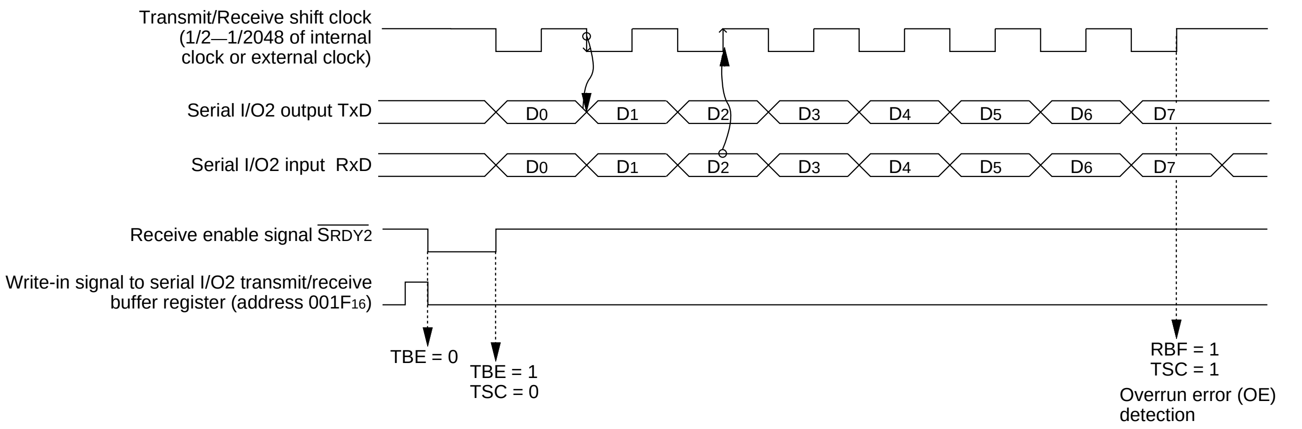


Fig. 37 Block diagram of clock synchronous serial I/O2



Notes 1 : The transmit interrupt (TI) can be selected to occur either when the transmit buffer has emptied (TBE=1) or after the transmit shift operation has ended (TSC=1), by setting transmit interrupt source selection bit (TIC) of the serial I/O2 control register.
2 : If data is written to the transmit buffer register when TSC=0, the transmit clock is generated continuously and serial data is output continuously from the TxD pin.
3 : The receive interrupt (RI) is set when the receive buffer full flag (RBF) becomes "1".

Fig. 38 Operation of clock synchronous serial I/O2 function

(2) Asynchronous serial I/O (UART) mode

The asynchronous serial I/O (UART) mode can be selected by clearing the serial I/O2 mode selection bit (b6) of the serial I/O2 control register (address $001D_{16}$) to “0”. Eight serial data transfer formats can be selected and the transfer formats used by the transmitter and receiver must be identical.

The transmit and receive shift registers each have a buffer (the two buffers have the same address in memory). Since the shift register cannot be written to or read from directly, transmit data is written to the transmit buffer, and receive data is read from the receive buffer. The transmit buffer can also hold the next data to be transmitted, and the receive buffer can receive 2-byte data continuously.

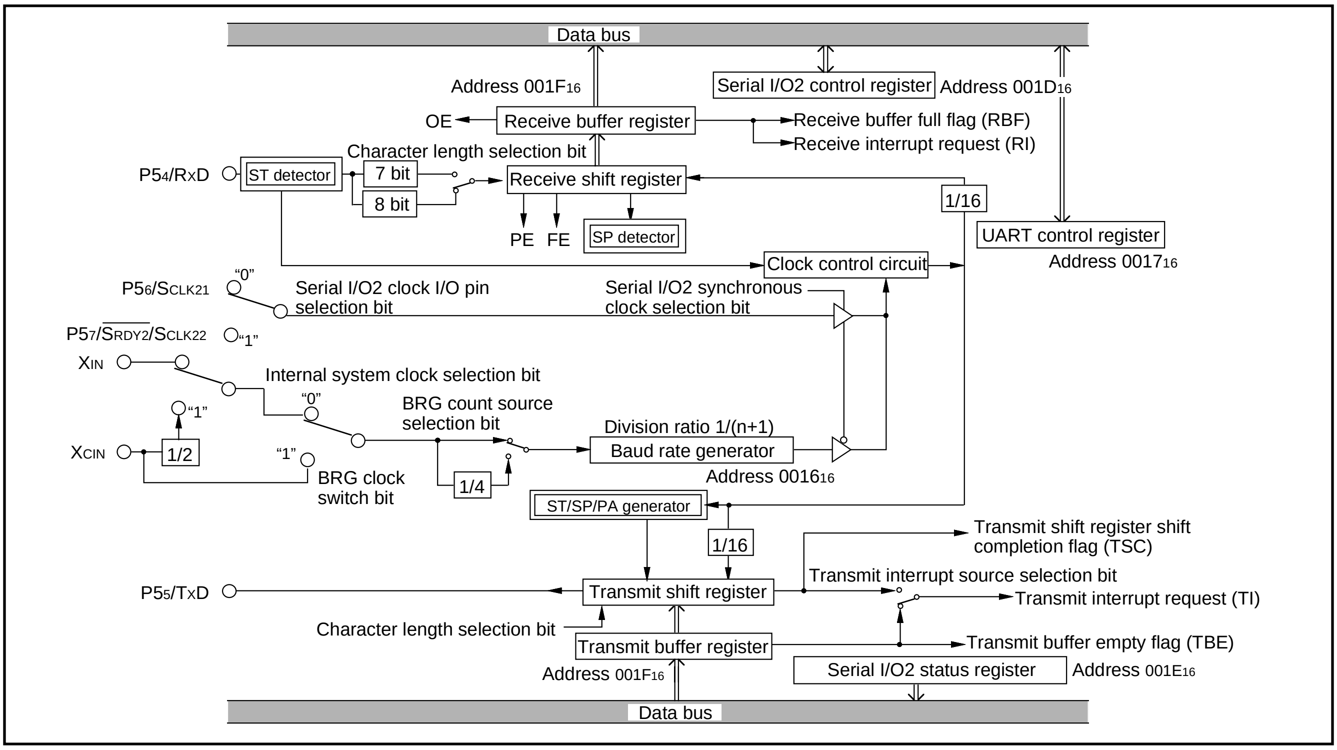


Fig. 39 Block diagram of UART serial I/O2

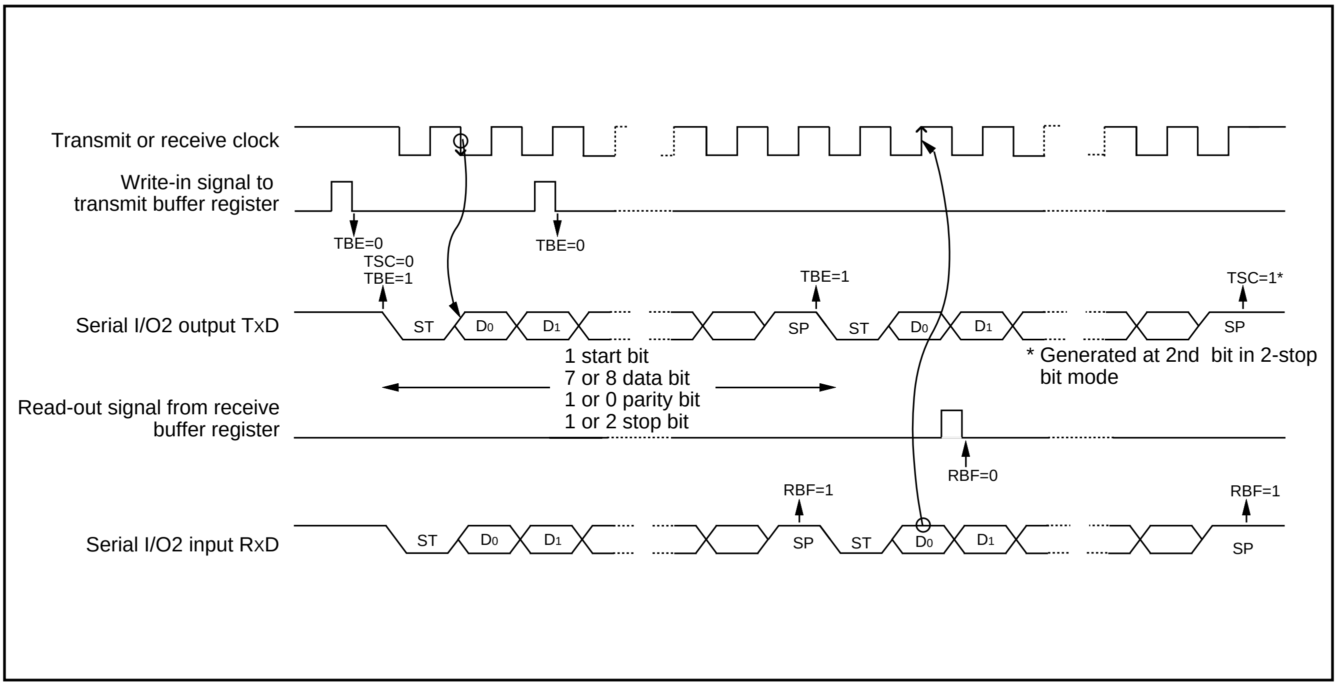


Fig. 40 Operation of UART serial I/O2 function

[Serial I/O2 Control Register] SIO2CON (001D16)

The serial I/O2 control register contains eight control bits for serial I/O2 functions.

[UART Control Register] UARTCON (001716)

This is a 7 bit register containing four control bits, which are valid when UART is selected, two control bits, which are valid when using serial I/O2, and one control bit, which is always valid.
Data format of serial data receive/transfer and the output structure of the P55/TxD pin, etc. are set by this register.

[Serial I/O2 Status Register] SIO2STS (001E16)

The read-only serial I/O2 status register consists of seven flags (b0 to b6) which indicate the operating status of the serial I/O2 function and various errors. Three of the flags (b4 to b6) are only valid in the UART mode. The receive buffer full flag (b1) is cleared to “0” when the receive buffer is read.
The error detection is performed at the same time data is transferred from the receive shift register to the receive buffer register, and the receive buffer full flag is set. A writing to the serial I/O2 status register clears error flags OE, PE, FE, and SE (b3 to b6, respectively). Writing “0” to the serial I/O2 enable bit (SIOE : b7 of the serial I/O2 control register) also clears all the status flags, including the error flags.
All bits of the serial I/O2 status register are initialized to “0” at reset, but if the transmit enable bit (b4) of the serial I/O2 control register has been set to “1”, the transmit shift register shift completion flag (b2) and the transmit buffer empty flag (b0) become “1”.

[Serial I/O2 Transmit Buffer Register/Receive Buffer Register] TB/RB (001F16)

The transmit buffer and the receive buffer are located in the same address. The transmit buffer is write-only and the receive buffer is read-only. If a character bit length is 7 bits, the MSB of data stored in the receive buffer is “0”.

[Baud Rate Generator] BRG (001616)

The baud rate generator determines the baud rate for serial transfer. With the 8-bit counter having a reload register, the baud rate generator divides the frequency of the count source by 1/(n+1), where n is the value written to the baud rate generator.

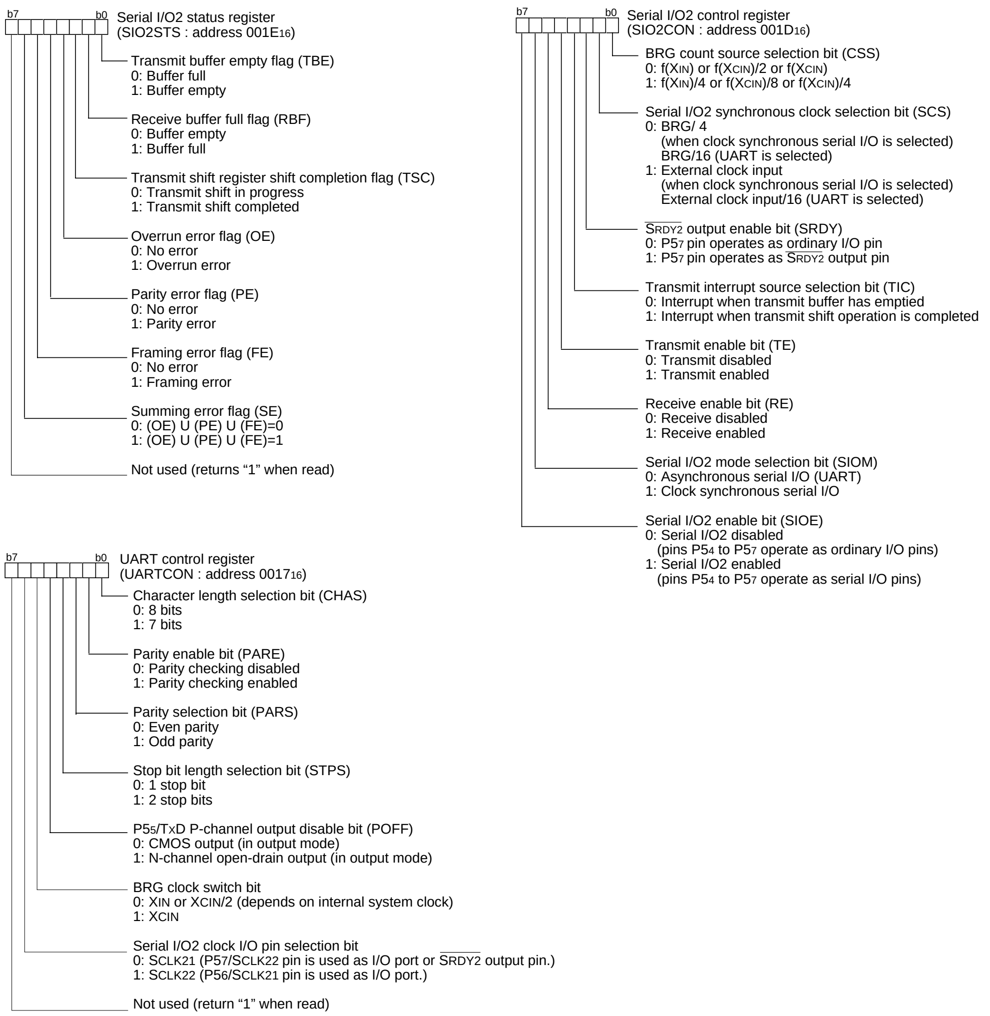


Fig. 41 Structure of serial I/O2 related register

FLD CONTROLLER

The 38B4 group has fluorescent display (FLD) drive and control circuits.

The FLD controller consists of the following components:

- •40 pins for FLD control pins
- •FLDC mode register
- •FLD data pointer
- •FLD data pointer reload register
- •Tdisp time set register
- •Toff1 time set register
- •Toff2 time set register
- •Port P0FLD/port switch register
- •Port P2FLD/port switch register
- •Port P8FLD/port switch register
- •Port P8 FLD output control register
- •FLD automatic display RAM (max. 160 bytes)

A gradation display mode can be used for bright/dark display as a display function.

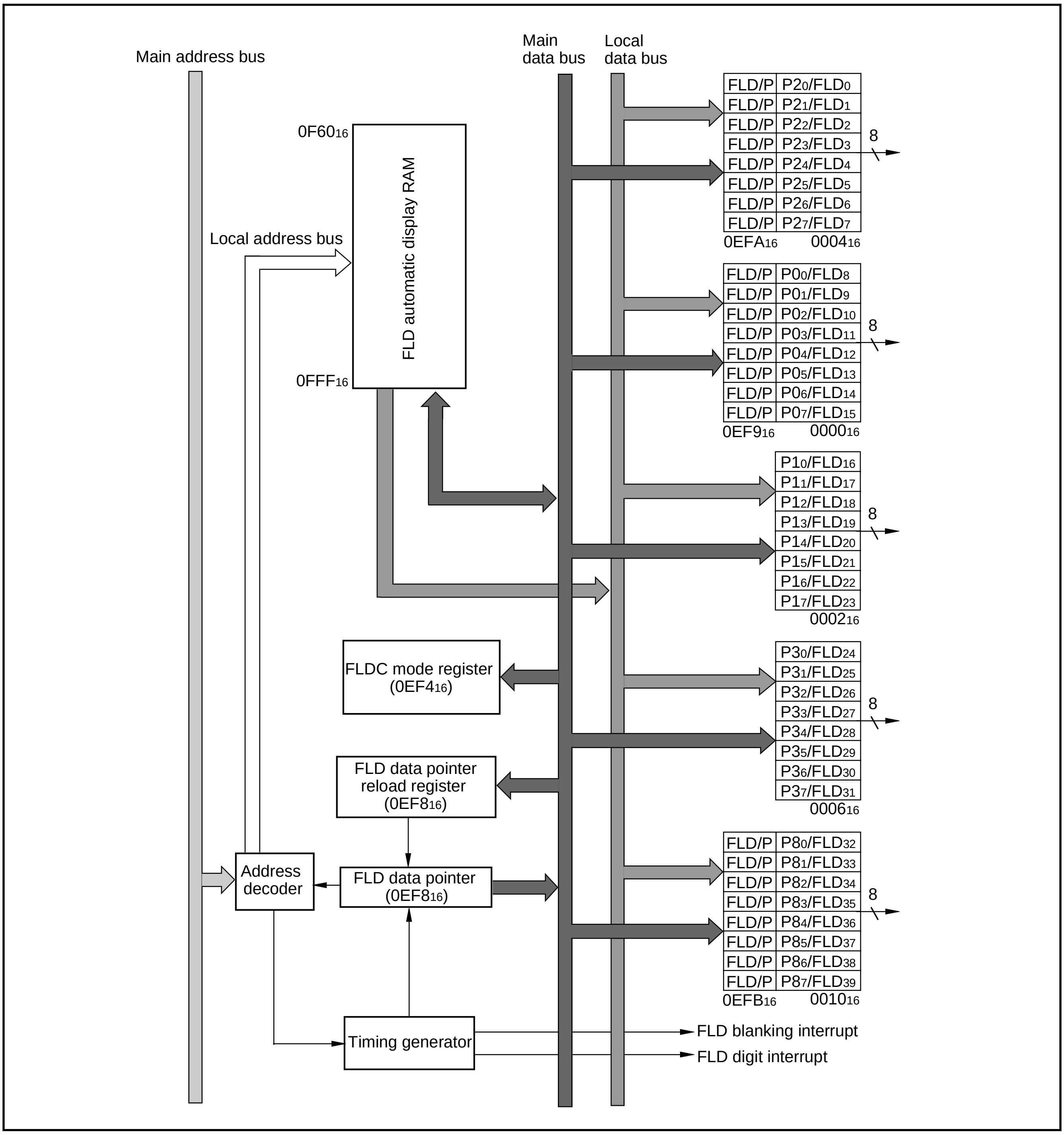
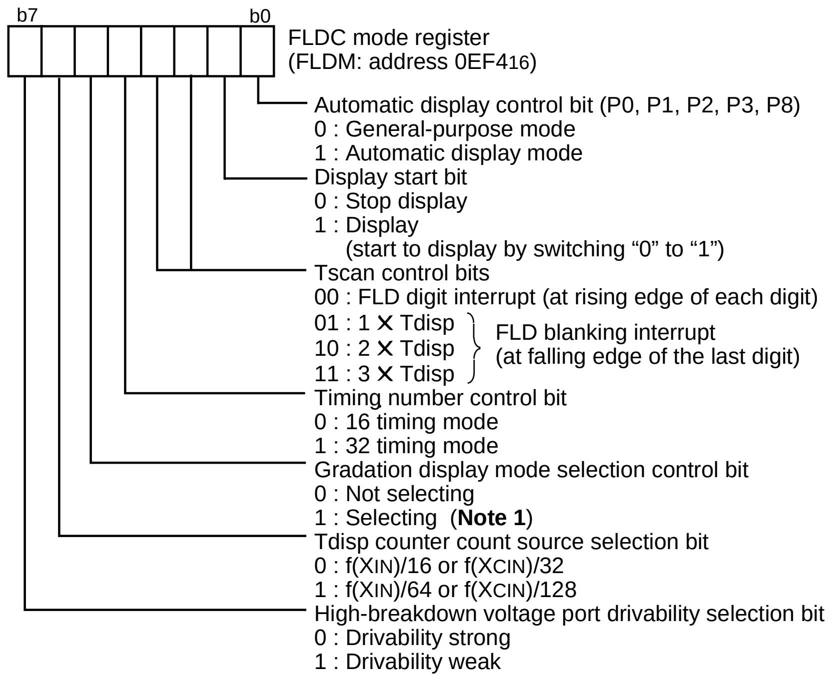


Fig. 42 Block diagram for FLD control circuit

[FLDC Mode Register] FLDM

The FLDC mode register is a 8-bit register respectively which is used to control the FLD automatic display and to set the blanking time Tscan for key-scan.



Notes 1: When a gradation display mode is selected, a number of timing is max. 16 timing. (Set the timing number control bit to “0”.)
2: When changing bit 4 (timing number control bit) or bit 5 (gradation display mode selection control bit), set “0” to bit 1 (display start bit) to perform at display stop state.

Fig. 43 Structure of FLDC mode register

FLD Automatic Display Pins

When the automatic display control bits of the FLDC mode register (address 0EF4$_{16}$) are set to “1,” the ports of P0, P1, P2, P3 and P8 are used as FLD automatic display pins.
When using the FLD automatic display mode, set each port to the FLD pin or the general-purpose port using the respective switch register in accordance with the number of segments and the number of digits.
This setting is performed by writing a value into the FLD/port switch register (addresses 0EF9$_{16}$ to 0EFB$_{16}$) of each port.
This setting can be performed in units of bit. When “0” is set, the port is set to the general-purpose port. When “1” is set, the port is set to the FLD pin. There is no restriction on whether the FLD pin is to be used as a segment pin or a digit pin.

Table 9 Pins in FLD automatic display mode

Port Name	Automatic Display Pins	Setting Method
P0, P2, P8$_0$–P8$_3$	FLD$_0$–FLD$_{15}$ FLD$_{32}$–FLD$_{35}$	The individual bits of the FLD/port switch register (addresses 0EF9$_{16}$–0EFB$_{16}$) can be set each pin either FLD port (“1”) or general-purpose port (“0”).
P1, P3	FLD$_{16}$–FLD$_{31}$	None (FLD only)
P8$_4$–P8$_7$	FLD$_{36}$–FLD$_{39}$	The individual bits of the FLD/port switch register (address 0EFB$_{16}$) can be set each pin to either FLD port (“1”) or general-purpose port (“0”). The output can be reversed by the port P8 FLD output control register (address 0EFC$_{16}$). The port output format is the CMOS output format. When using the port as a display pin, a driver must be installed externally.

	Setting example 1	Setting example 2	Setting example 3	Setting example 4
Number of segments	15	25	18	16
Number of digits	8	15	20	10
Port P2	0 P2$_0$	1 FLD$_0$(SEG$_1$)	0 P2$_0$	0 P2$_0$
	0 P2$_1$	1 FLD$_1$(SEG$_2$)	0 P2$_1$	0 P2$_1$
	0 P2$_2$	1 FLD$_2$(SEG$_3$)	1 FLD$_2$(SEG$_1$)	0 P2$_2$
	0 P2$_3$	1 FLD$_3$(SEG$_4$)	1 FLD$_3$(SEG$_2$)	0 P2$_3$
	0 P2$_4$	1 FLD$_4$(SEG$_5$)	1 FLD$_4$(SEG$_3$)	0 P2$_4$
	0 P2$_5$	1 FLD$_5$(SEG$_6$)	1 FLD$_5$(SEG$_4$)	0 P2$_5$
	0 P2$_6$	1 FLD$_6$(SEG$_7$)	1 FLD$_6$(SEG$_5$)	1 FLD$_4$(SEG$_1$)
	0 P2$_7$	1 FLD$_7$(SEG$_8$)	1 FLD$_7$(SEG$_6$)	1 FLD$_5$(SEG$_2$)
Port P0	1 FLD$_8$(SEG$_1$)	1 FLD$_8$(SEG$_9$)	1 FLD$_8$(DIG$_1$)	1 FLD$_6$(SEG$_3$)
	0 P0$_1$	1 FLD$_9$(SEG$_{10}$)	1 FLD$_9$(DIG$_2$)	1 FLD$_7$(SEG$_4$)
	0 P0$_2$	1 FLD$_{10}$(SEG$_{11}$)	1 FLD$_{10}$(DIG$_3$)	1 FLD$_8$(SEG$_5$)
	0 P0$_3$	1 FLD$_{11}$(SEG$_{12}$)	1 FLD$_{11}$(DIG$_4$)	1 FLD$_9$(SEG$_6$)
	0 P0$_4$	1 FLD$_{12}$(SEG$_{13}$)	1 FLD$_{12}$(DIG$_5$)	1 FLD$_{10}$(SEG$_7$)
	0 P0$_5$	1 FLD$_{13}$(SEG$_{14}$)	1 FLD$_{13}$(DIG$_6$)	1 FLD$_{11}$(SEG$_8$)
	1 FLD$_{14}$(SEG$_2$)	1 FLD$_{14}$(SEG$_{15}$)	1 FLD$_{14}$(DIG$_7$)	1 FLD$_{12}$(SEG$_9$)
	1 FLD$_{15}$(SEG$_3$)	1 FLD$_{15}$(SEG$_{16}$)	1 FLD$_{15}$(DIG$_8$)	1 FLD$_{13}$(SEG$_{10}$)
Port P1	FLD$_{16}$(DIG$_1$) 1	FLD$_{16}$(DIG$_1$) 1	FLD$_{16}$(DIG$_9$) 1	FLD$_{16}$(DIG$_1$) 1
	FLD$_{17}$(DIG$_2$) 1	FLD$_{17}$(DIG$_2$) 1	FLD$_{17}$(DIG$_{10}$) 1	FLD$_{17}$(DIG$_2$) 1
	FLD$_{18}$(DIG$_3$) 1	FLD$_{18}$(DIG$_3$) 1	FLD$_{18}$(DIG$_{11}$) 1	FLD$_{18}$(DIG$_3$) 1
	FLD$_{19}$(DIG$_4$) 1	FLD$_{19}$(DIG$_4$) 1	FLD$_{19}$(DIG$_{12}$) 1	FLD$_{19}$(DIG$_4$) 1
	FLD$_{20}$(SEG$_4$) 0	FLD$_{20}$(DIG$_5$) 1	FLD$_{20}$(DIG$_{13}$) 1	FLD$_{20}$(DIG$_5$) 1
	FLD$_{21}$(SEG$_5$) 0	FLD$_{21}$(DIG$_6$) 1	FLD$_{21}$(DIG$_{14}$) 1	FLD$_{21}$(DIG$_6$) 1
	FLD$_{22}$(SEG$_6$) 0	FLD$_{22}$(DIG$_7$) 1	FLD$_{22}$(DIG$_{15}$) 1	FLD$_{22}$(DIG$_7$) 1
	FLD$_{23}$(SEG$_7$) 0	FLD$_{23}$(DIG$_8$) 1	FLD$_{23}$(DIG$_{16}$) 1	FLD$_{23}$(DIG$_8$) 1
Port P3	FLD$_{24}$(SEG$_8$) 0	FLD$_{24}$(DIG$_9$) 1	FLD$_{24}$(DIG$_{17}$) 1	FLD$_{24}$(DIG$_9$) 1
	FLD$_{25}$(SEG$_9$) 0	FLD$_{25}$(DIG$_{10}$) 1	FLD$_{25}$(DIG$_{18}$) 1	FLD$_{25}$(DIG$_{10}$) 1
	FLD$_{26}$(SEG$_{10}$) 0	FLD$_{26}$(DIG$_{11}$) 1	FLD$_{26}$(DIG$_{19}$) 1	FLD$_{14}$(SEG$_{11}$) 0
	FLD$_{27}$(SEG$_{11}$) 0	FLD$_{27}$(DIG$_{12}$) 1	FLD$_{27}$(DIG$_{20}$) 1	FLD$_{15}$(SEG$_{12}$) 0
	FLD$_{28}$(DIG$_5$) 1	FLD$_{28}$(DIG$_{13}$) 1	FLD$_{28}$(SEG$_7$) 0	FLD$_{26}$(SEG$_{13}$) 0
	FLD$_{29}$(DIG$_6$) 1	FLD$_{29}$(DIG$_{14}$) 1	FLD$_{29}$(SEG$_8$) 0	FLD$_{27}$(SEG$_{14}$) 0
	FLD$_{30}$(DIG$_7$) 1	FLD$_{30}$(DIG$_{15}$) 1	FLD$_{30}$(SEG$_9$) 0	FLD$_{28}$(SEG$_{15}$) 0
	FLD$_{31}$(DIG$_8$) 1	FLD$_{31}$(SEG$_{17}$) 0	FLD$_{31}$(SEG$_{10}$) 0	FLD$_{29}$(SEG$_{16}$) 0
Port P8	1 FLD$_{32}$(SEG$_{12}$)	1 FLD$_{32}$(SEG$_{18}$)	1 FLD$_{32}$(SEG$_{11}$)	0 P8$_0$
	1 FLD$_{33}$(SEG$_{13}$)	1 FLD$_{33}$(SEG$_{19}$)	1 FLD$_{33}$(SEG$_{12}$)	0 P8$_1$
	1 FLD$_{34}$(SEG$_{14}$)	1 FLD$_{34}$(SEG$_{20}$)	1 FLD$_{34}$(SEG$_{13}$)	0 P8$_2$
	1 FLD$_{35}$(SEG$_{15}$)	1 FLD$_{35}$(SEG$_{21}$)	1 FLD$_{35}$(SEG$_{14}$)	0 P8$_3$
	0 P8$_4$	1 FLD$_{36}$(SEG$_{22}$)	1 FLD$_{36}$(SEG$_{15}$)	0 P8$_4$
	0 P8$_5$	1 FLD$_{37}$(SEG$_{23}$)	1 FLD$_{37}$(SEG$_{16}$)	0 P8$_5$
	0 P8$_6$	1 FLD$_{38}$(SEG$_{24}$)	1 FLD$_{38}$(SEG$_{17}$)	0 P8$_6$
	0 P8$_7$	1 FLD$_{39}$(SEG$_{25}$)	1 FLD$_{39}$(SEG$_{18}$)	0 P8$_7$

Value of FLD/port switch register

Value of FLDRAM write disable register

If data is set to “1”, data is protected. This setting does not decide the FLD port function (SEG/DIG).

Fig. 44 Segment/Digit setting example

FLD Automatic Display RAM

The FLD automatic display RAM uses the 160 bytes of addresses $0F60_{16}$ to $0FFF_{16}$. For FLD, the 3 modes of 16-timing ordinary mode, 16-timing•gradation display mode and 32-timing mode are available depending on the number of timings and the presence/absence of gradation display.

The automatic display RAM in each mode is as follows:

(1) 16-timing•ordinary mode

The 80 bytes of addresses $0FB0_{16}$ to $0FFF_{16}$ are used as a FLD display data store area. Because addresses $0F60_{16}$ to $0FAF_{16}$ are not used as the automatic display RAM, they can be the ordinary RAM or serial I/O automatic transfer RAM.

(2) 16-timing•gradation display mode

The 160 bytes of addresses $0F60_{16}$ to $0FFF_{16}$ are used. The 80 bytes of addresses $0FB0_{16}$ to $0FFF_{16}$ are used as an FLD display data store area, while the 80 bytes of addresses $0F60_{16}$ to $0FAF_{16}$ are used as a gradation display control data store area.

(3) 32-timing mode

The 160 bytes of addresses $0F60_{16}$ to $0FFF_{16}$ are used as an FLD display data store area.

[FLD Data Pointer and FLD Data Pointer Reload Register] FLDDP ($0EF8_{16}$)

Both the FLD data pointer and FLD data pointer reload register are 8-bit registers assigned at address $0EF8_{16}$. When writing data to this address, the data is written to the FLD data pointer reload register; when reading data from this address, the value in the FLD data pointer is read.

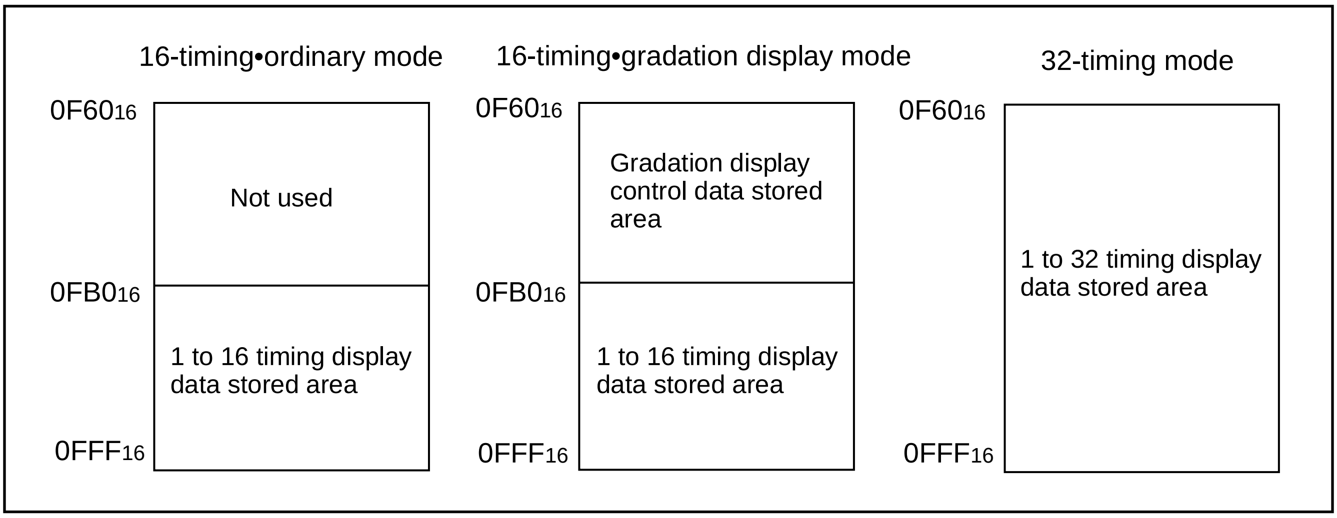


Fig. 45 FLD automatic display RAM assignment

Data Setup

(1) 16-timing•ordinary mode

The area of addresses 0FB0$_{16}$ to 0FFF$_{16}$ are used as a FLD automatic display RAM.

When data is stored in the FLD automatic display RAM, the last data of FLD port P2 is stored at address 0FB0$_{16}$, the last data of FLD port P0 is stored at address 0FC0$_{16}$, the last data of FLD port P1 is stored at address 0FD0$_{16}$, the last data of FLD port P3 is stored at address 0FE0$_{16}$, and the last data of FLD port P8 is stored at address 0FF0$_{16}$, to assign in sequence from the last data respectively.

The first data of the FLD port P2, P0, P1, P3, and P8 is stored at an address which adds the value of (the timing number – 1) to the corresponding address 0FB0$_{16}$, 0FC0$_{16}$, 0FD0$_{16}$, 0FE0$_{16}$, and 0FF0$_{16}$.

Set the FLD data pointer reload register to the value given by the timing number – 1. “1” is always written to bits 7, 6, and 5. Note that “0” is always read from bits 7, 6, and 5 when reading. “1” is always set to bit 4, but this bit become written value when reading.

(2) 16-timing•gradation display mode

Display data setting is performed in the same way as that of the 16-timing•ordinary mode. Gradation display control data is arranged at an address resulting from subtracting 0050$_{16}$ from the display data store address of each timing and pin. Bright display is performed by setting “0”, and dark display is performed by setting “1”.

Set the FLD data pointer reload register to the value given by the timing number – 1. “1” is always written to bits 7, 6, and 5. Note that “0” is always read from bits 7, 6, and 5 when reading. “1” is always set to bit 4, but this bit become written value when reading.

(3) 32-timing mode

The area of addresses 0F60$_{16}$ to 0FFF$_{16}$ are used as a FLD automatic display RAM. When data is stored in the FLD automatic display RAM, the last data of FLD port P2 is stored at address 0F60$_{16}$, the last data of FLD port P0 is stored at address 0F80$_{16}$, the last data of FLD port P1 is stored at address 0FA0$_{16}$, the last data of FLD port P3 is stored at address 0FC0$_{16}$, and the last data of FLD port P8 is stored at address 0FE0$_{16}$, to assign in sequence from the last data respectively.

The first data of the FLD port P2, P0, P1, P3, and P8 is stored at an address which adds the value of (the timing number – 1) to the corresponding address 0F60$_{16}$, 0F80$_{16}$, 0FA0$_{16}$, 0FC0$_{16}$, and 0FE0$_{16}$.

Set the FLD data pointer reload register to the value given by the timing number –1. “1” is always written to bits 7, 6, and 5. Note that “0” is always read from bits 7, 6, and 5 when reading.

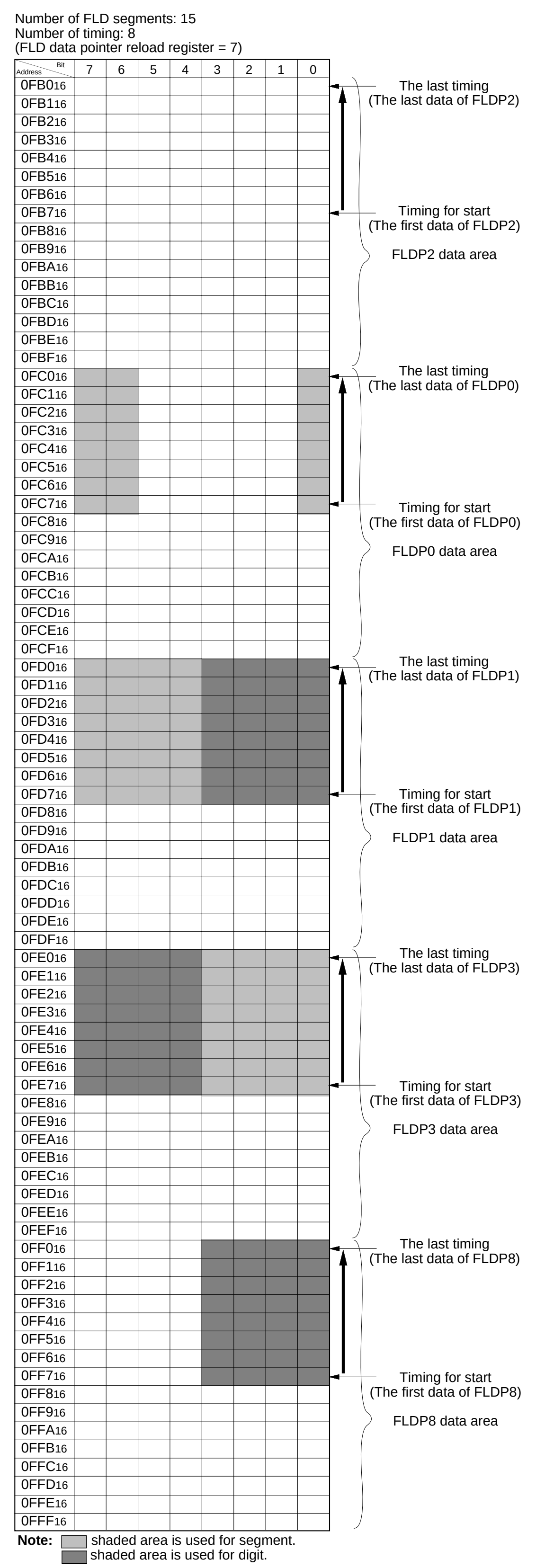


Fig. 46 Example of using FLD automatic display RAM in 16-timing•ordinary mode

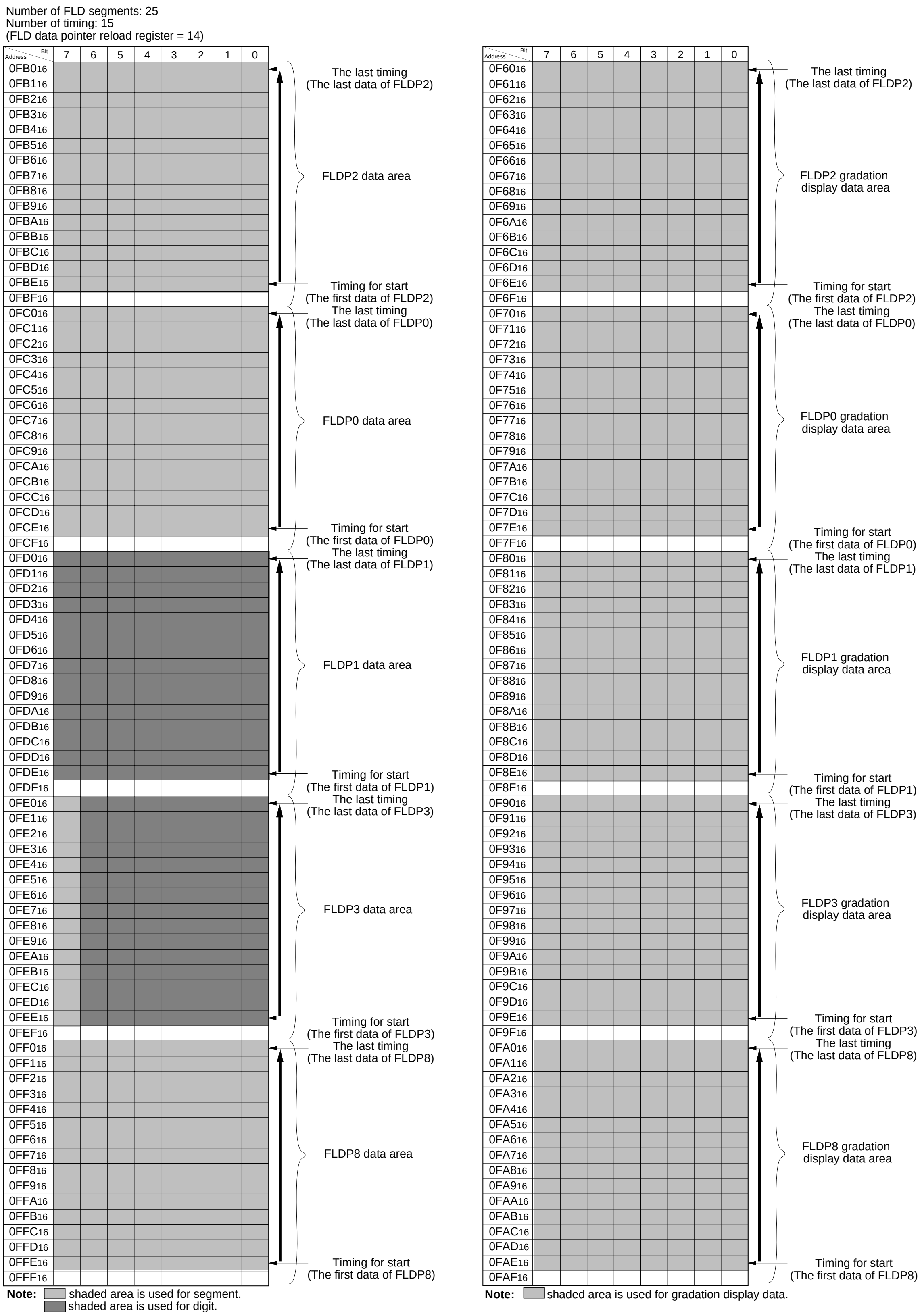


Fig. 47 Example of using FLD automatic display RAM in 16-timing•gradation display mode

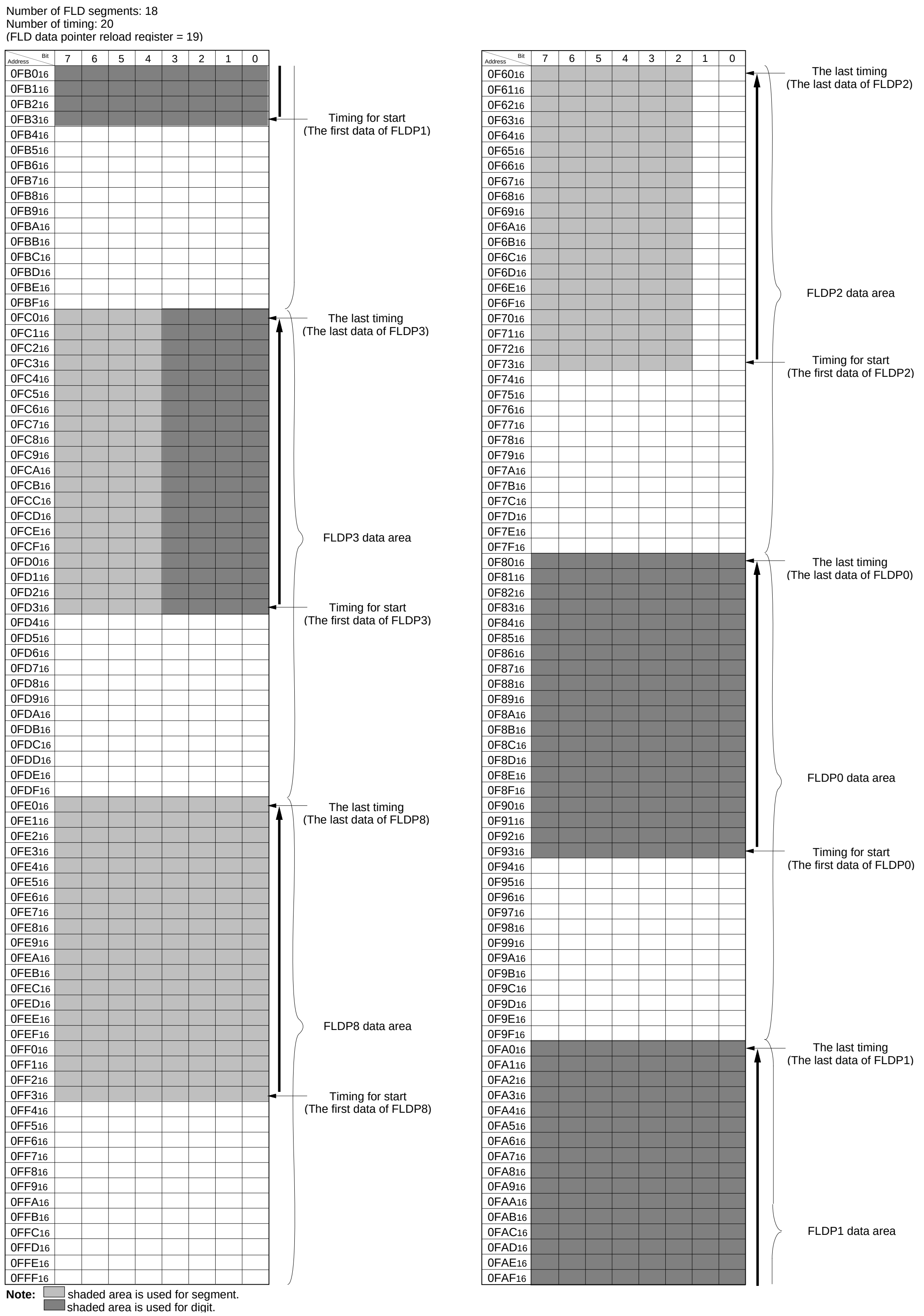


Fig. 48 Example of using FLD automatic display RAM in 32-timing mode

Setting Method When Using Grid Scan Type FLD

When using the grid scan type FLD, set “1” in the RAM area corresponding to the digit ports that output “1” at each timing. Set “0” in the RAM area corresponding to the other digit ports.

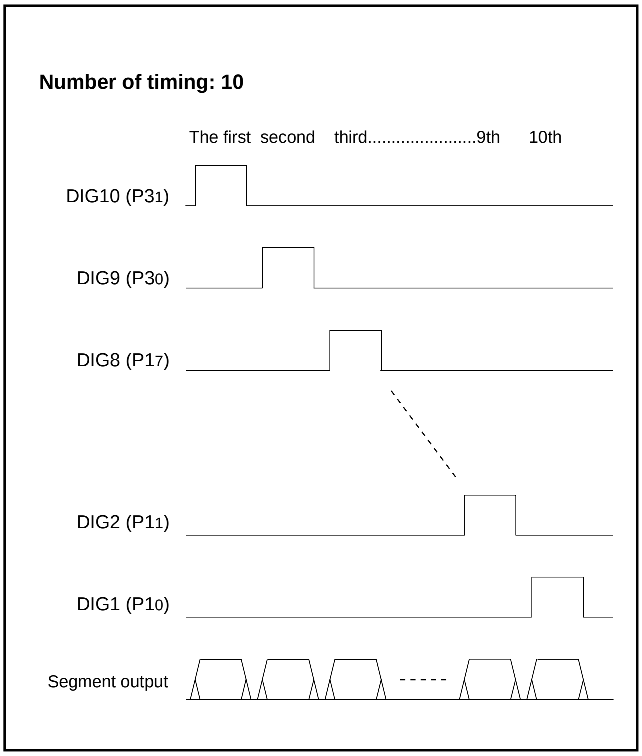


Fig. 49 Example of digit timing using grid scan type

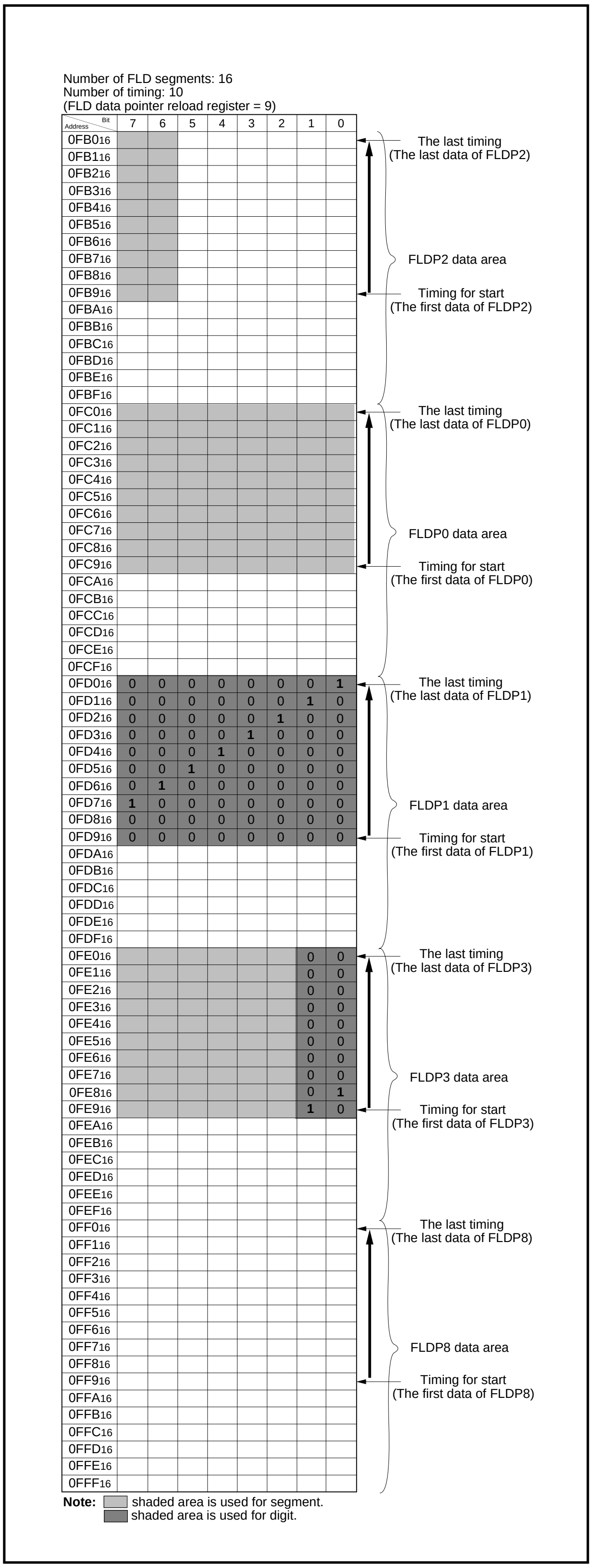


Fig. 50 Example of using FLD automatic display RAM using grid scan type

Timing Setting

Each timing is set by the FLDC mode register, Tdisp time set register, Toff1 time set register, and Toff2 time set register.

●**Tdisp time setting**

Set the Tdisp time by the Tdisp counter count source selection bit of the FLDC mode register and the Tdisp time set register. Supposing that the value of the Tdisp time set register is n, the Tdisp time is represented as Tdisp = (n+1) × t (t: count source synchronization).

When the Tdisp counter count source selection bit of the FLDC mode register is "0" and the value of the Tdisp time set register is 200 ($C8_{16}$), the Tdisp time is: Tdisp = (200+1) × 4 (at X_{IN}= 4 MHz) = 804 µs. When reading the Tdisp time set register, the value in the counter is read out.

●**Toff1 time setting**

Set the Toff1 time by the Toff1 time set register.

Supposing that the value of the Toff1 time set register is n1, the Toff1 time is represented as Toff1 = n1 × t.

When the Tdisp counter count source selection bit of the FLDC mode register is "0" and the value of the Toff1 time set register is 30 ($1E_{16}$), Toff1 = 30 × 4 (at X_{IN} = 4 MHz) = 120 µs.

Set a value of 03_{16} or more to the Toff1 time set register (address $0EF6_{16}$).

●**Toff2 time setting**

Set the Toff2 time by the Toff2 time set register.

Supposing that the value of the Toff2 time set register is n2, the Toff2 time is represented as Toff2 = n2 × t.

When the Tdisp counter count source selection bit of the FLDC mode register is "0" and the value of the Toff2 time set register is 180 ($B4_{16}$), Toff2 = 180 × 4 (at X_{IN} = 4 MHz) = 720 µs.

This Toff2 time setting is valid only for FLD ports which are in the gradation display mode and whose gradation display control RAM value is "1".

When setting "1" to bit 7 of the P8FLD output control register (address $0EFC_{16}$), set a value of 03_{16} or more to the Toff2 time set register (address $0EF7_{16}$).

FLD Automatic Display Start

To perform FLD automatic display, set the following registers.

•Port P0FLD/port switch register
•Port P2FLD/port switch register
•Port P8FLD/port switch register
•FLDC mode register
•Tdisp time set register
•Toff1 time set register
•Toff2 time set register
•FLD data pointer

FLD automatic display mode is selected by writing "1" to the bit 0 of the FLDC mode register (address $0EF4_{16}$), and the automatic display is started by writing "1" to bit 1. During FLD automatic display, bit 1 of the FLDC mode register (address $0EF4_{16}$) always keeps "1", and FLD automatic display can be interrupted by writing "0" to bit 1.

Key-scan

When a key-scan is performed with the segment during key-scan blanking period Tscan, take the following sequence:

1. Write "0" to bit 0 of the FLDC mode register (address $0EF4_{16}$).
2. Set the port corresponding to the segment for key-scan to the output port.
3. Perform the key-scan.
4. After the key-scan is performed, write "1" to bit 0 of FLDC mode register (address $0EF4_{16}$).

■ Note

When performing a key-scan according to the above step 1 to 4, take the following points into consideration.

1. Do not set "0" in bit 1 of the FLDC mode register (address $0EF4_{16}$).
2. Do not set "1" in the ports corresponding to digits.

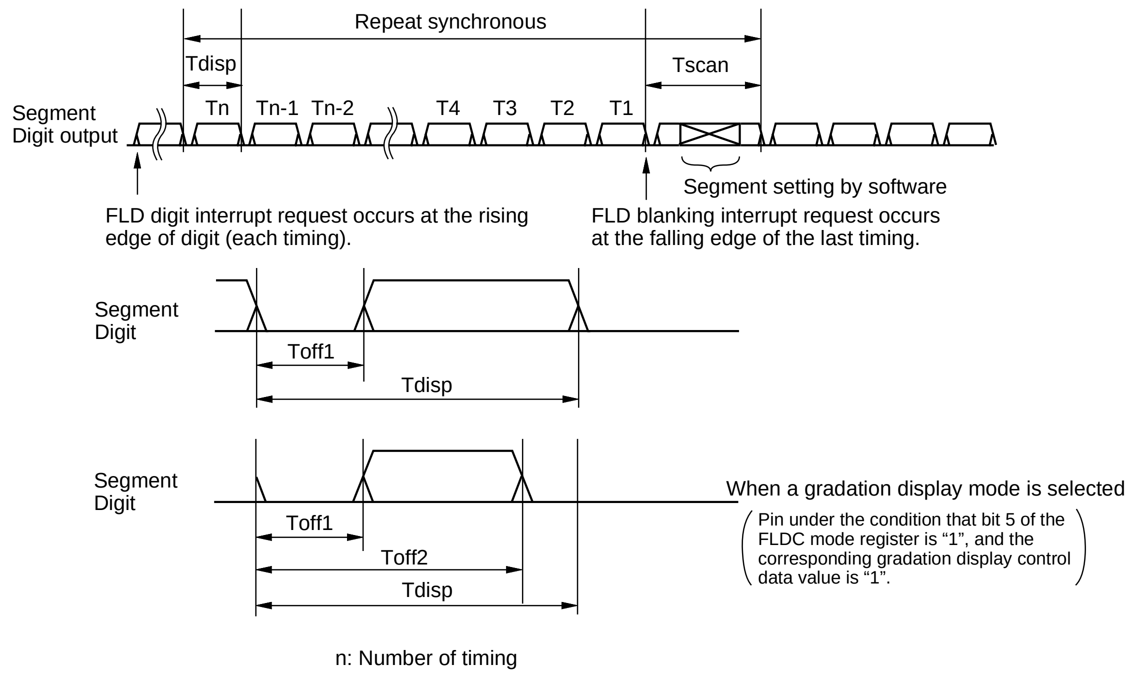


Fig. 51 FLDC timing

$P8_4$ to $P8_7$ FLD Output Reverse Function

$P8_4$ to $P8_7$ are provided with a function to reverse the polarity of the FLD output. This function is useful in adjusting the polarity when using an externally installed driver.
The output polarity can be reversed by setting “1” to bit 0 of the port P8 FLD output control register.

$P8_4$ to $P8_7$ Toff Invalid Function

$P8_4$ to $P8_7$ can output waveform in which Toff is invalid, when $P8_4$ to $P8_7$ is selected FLD ports (See Figure 52).
The function is useful when using a 4 bits →16 bits decoder. The Toff can be invalid by setting “1” to bit 2 of the port P8FLD output control register (address $0EFC_{16}$).

$P8_4$ to $P8_7$ Output Delay Function

$P8_4$ to $P8_7$ can output waveform in which is delayed for 16 µs, when selecting FLD port and selecting Toff invalid function (See Figure 52). When using a 4 bits →16 bits decoder, the function can be useful for prevention of leak radiation caused by phase discrepancy between segment output waveform and digit output waveform. This function can be set by setting “1” to bit 3 of the port P8FLD output control register (address $0EFC_{16}$).

Dimmer Signal Output Function

$P6_3$ can output the dimmer signal. When using a 4 bits →16 bits decoder, the dimmer signal can be used as a control signal for a 4 bits →16 bits decoder. When using M35501FP, the dimmer signal can be used as the CLK signal. The dimmer signal can be output by setting “1” to bit 4 of the port P8FLD output control register (address $0EFC_{16}$).

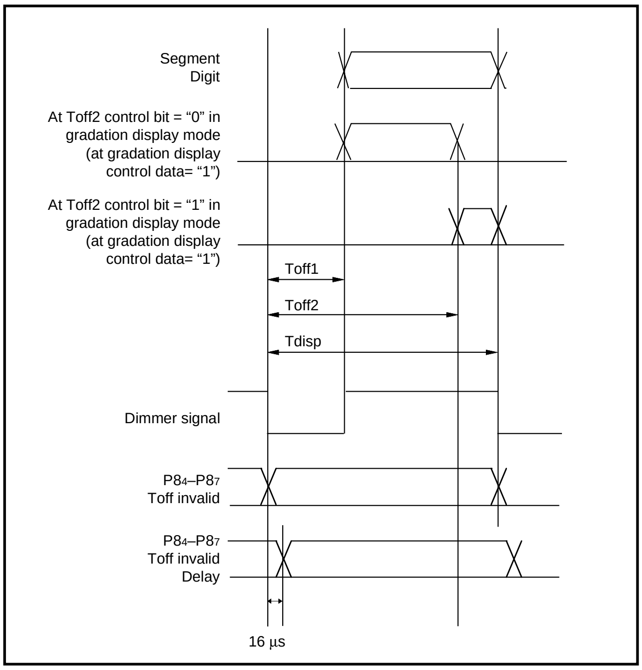


Fig. 52 $P8_4$ to $P8_7$ FLD output waveform

Toff2 Control Bit

The value of the Toff2 time set register is valid when gradation display mode is selected. The FLD ports output (set) the data of display RAM at the end of the Toff1 time and output “0” (reset) at the end of the Toff2 time, when bit 7 of the port P8FLD output control register is “0”.
The FLD ports output (set) the data of display RAM at the end of the Toff2 time and output “0” (reset) at the end of Tdisp time, when bit 7 of the port P8FLD output control register is “1”.

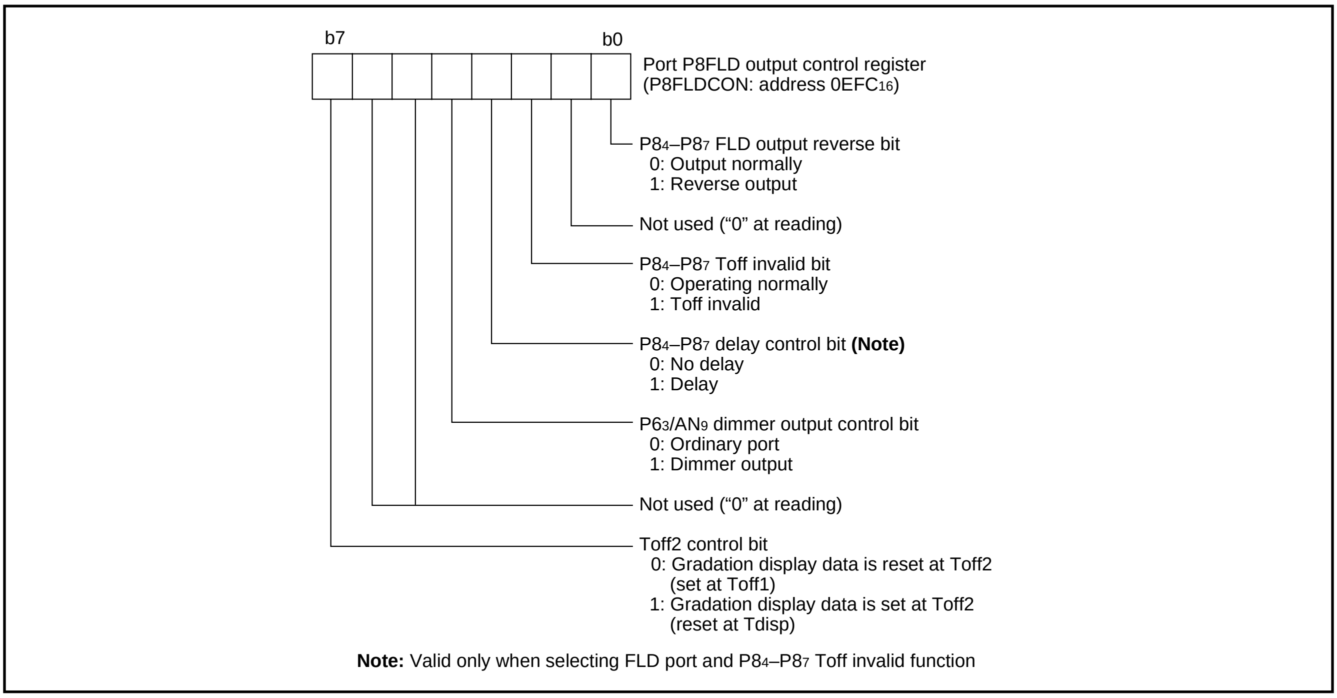


Fig. 53 Structure of port P8 FLD output control register

A-D CONVERTER

The 38B4 group has a 10-bit A-D converter. The A-D converter performs successive approximation conversion.

[A-D Conversion Register] AD

One of these registers is a high-order register, and the other is a low-order register. The high-order 8 bits of a conversion result is stored in the A-D conversion register (high-order) (address 0034_{16}), and the low-order 2 bits of the same result are stored in bit 7 and bit 6 of the A-D conversion register (low-order) (address 0033_{16}). During A-D conversion, do not read these registers.

[A-D Control Register] ADCON

This register controls A-D converter. Bits 3 to 0 are analog input pin selection bits. Bit 4 is an AD conversion completion bit and "0" during A-D conversion. This bit is set to "1" upon completion of A-D conversion.
A-D conversion is started by setting "0" in this bit.

[Comparison Voltage Generator]

The comparison voltage generator divides the voltage between AV_{SS} and V_{REF}, and outputs the divided voltages.

[Channel Selector]

The channel selector selects one of the input ports $P7_7/AN_7$–$P7_0/AN_0$, and $P6_5/S_{STB1}/AN_{11}$–$P6_2/S_{RDY1}/AN_8$ and inputs it to the comparator.
When port $P6_4$ is selected as an analog input pin, an external interrupt function (INT_4) is invalid.

[Comparator and Control Circuit]

The comparator and control circuit compares an analog input voltage with the comparison voltage and stores the result in the A-D conversion register. When an A-D conversion is completed, the control circuit sets the AD conversion completion bit and the AD conversion interrupt request bit to "1".
Note that the comparator is constructed linked to a capacitor, so set $f(X_{IN})$ to at least 250 kHz during A-D conversion. Use a CPU system clock dividing the main clock X_{IN} as the internal system clock.

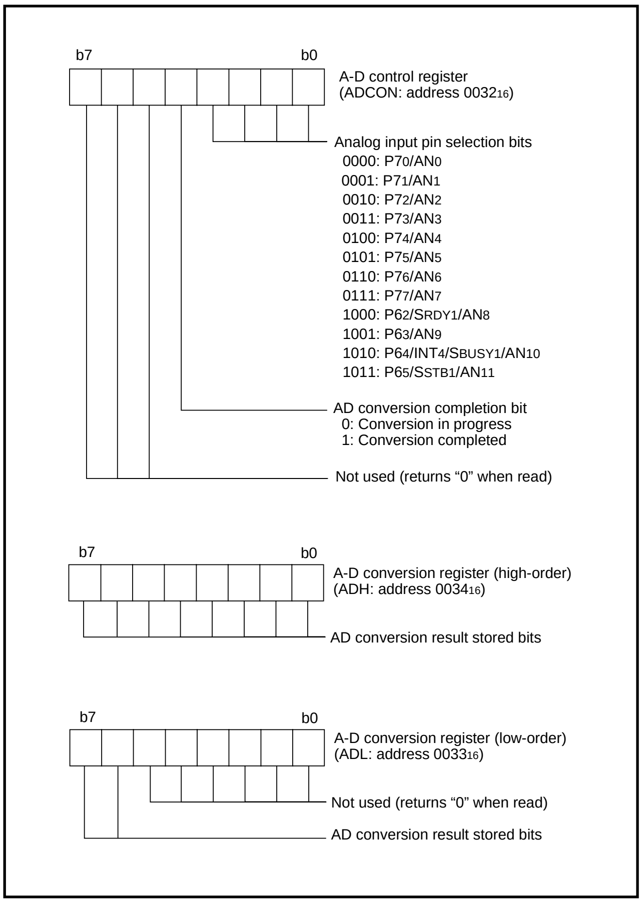


Fig. 54 Structure of A-D control register

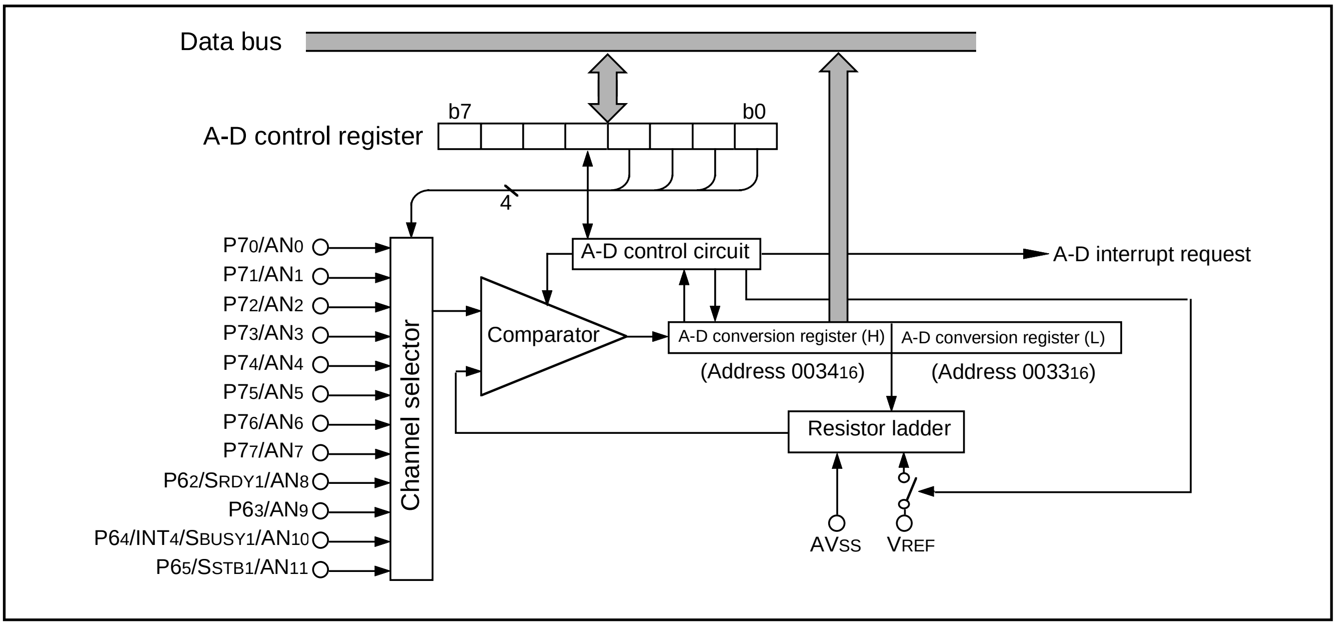


Fig. 55 Block diagram of A-D converter

PULSE WIDTH MODULATION (PWM)

The 38B4 group has a PWM function with a 14-bit resolution. When the oscillation frequency X_{IN} is 4 MHz, the minimum resolution bit width is 250 ns and the cycle period is 4096 µs. The PWM timing generator supplies a PWM control signal based on a signal that is the frequency of the X_{IN} clock.
The explanation in the rest assumes X_{IN} = 4 MHz.

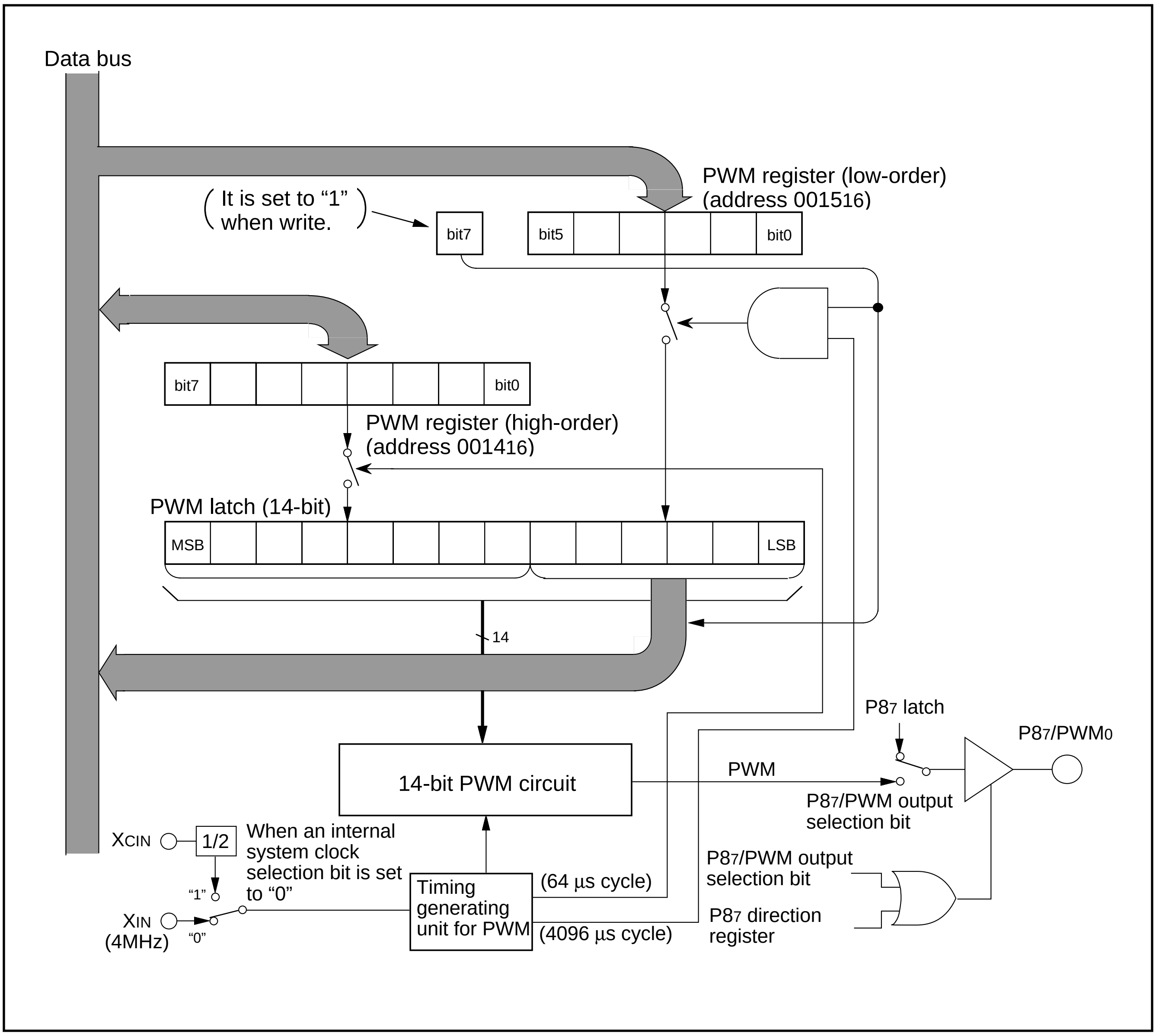


Fig. 56 PWM block diagram

Data Setup

The PWM output pin also function as port $P8_7$. Set port $P8_7$ to be the PWM output pin by setting bit 0 of the PWM control register (address 0026_{16}) to “1”. The high-order 8 bits of output data are set in the high-order PWM register PWMH (address 0014_{16}) and the low-order 6 bits are set in the low-order PWM register PWML (address 0015_{16}).

PWM Operation

The timing of the 14-bit PWM function is shown in Figure 57.
The 14-bit PWM data is divided into the low-order 6 bits and the high-order 8 bits in the PWM latch.
The high-order 8 bits of data determine how long an “H” level signal is output during each sub-period. There are 64 sub-periods in each period, and each sub-period t is 256 $\times$ τ (= 64 µs) long. The signal’s “H” has a length equal to N times τ, and its minimum resolution = 250 ns.
The last bit of the sub-period becomes the ADD bit which is specified either “H” or “L”, by the contents of PWML. As shown in Table 10, the ADD bit is decided either “H” or “L”.
That is, only in the sub-period tm shown in Table 10 in the PWM cycle period T = 64t, the “H” duration is lengthened during the minimum resolution width τ period in comparison with the other period.
For example, if the high-order eight bits of the 14-bit data are “03_{16}” and the low-order six bits are “05_{16}”, the length of the “H” level output in sub-periods t_8, t_{24}, t_{32}, t_{40} and t_{56} is 4 τ, and its length 3 τ in all other sub-periods.
Time at the “H” level of each sub-period almost becomes equal because the time becomes length set in the high-order 8 bits or becomes the value plus τ, and this sub-period t (= 64 µs, approximate 15.6 kHz) becomes cycle period approximately.

Transfer From Register To Latch

Data written to the PWML register is transferred to the PWM latch once in each PWM period (every 4096 µs), and data written to the PWMH register is transferred to the PWM latch once in each sub-period (every 64 µs). When the PWML register is read, the contents of the latch are read. However, bit 7 of the PWML register indicates whether the transfer to the PWM latch is completed; the transfer is completed when bit 7 is “0”.

Table 10 Relationship between low-order 6-bit data and setting period of ADD bit

Low-order 6-bit data	Sub-periods tm lengthened (m = 0 to 63)
0 0 0 0 0 0 (LSB)	None
0 0 0 0 0 1	m = 32
0 0 0 0 1 0	m = 16, 48
0 0 0 1 0 0	m = 8, 24, 40, 56
0 0 1 0 0 0	m = 4, 12, 20, 28, 36, 44, 52, 60
0 1 0 0 0 0	m = 2, 6, 10, 14, 18, 22, 26, 30, 34, 38, 42, 46, 50, 54, 58, 62
1 0 0 0 0 0	m = 1, 3, 5, 7, ..., 57, 59, 61, 63

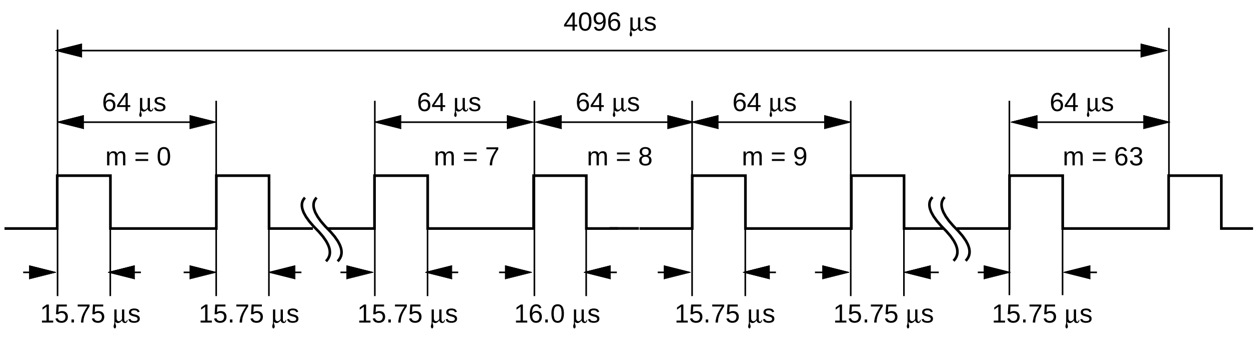


Fig. 57 PWM timing

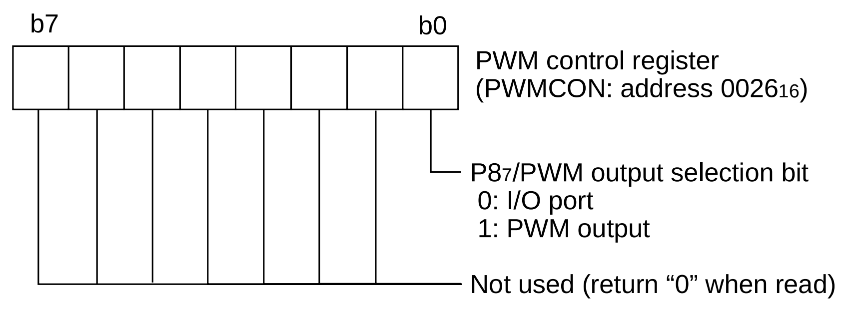


Fig. 58 Structure of PWM control register

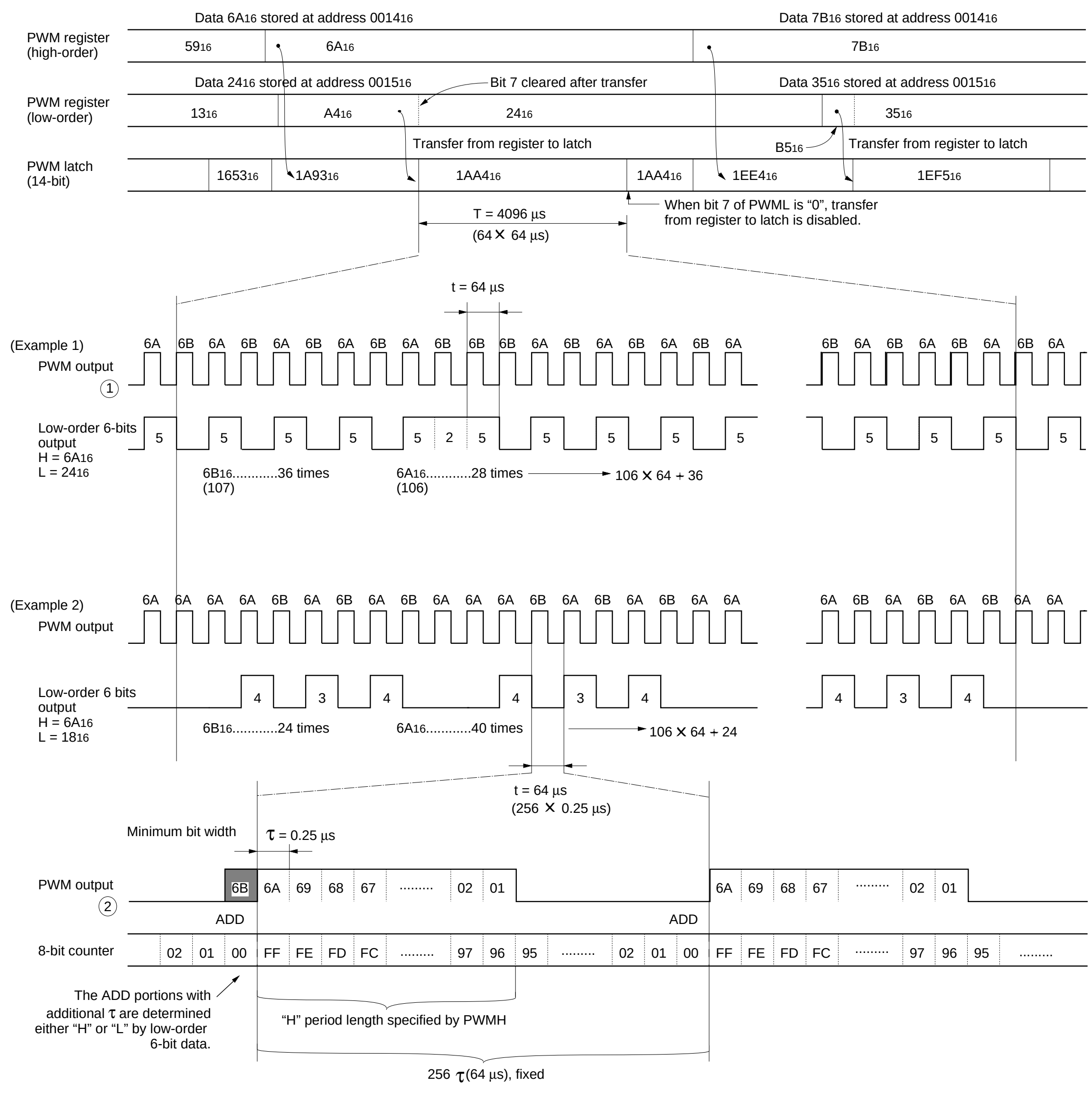


Fig. 59 14-bit PWM timing

INTERRUPT INTERVAL DETERMINATION FUNCTION

The 38B4 group has an interrupt interval determination circuit.
This interrupt interval determination circuit has an 8-bit binary up counter. Using this counter, it determines a duration of time from the rising edge (falling edge) of an input signal pulse on the $P4_7/INT_2$ pin to the rising edge (falling edge) of the signal pulse that is input next.
How to determine the interrupt interval is described below.

1. Enable the INT_2 interrupt by setting bit 2 of the interrupt control register 1 (address $003E_{16}$). Select the rising interval or falling interval by setting bit 2 of the interrupt edge selection register (address $003A_{16}$).
2. Set bit 0 of the interrupt interval determination control register (address 0031_{16}) to "1" (interrupt interval determination operating).
3. Select the sampling clock of 8-bit binary up counter by setting bit 1 of the interrupt interval determination control register. When writing "0", $f(X_{IN})/128$ is selected (the sampling interval: 32 µs at $f(X_{IN})$ = 4.19 MHz); when "1", $f(X_{IN})/256$ is selected (the sampling interval: 64 µs at $f(X_{IN})$ = 4.19 MHz).
4. When the signal of polarity which is set on the INT_2 pin (rising or falling edge) is input, the 8-bit binary up counter starts counting up of the selected counter sampling clock.
5. When the signal of polarity above 4 is input again, the value of the 8-bit binary up counter is transferred to the interrupt interval determination register (address 0030_{16}), and the remote control interrupt request occurs. Immediately after that, the 8-bit binary up counter continues to count up again from "00_{16}".
6. When count value reaches "FF_{16}", the 8-bit binary up counter stops counting up. Then, simultaneously when the next counter sampling clock is input, the counter sets value "FF_{16}" to the interrupt interval determination register to generate the counter overflow interrupt request.

Noise Filter

The $P4_7/INT_2$ pin builds in the noise filter.
The noise filter operation is described below.

1. Select the sampling clock of the input signal with bits 2 and 3 of the interrupt interval determination control register. When not using the noise filter, set "00".
2. The $P4_7/INT_2$ input signal is sampled in synchronization with the selected clock. When sampling the same level signal in a series of three sampling, the signal is recognized as the interrupt signal, and the interrupt request occurs.
   When setting bit 4 of interrupt interval determination control register to "1", the interrupt request can occur at both rising and falling edges.
   When using the noise filter, set the minimum pulse width of the INT_2 input signal to 3 cycles or more of the sample clock.

Note: In the low-speed mode (CM_7 = 1), the interrupt interval determination function cannot operate.

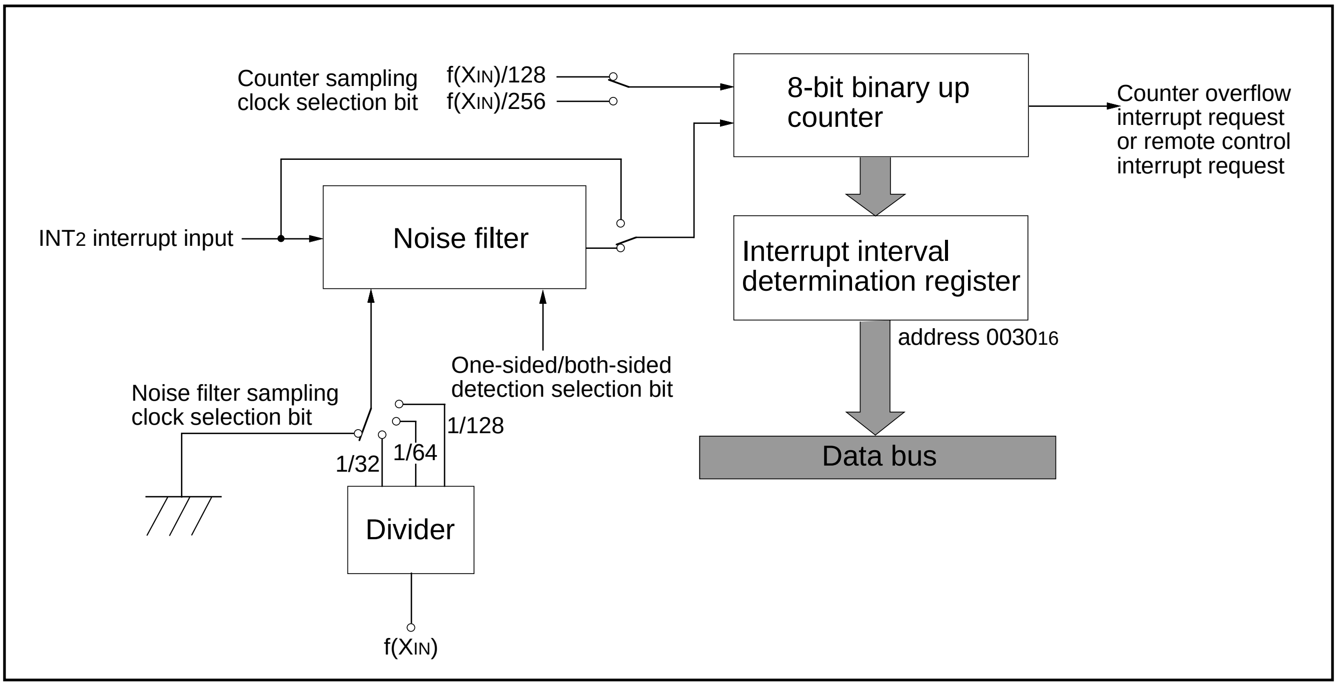


Fig. 60 Interrupt interval determination circuit block diagram

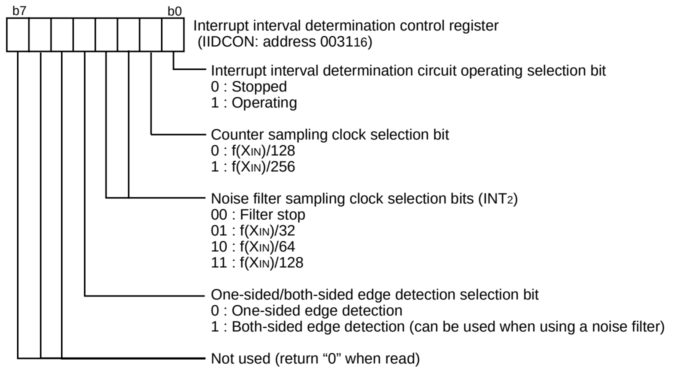


Fig. 61 Structure of interrupt interval determination control register

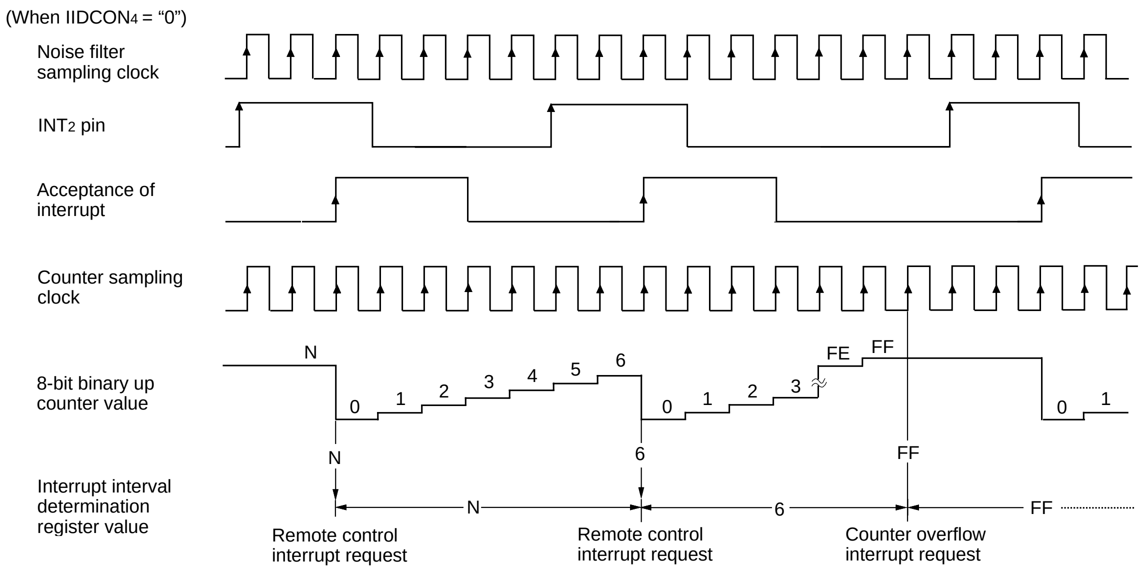


Fig. 62 Interrupt interval determination operation example (at rising edge active)

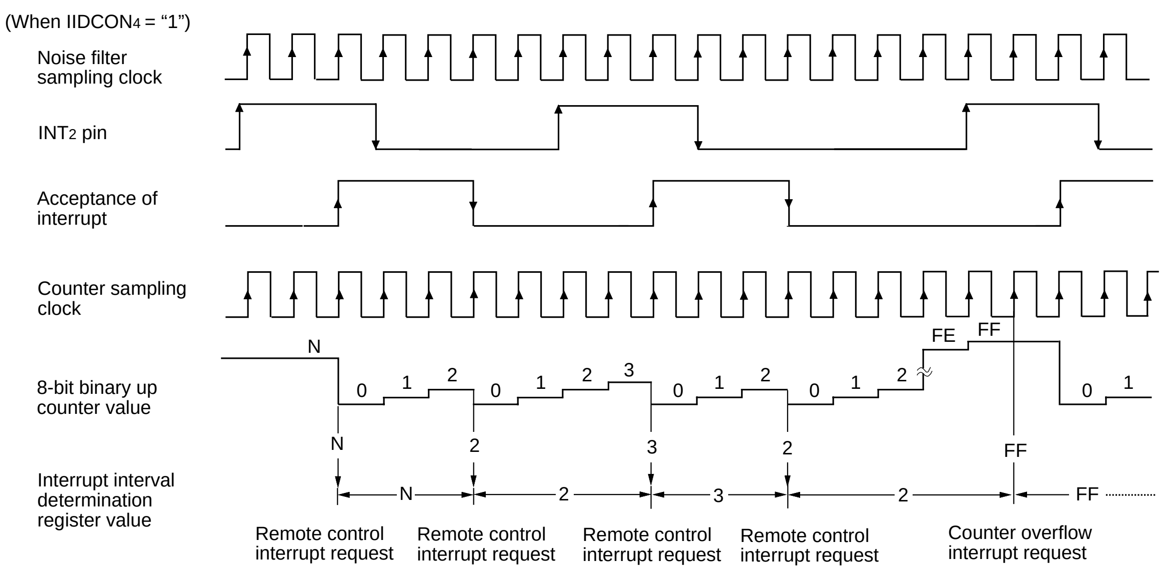


Fig. 63 Interrupt interval determination operation example (at both-sided edge active)

WATCHDOG TIMER

The watchdog timer gives a mean of returning to the reset status when a program cannot run on a normal loop (for example, because of a software runaway). The watchdog timer consists of an 8-bit watchdog timer L and a 12-bit watchdog timer H.

Standard Operation Of Watchdog Timer

When any data is not written into the watchdog timer control register (address $002B_{16}$) after resetting, the watchdog timer is in the stop state. The watchdog timer starts to count down by writing an optional value into the watchdog timer control register (address $002B_{16}$) and an internal reset occurs at an underflow of the watchdog timer H.
Accordingly, programming is usually performed so that writing to the watchdog timer control register (address $002B_{16}$) may be started before an underflow. When the watchdog timer control register (address $002B_{16}$) is read, the values of the high-order 6 bits of the watchdog timer H, STP instruction disable bit, and watchdog timer H count source selection bit are read.

●Initial value of watchdog timer

At reset or writing to the watchdog timer control register (address $002B_{16}$), a watchdog timer H is set to "FFF_{16}" and a watchdog timer L to "FF_{16}".

●Watchdog timer H count source selection bit operation

Bit 7 of the watchdog timer control register (address $002B_{16}$) permits selecting a watchdog timer H count source. When this bit is set to "0", the underflow signal of watchdog timer L becomes the count source. The detection time is set then to f(XIN) = 2.1 s at 4 MHz frequency and f(XCIN) = 512 s at 32 kHz frequency.
When this bit is set to "1", the count source becomes the signal divided by 8 for f(XIN) (or divided by 16 for f(XCIN)). The detection time in this case is set to f(XIN) = 8.2 ms at 4 MHz frequency and f(XCIN) = 2 s at 32 KHz frequency. This bit is cleared to "0" after resetting.

●Operation of STP instruction disable bit

Bit 6 of the watchdog timer control register (address $002B_{16}$) permits disabling the STP instruction when the watchdog timer is in operation.
When this bit is "0", the STP instruction is enabled.
When this bit is "1", the STP instruction is disabled.
Once the STP instruction is executed, an internal resetting occurs.
When this bit is set to "1", it cannot be rewritten to "0" by program.
This bit is cleared to "0" after resetting.

■ Note

When releasing the stop mode, the watchdog timer performs its count operation even in the stop release waiting time. Be careful not to cause the watchdog timer H to underflow in the stop release waiting time, for example, by writing data in the watchdog timer control register (address $002B_{16}$) before executing the STP instruction.

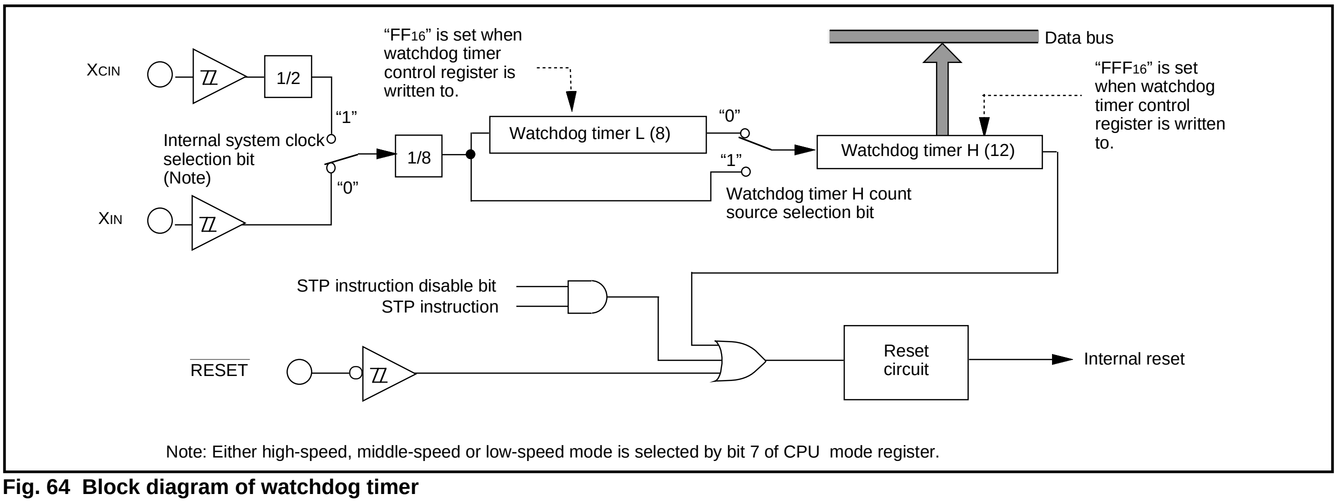


Fig. 64 Block diagram of watchdog timer

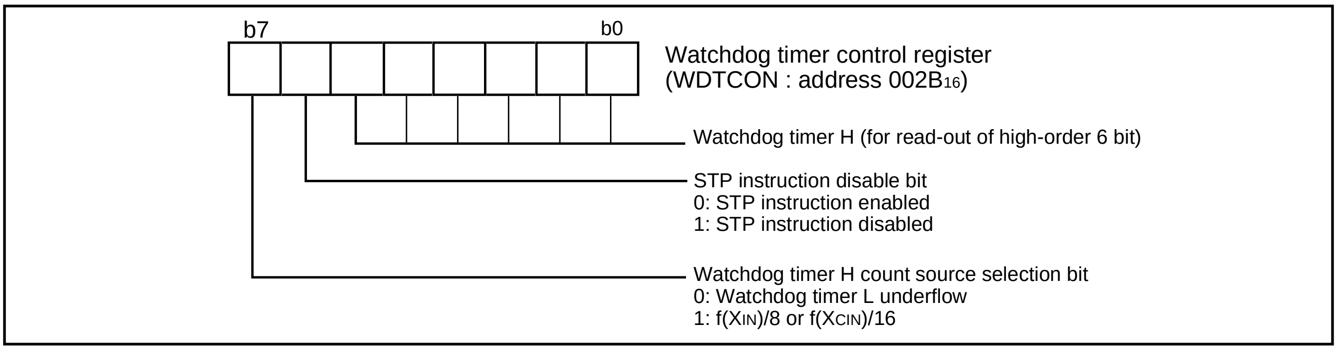


Fig. 65 Structure of watchdog timer control register

BUZZER OUTPUT CIRCUIT

The 38B4 group has a buzzer output circuit. One of 1 kHz, 2 kHz and 4 kHz (at X_{IN} = 4.19 MHz) frequencies can be selected by the buzzer output control register (address $0EFD_{16}$). Either $P4_3/B_{UZ01}$ or $P2_0/B_{UZ02}/FLD_0$ can be selected as a buzzer output port by the output port selection bits (b2 and b3 of address $0EFD_{16}$).
The buzzer output is controlled by the buzzer output ON/OFF bit (b4).

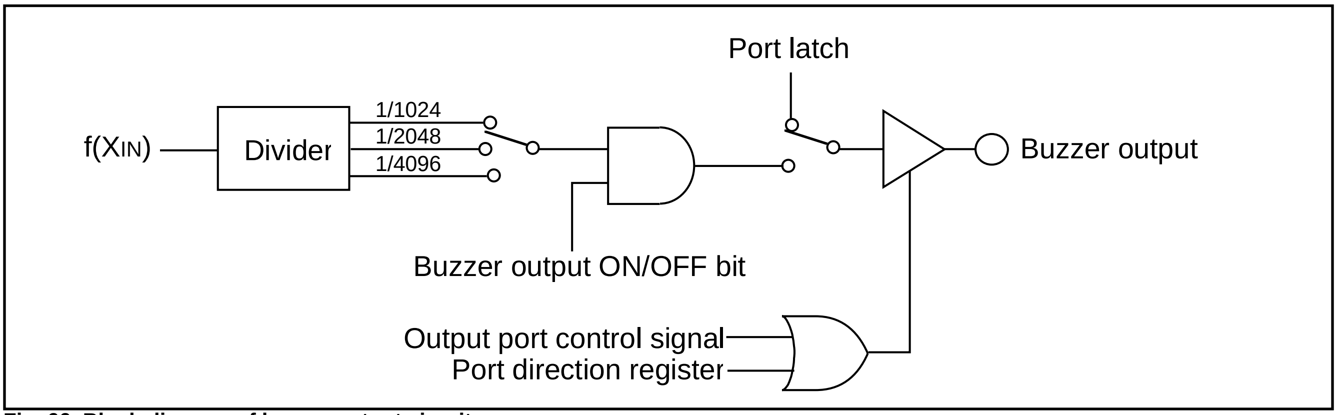


Fig. 66 Block diagram of buzzer output circuit

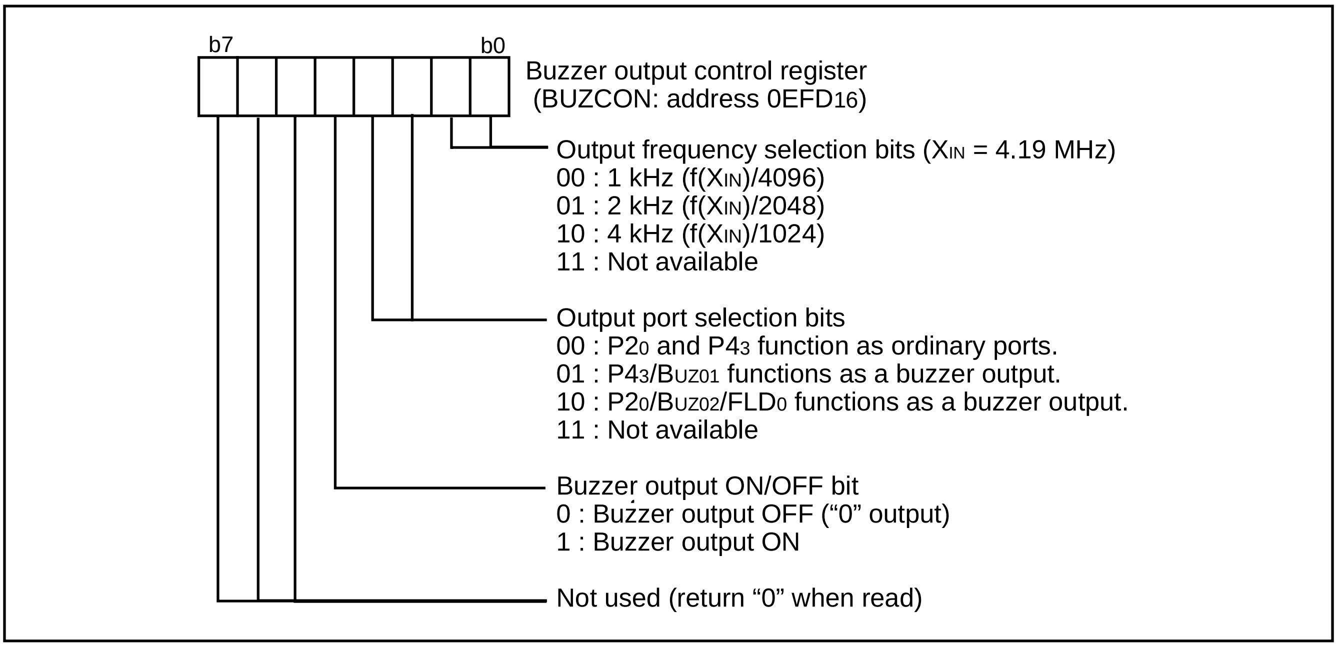


Fig. 67 Structure of buzzer output control register

RESET CIRCUIT

To reset the microcomputer, $\overline{\text{RESET}}$ pin should be held at an “L” level for 2 µs or more. Then the $\overline{\text{RESET}}$ pin is returned to an “H” level (the power source voltage should be between 2.7 V and 5.5 V, and the oscillation should be stable), reset is released. After the reset is completed, the program starts from the address contained in address $FFFD_{16}$ (high-order byte) and address $FFFC_{16}$ (low-order byte). Make sure that the reset input voltage is less than 0.5 V for V_{CC} of 2.7 V (switching to the high-speed mode, a power source voltage must be between 4.0 V and 5.5 V).

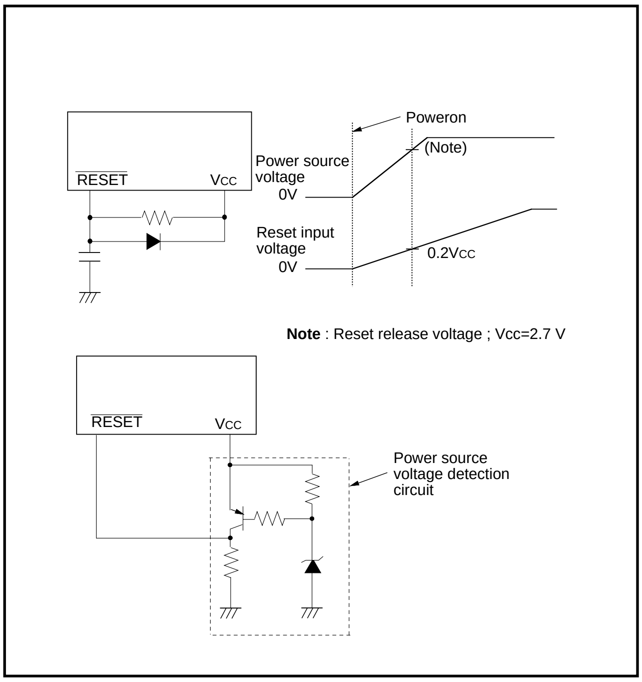


Fig. 68 Reset circuit example

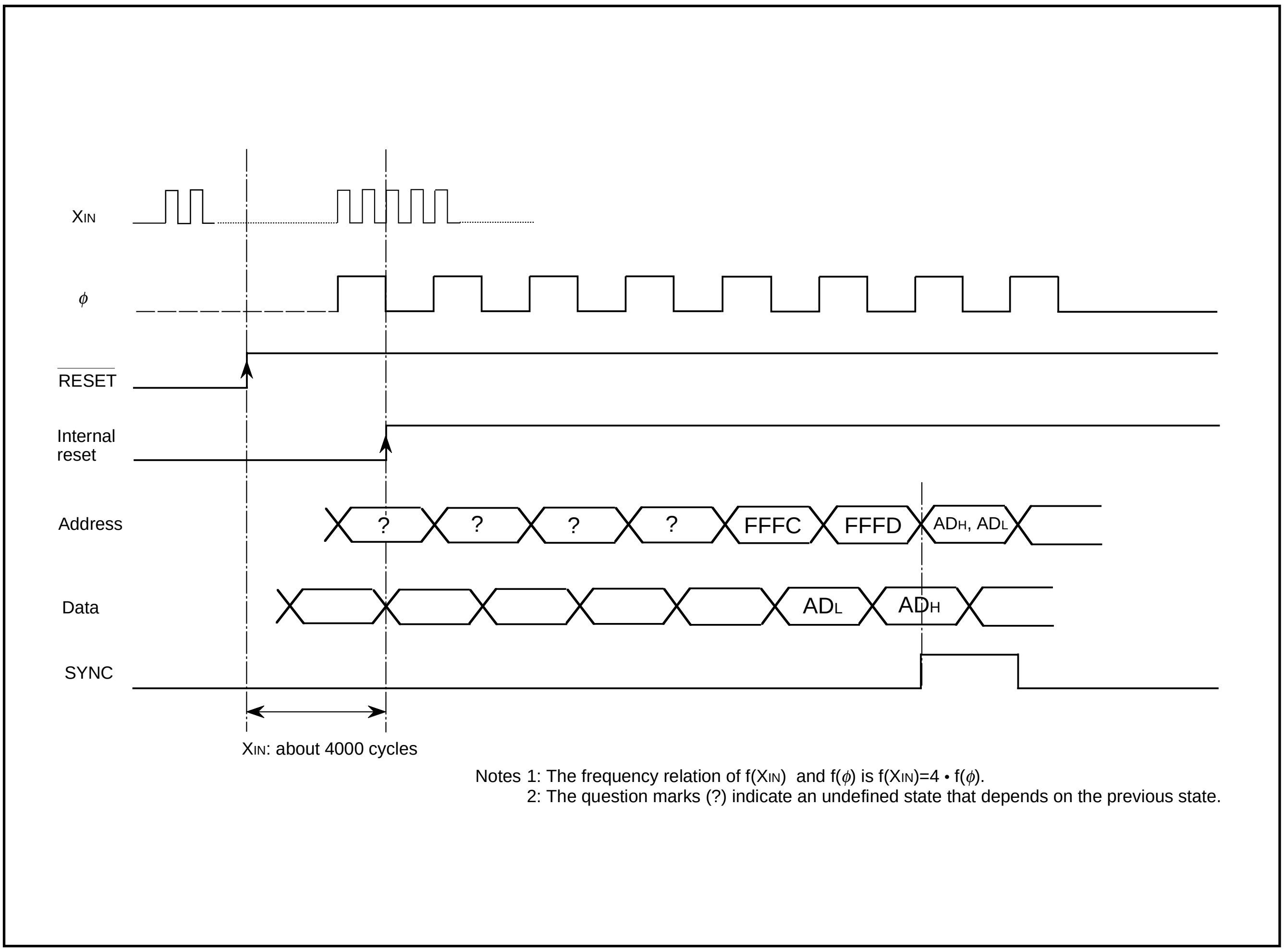


Fig. 69 Reset sequence

	Address	Register contents
(1) Port P0	0000_{16}	00_{16}
(2) Port P0 direction register	0001_{16}	00_{16}
(3) Port P1	0002_{16}	00_{16}
(4) Port P2	0004_{16}	00_{16}
(5) Port P2 direction register	0005_{16}	00_{16}
(6) Port P3	0006_{16}	00_{16}
(7) Port P4	0008_{16}	00_{16}
(8) Port P4 direction register	0009_{16}	00_{16}
(9) Port P5	$000A_{16}$	00_{16}
(10) Port P5 direction register	$000B_{16}$	00_{16}
(11) Port P6	$000C_{16}$	00_{16}
(12) Port P6 direction register	$000D_{16}$	00_{16}
(13) Port P7	$000E_{16}$	00_{16}
(14) Port P7 direction register	$000F_{16}$	00_{16}
(15) Port P8	0010_{16}	00_{16}
(16) Port P8 direction register	0011_{16}	00_{16}
(17) Port P9	0012_{16}	00_{16}
(18) Port P9 direction register	0013_{16}	00_{16}
(19) UART control register	0017_{16}	80_{16}
(20) Serial I/O1 control register 1	0019_{16}	00_{16}
(21) Serial I/O1 control register 2	$001A_{16}$	00_{16}
(22) Serial I/O1 control register 3	$001C_{16}$	00_{16}
(23) Serial I/O2 control register	$001D_{16}$	00_{16}
(24) Serial I/O2 status register	$001E_{16}$	80_{16}
(25) Timer 1	0020_{16}	FF_{16}
(26) Timer 2	0021_{16}	01_{16}
(27) Timer 3	0022_{16}	FF_{16}
(28) Timer 4	0023_{16}	FF_{16}
(29) Timer 5	0024_{16}	FF_{16}
(30) Timer 6	0025_{16}	FF_{16}
(31) PWM control register	0026_{16}	00_{16}
(32) Timer 12 mode register	0028_{16}	00_{16}

	Address	Register contents
(33) Timer 34 mode register	0029_{16}	00_{16}
(34) Timer 56 mode register	$002A_{16}$	00_{16}
(35) Watchdog timer control register	$002B_{16}$	$3F_{16}$
(36) Timer X (low-order)	$002C_{16}$	FF_{16}
(37) Timer X (high-order)	$002D_{16}$	FF_{16}
(38) Timer X mode register 1	$002E_{16}$	00_{16}
(39) Timer X mode register 2	$002F_{16}$	00_{16}
(40) Interrupt interval determination control register	0031_{16}	00_{16}
(41) A-D control register	0032_{16}	10_{16}
(42) Interrupt source switch register	0039_{16}	00_{16}
(43) Interrupt edge selection register	$003A_{16}$	00_{16}
(44) CPU mode register	$003B_{16}$	0 1 0 0 1 0 0 0
(45) Interrupt request register 1	$003C_{16}$	00_{16}
(46) Interrupt request register 2	$003D_{16}$	00_{16}
(47) Interrupt control register 1	$003E_{16}$	00_{16}
(48) Interrupt control register 2	$003F_{16}$	00_{16}
(49) Pull-up control register 1	$0EF0_{16}$	00_{16}
(50) Pull-up control register 2	$0EF1_{16}$	00_{16}
(51) FLDC mode register	$0EF4_{16}$	00_{16}
(52) Tdisp time set register	$0EF5_{16}$	00_{16}
(53) Toff1 time set register	$0EF6_{16}$	FF_{16}
(54) Toff2 time set register	$0EF7_{16}$	FF_{16}
(55) Port P0FLD/port switch register	$0EF9_{16}$	00_{16}
(56) Port P2FLD/port switch register	$0EFA_{16}$	00_{16}
(57) Port P8FLD/port switch register	$0EFB_{16}$	00_{16}
(58) Port P8FLD output control register	$0EFC_{16}$	00_{16}
(59) Buzzer output control register	$0EFD_{16}$	00_{16}
(60) Processor status register	(PS)	× × × × × 1 × ×
(61) Program counter	(PC_H)	$FFFD_{16}$ contents
	(PC_L)	$FFFC_{16}$ contents

×: Not fixed
Since the initial values for other than above mentioned registers and RAM contents are indefinite at reset, they must be set.

Fig. 70 Internal status at reset

CLOCK GENERATING CIRCUIT

The 38B4 group has two built-in oscillation circuits. An oscillation circuit can be formed by connecting a resonator between X_{IN} and X_{OUT} (X_{CIN} and X_{COUT}). Use the circuit constants in accordance with the resonator manufacturer's recommended values. No external resistor is needed between X_{IN} and X_{OUT} since a feedback resistor exists on-chip. However, an external feedback resistor is needed between X_{CIN} and X_{COUT}.
Immediately after power on, only the X_{IN} oscillation circuit starts oscillating, and X_{CIN} and X_{COUT} pins function as I/O ports.

Frequency Control

(1) Middle-speed mode
The internal system clock is the frequency of X_{IN} divided by 4. After reset, this mode is selected.

(2) High-speed mode
The internal system clock is the frequency of X_{IN}.

(3) Low-speed mode
The internal system clock is the frequency of X_{CIN} divided by 2.

■Note
If you switch the mode between middle/high-speed and low-speed, stabilize both X_{IN} and X_{CIN} oscillations. The sufficient time is required for the sub clock to stabilize, especially immediately after power on and at returning from stop mode. When switching the mode between middle/high-speed and low-speed, set the frequency on condition that $f(X_{IN}) > 3f(X_{CIN})$.

(4) Low power consumption mode
The low power consumption operation can be realized by stopping the main clock X_{IN} in low-speed mode. To stop the main clock, set bit 5 of the CPU mode register to "1". When the main clock X_{IN} is restarted (by setting the main clock stop bit to "0"), set enough time for oscillation to stabilize.
By clearing furthermore the X_{COUT} drivability selection bit (b3) of CPU mode register to "0", low power consumption operation of less than 200 µA ($f(X_{CIN})$ = 32 kHz) can be realized by reducing the drivability between X_{CIN} and X_{COUT}. At reset or during STP instruction execution this bit is set to "1" and a strong drivability that has an easy oscillation start is set.

Oscillation Control

(1) Stop mode
If the STP instruction is executed, the internal system clock stops at an "H" level, and X_{IN} and X_{CIN} oscillators stop. Timer 1 is set to "FF_{16}" and timer 2 is set to "01_{16}".
Either X_{IN} divided by 8 or X_{CIN} divided by 16 is input to timer 1 as count source, and the output of timer 1 is connected to timer 2. The bits of the timer 12 mode register are cleared to "0". Set the interrupt enable bits of the timer 1 and timer 2 to disabled ("0") before executing the STP instruction. Oscillator restarts when an external interrupt is received or reset, but the internal system clock is not supplied to the CPU until timer 1 underflows. This allows time for the clock circuit oscillation to stabilize.

(2) Wait mode
If the WIT instruction is executed, the internal system clock stops at an "H" level. The states of X_{IN} and X_{CIN} are the same as the state before executing the WIT instruction. The internal system clock restarts at reset or when an interrupt is received. Since the oscillator does not stop, normal operation can be started immediately after the clock is restarted.

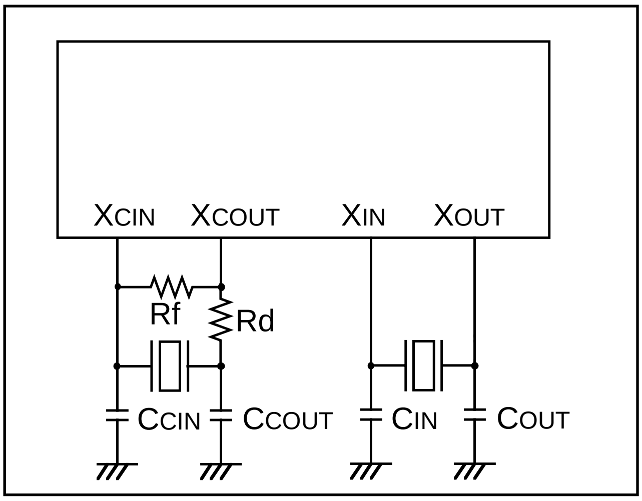


Fig. 71 Ceramic resonator circuit

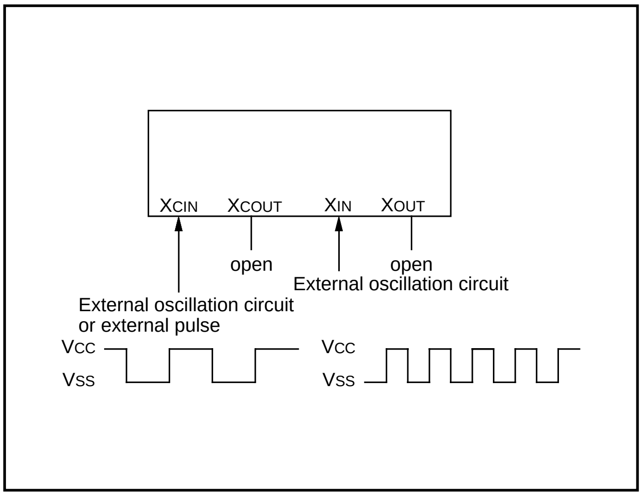
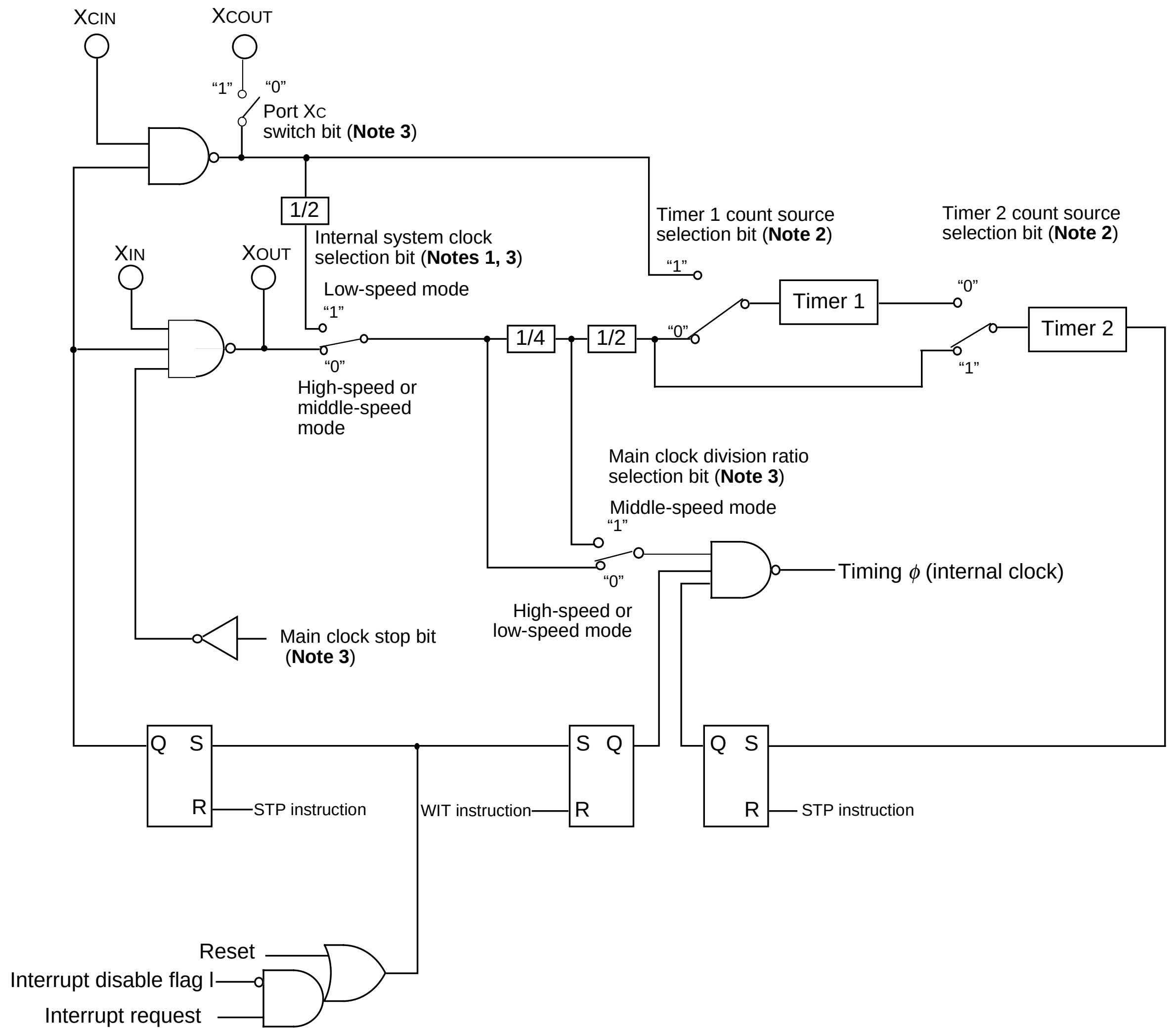
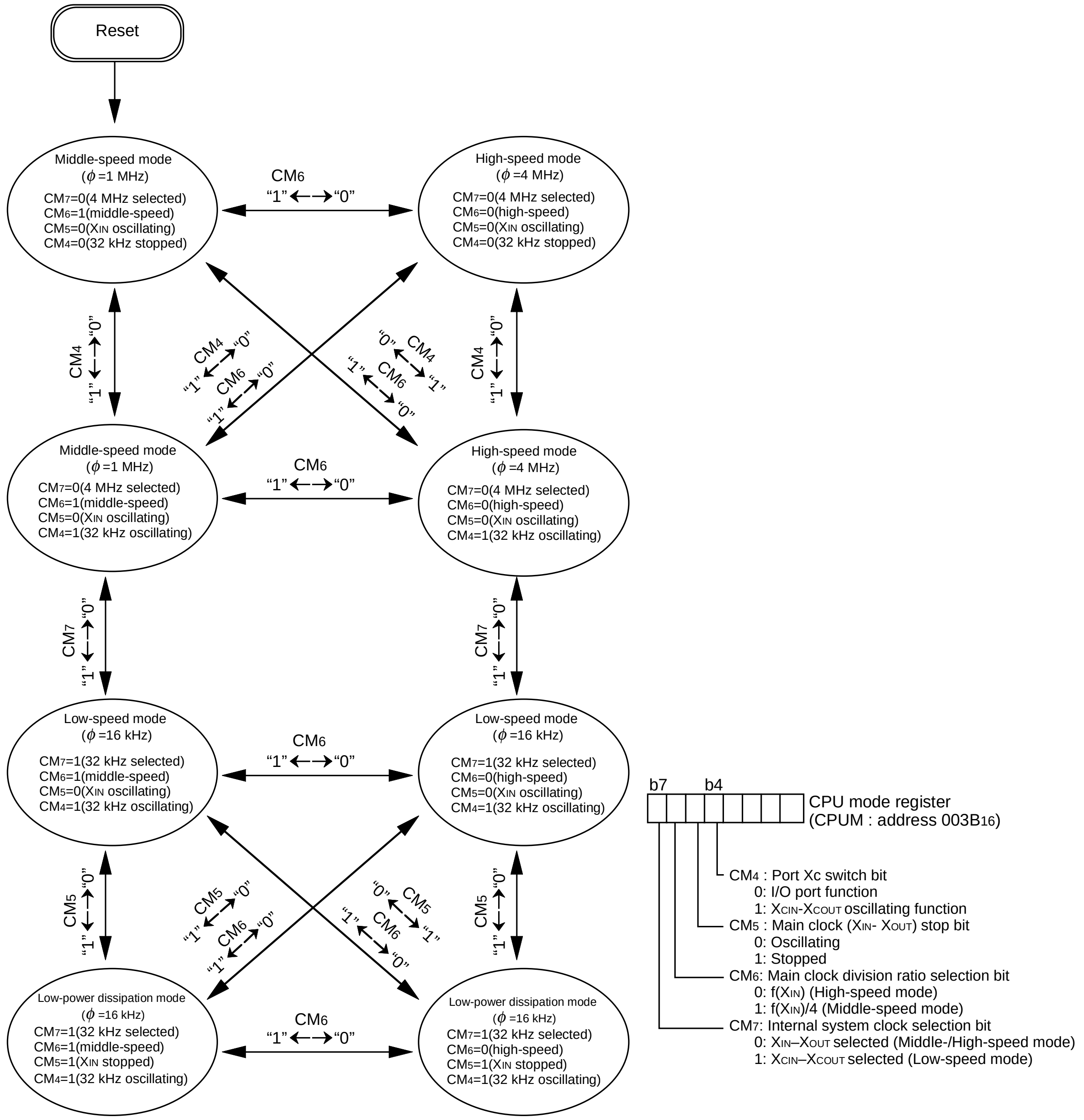


Fig. 72 External clock input circuit



Notes 1: When low-speed mode is selected, set the port Xc switch bit (b4) to "1".
2: Refer to the structure of the timer 12 mode register.
3: Refer to the structure of the CPU mode register.

Fig. 73 Clock generating circuit block diagram



Notes 1: Switch the mode by the allows shown between the mode blocks. (Do not switch between the mode directly without an allow.)
2: The all modes can be switched to the stop mode or the wait mode and return to the source mode when the stop mode or the wait mode is ended.
3: Timer operates in the wait mode.
4: When the stop mode is ended, a delay of approximately 1 ms occurs by Timer 1 in middle-/high-speed mode.
5: When the stop mode is ended, a delay of approximately 0.25 s occurs by Timer 1 in low-speed mode.
6: The example assumes that 4 MHz is being applied to the X_{IN} pin and 32 kHz to the X_{CIN} pin. ϕ indicates the internal system clock.

Fig. 74 State transitions of system clock

NOTES ON PROGRAMMING

Processor Status Register

The contents of the processor status register (PS) after a reset are undefined, except for the interrupt disable flag (I) which is “1”. After a reset, initialize flags which affect program execution. In particular, it is essential to initialize the index X mode (T) and the decimal mode (D) flags because of their effect on calculations.

Interrupts

The contents of the interrupt request bits do not change immediately after they have been written. After writing to an interrupt request register, execute at least one instruction before performing a BBC or BBS instruction.

Decimal Calculations

•To calculate in decimal notation, set the decimal mode flag (D) to “1”, then execute an ADC or SBC instruction. Only the ADC and SBC instructions yield proper decimal results. After executing an ADC or SBC instruction, execute at least one instruction before executing a SEC, CLC, or CLD instruction.
•In decimal mode, the values of the negative (N), overflow (V), and zero (Z) flags are invalid.

Timers

If a value n (between 0 and 255) is written to a timer latch, the frequency division ratio is 1/(n+1).

Multiplication and Division Instructions

•The index X mode (T) and the decimal mode (D) flags do not affect the MUL and DIV instruction.
•The execution of these instructions does not change the contents of the processor status register.

Ports

The contents of the port direction registers cannot be read. The following cannot be used:
•The data transfer instruction (LDA, etc.)
•The operation instruction when the index X mode flag (T) is “1”
•The addressing mode which uses the value of a direction register as an index
•The bit-test instruction (BBC or BBS, etc.) to a direction register
•The read-modify-write instructions (ROR, CLB, or SEB, etc.) to a direction register.
Use instructions such as LDM and STA, etc., to set the port direction registers.

Serial I/O

•Using an external clock
When using an external clock, input “H” to the external clock input pin and clear the serial I/O interrupt request bit before executing serial I/O transfer and serial I/O automatic transfer.
•Using an internal clock
When using an internal clock, set the synchronous clock to the internal clock, then clear the serial I/O interrupt request bit before executing a serial I/O transfer and serial I/O automatic transfer.

Automatic Transfer Serial I/O

When using the automatic transfer serial I/O mode of the serial I/O1, set an automatic transfer interval as the following.
Otherwise the serial data might be incorrectly transmitted/received.

•Set an automatic transfer interval for each 1-byte data transfer as the following:
(1) Not using FLD controller
Keep the interval for **5 cycles or more of internal system clock** from clock rising of the last bit of 1-byte data.

(2) Using FLD controller
(a) Not using gradation display
Keep the interval for **12 cycles or more of internal system clock** from clock rising of the last bit of 1-byte data.
(b) Using gradation display
Keep the interval for **18 cycles or more of internal system clock** from clock rising of the last bit of 1-byte data.

A-D Converter

The comparator uses internal capacitors whose charge will be lost if the clock frequency is too low.
Therefore, make sure that $f(X_{IN})$ is at least on 250 kHz during an A-D conversion.
Do not execute the STP or WIT instruction during an A-D conversion.

Instruction Execution Time

The instruction execution time is obtained by multiplying the frequency of the internal system clock by the number of cycles needed to execute an instruction.
The number of cycles required to execute an instruction is shown in the list of machine instructions.
The frequency of the internal system clock is the same of the X_{IN} frequency in high-speed mode.

At STP Instruction Release

At the STP instruction release, all bits of the timer 12 mode register are cleared.
The X_{COUT} drivability selection bit (the CPU mode register) is set to “1” (high drive) in order to start oscillating.

DATA REQUIRED FOR MASK ORDERS

The following are necessary when ordering a mask ROM production:
(1) Mask ROM Order Confirmation Form
(2) Mark Specification Form
(3) Data to be written to ROM, in EPROM form (three identical copies)

MASK OPTION OF PULL-DOWN RESISTOR
(object product: M38B4XMXH-XXXXFP)

Whether built-in pull-down resistors are connected or not to high-breakdown voltage ports $P2_0$ to $P2_7$ and $P8_0$ to $P8_3$ can be specified in ordering mask ROM. The option type can be specified from among 8 types; A to G, P as shown Table 11.

Table 11 Mask option type of pull-down resistor

Option type	Connective port of pull-down resistor (connected at “1” writing)												Restriction
	$P2_0$	$P2_1$	$P2_2$	$P2_3$	$P2_4$	$P2_5$	$P2_6$	$P2_7$	$P8_0$	$P8_1$	$P8_2$	$P8_3$	
A ($41)													
B ($42)							1	1					
C ($43)					1	1	1	1					
D ($44)			1	1	1	1	1	1					
E ($45)	1	1	1	1	1	1	1	1					
F ($46)	1	1	1	1	1	1	1	1	1	1			
G ($47)	1	1	1	1	1	1	1	1	1	1	1	1	
P ($50)	1	1	1	1	1	1	1	1					**(Note 4)**

Notes 1: The electrical characteristics of high-breakdown voltage ports $P2_0$ to $P2_7$ and $P8_0$ to $P8_3$’s built-in pull-down resistors are the same as that of high-breakdown voltage ports $P0_0$ to $P0_7$.

2: The absolute maximum ratings of power dissipation may be exceed owing to the number of built-in pull-down resistor. After calculating the power dissipation, specify the option type.

3: One time PROM version and EPROM version cannot be specified whether built-in pull-down resistors are connected or not likewise option type A.

4: <u>INT_3 function and $CNTR_1$ function cannot be used in the option type P.</u>

Power Dissipation Calculating Method

●Fixed number depending on microcomputer’s standard

- V_{OH} output fall voltage of high-breakdown port
  2 V (max.); | Current value | = at 18 mA
- Resistor value 43 V / 900 µA = 48 kΩ (min.)
- Power dissipation of internal circuit (CPU, ROM, RAM etc.) = 5 V ✕ 15 mA = 75 mW

●Fixed number depending on use condition

- Apply voltage to V_{EE} pin: Vcc – 45 V
- Timing number a; digit number b; segment number c
- Ratio of Toff time corresponding Tdisp time: 1/16
- Turn ON segment number during repeat cycle: d
- All segment number during repeat cycle: e (= a ✕ c)
- Total number of built-in resistor: for digit; f, for segment; g
- Digit pin current value h (mA)
- Segment pin current value i (mA)

(1) Digit pin power dissipation
{h ✕ b ✕ (1–Toff/Tdisp) ✕ voltage} / a

(2) Segment pin power dissipation
{i ✕ d ✕ (1–Toff/Tdisp) ✕ voltage} / a

(3) Pull-down resistor power dissipation (digit)
{power dissipation per 1 digit ✕ (b ✕ f / b) ✕ (1–Toff/Tdisp) } / a

(4) Pull-down resistor power dissipation (segment)
{power dissipation per 1 segment ✕ (d ✕ g / c) ✕ (1–Toff/Tdisp) } / a

(5) Internal circuit power dissipation (CPU, ROM, RAM etc.) = 75 mW

(1) + (2)+ (3) + (4) + (5) = <u>X mW</u>

Power Dissipation Calculating Example 1

●Fixed number depending on microcomputer’s standard

- V_{OH} output fall voltage of high-breakdown port
  2 V (max.); | Current value | = at 18 mA
- Resistor value 43 V / 900 µA = 48 kΩ (min.)
- Power dissipation of internal circuit (CPU, ROM, RAM etc.) = 5 V ✕ 15 mA = 75 mW

●Fixed number depending on use condition

- Apply voltage to V_{EE} pin: Vcc – 45 V
- Timing number 17; digit number 16; segment number 20
- Ratio of Toff time corresponding Tdisp time: 1/16
- Turn ON segment number during repeat cycle: 31
- All segment number during repeat cycle: 340 (= 17 ✕ 20)
- Total number of built-in resistor: for digit; 16, for segment; 20
- Digit pin current value: 18 (mA)
- Segment pin current value: 3 (mA)

(1) Digit pin power dissipation
{18 ✕ 16 ✕ (1–1/16) ✕ 2} / 17 = 31.77 mW

(2) Segment pin power dissipation
{3 ✕ 31 ✕ (1–1/16) ✕ 2} / 17 = 10.26 mW

(3) Pull-down resistor power dissipation (digit)
$(45 – 2)^2$ /48 ✕ (16 ✕ 16/16) ✕ (1 – 1/16) / 17 = 33.99 mW

(4) Pull-down resistor power dissipation (segment)
$(45 – 2)^2$ /48 ✕ (31 ✕ 20/20) ✕ (1 – 1/16) / 17 = 65.86 mW

(5) Internal circuit power dissipation (CPU, ROM, RAM etc.) = 75 mW

(1) + (2)+ (3) + (4) + (5) = <u>217 mW</u>

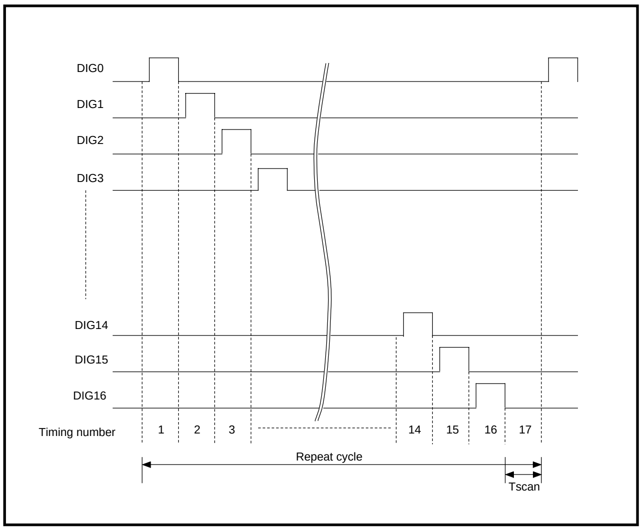


Fig. 75 Digit timing waveform (1)

Power Dissipation Calculating Example 2 (when 2 or more digit is turned ON at same time)

●Fixed number depending on microcomputer's standard

- V_{OH} output fall voltage of high-breakdown port 2 V (max.); | Current value | = at 18 mA
- Resistor value 43 V / 900 µA = 48 kΩ (min.)
- Power dissipation of internal circuit (CPU, ROM, RAM etc.) = 5 V × 15 mA = 75 mW

●Fixed number depending on use condition

- Apply voltage to V_{EE} pin: Vcc – 45 V
- Timing number 11; digit number 12; segment number 24
- Ratio of Toff time corresponding Tdisp time: 1/16
- Turn ON segment number during repeat cycle: 114
- All segment number during repeat cycle: 264 (= 11 × 24)
- Total number of built-in resistor: for digit; 10, for segment; 22
- Digit pin current value: 18 (mA)
- Segment pin current value: 3 (mA)

(1) Digit pin power dissipation
{18 × 12 × (1–1/16) × 2} / 11 = 36.82 mW
(2) Segment pin power dissipation
{3 × 114 × (1–1/16) × 2} / 11 = 58.30 mW
(3) Pull-down resistor power dissipation (digit)
$(45 – 2)^2$ /48 × (12 × 10/12) × (1 – 1/16) / 11 = 32.84 mW
(4) Pull-down resistor power dissipation (segment)
$(45 – 2)^2$ /48 × (114 × 22/24) × (1 – 1/16) / 11 = 343.08 mW
(5) Internal circuit power dissipation (CPU, ROM, RAM etc.) = 75 mW

(1) + (2)+ (3) + (4) + (5) = 547 mW

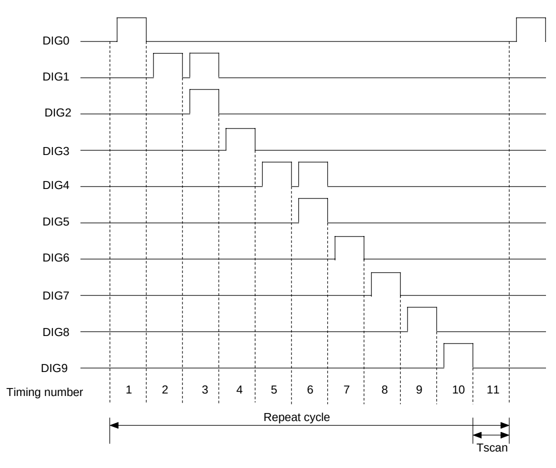


Fig. 76 Digit timing waveform (2)

ABSOLUTE MAXIMUM RATINGS

Table 12 Absolute maximum ratings

Symbol	Parameter		Conditions	Ratings	Unit
V_{CC}	Power source voltage		All voltages are based on V_{SS}. Output transistors are cut off.	–0.3 to 6.5	V
V_{EE}	Pull-down power source voltage			V_{CC} – 45 to V_{CC} +0.3 **(Note 1)**	V
				V_{CC} – 42 to V_{CC} +0.3 **(Note 2)**	V
V_I	Input voltage	$P4_7$, $P5_0$–$P5_7$, $P6_1$–$P6_5$, $P7_0$–$P7_7$, $P8_4$–$P8_7$, $P9_0$, $P9_1$		–0.3 to V_{CC} +0.3	V
V_I	Input voltage	$P4_0$–$P4_6$, $P6_0$		–0.3 to 13	V
V_I	Input voltage	$P0_0$–$P0_7$, $P2_0$–$P2_7$, $P8_0$–$P8_3$		V_{CC} – 45 to V_{CC} +0.3 **(Note 1)**	V
				V_{CC} – 42 to V_{CC} +0.3 **(Note 2)**	V
V_I	Input voltage	$\overline{\text{RESET}}$, X_{IN}		–0.3 to V_{CC} +0.3	V
V_I	Input voltage	X_{CIN}		–0.3 to V_{CC} +0.3	V
V_O	Output voltage	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P8_0$–$P8_3$		V_{CC} – 45 to V_{CC} +0.3 **(Note 1)**	V
				V_{CC} – 42 to V_{CC} +0.3 **(Note 2)**	V
V_O	Output voltage	$P5_0$–$P5_7$, $P6_1$–$P6_5$, $P7_0$–$P7_7$, $P8_4$–$P8_7$, $P9_0$, $P9_1$, X_{OUT}, X_{COUT}		–0.3 to V_{CC} +0.3	V
V_O	Output voltage	$P4_0$–$P4_6$, $P6_0$		–0.3 to 13	V
P_d	Power dissipation		Ta = –20 to 65 °C	800	mW
			Ta = 65 to 85 °C	800 – 12.5 × (Ta – 65)	mW
T_{opr}	Operating temperature			–20 to 85	°C
T_{stg}	Storage temperature			–40 to 125	°C

Notes 1: When Vcc is 4.0 to 5.5 V.
2: When Vcc is 2.7 to 4.0 V.

RECOMMENDED OPERATING CONDITIONS

Table 13 Recommended operating conditions (1)
(Vcc = 2.7 to 5.5 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter			Limits Min.	Limits Typ.	Limits Max.	Unit
V_{CC}	Power source voltage	In high-speed mode		4.0	5.0	5.5	V
		In middle-/low-speed mode, 2 MHz or less in high-speed mode		2.7	5.0	5.5	V
V_{SS}	Power source voltage				0		V
V_{EE}	Pull-down power source voltage	V_{CC} = 4.0 to 5.5 V		V_{CC}–43		V_{CC}	V
		V_{CC} = 2.7 to 4.0 V		V_{CC}–40		V_{CC}	V
V_{REF}	Analog reference voltage (when A-D converter is used)			2.0		V_{CC}	V
AV_{SS}	Analog power source voltage				0		V
V_{IA}	Analog input voltage	AN_0–AN_{11}		0		V_{CC}	V
V_{IH}	"H" input voltage	$P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_5$, $P7_0$–$P7_7$, $P9_0$, $P9_1$	V_{CC} = 4.0 to 5.5 V	$0.75V_{CC}$		V_{CC}	V
			V_{CC} = 2.7 to 4.0 V	$0.8V_{CC}$		V_{CC}	V
V_{IH}	"H" input voltage	$P8_4$–$P8_7$	V_{CC} = 4.0 to 5.5 V	$0.4V_{CC}$		V_{CC}	V
			V_{CC} = 2.7 to 4.0 V	0.5Vcc		Vcc	V
V_{IH}	"H" input voltage	$P0_0$–$P0_7$		$0.8V_{CC}$		V_{CC}	V
V_{IH}	"H" input voltage	$P2_0$–$P2_7$, $P8_0$–$P8_3$	V_{CC} = 4.0 to 5.5 V	$0.52V_{CC}$		V_{CC}	V
			V_{CC} = 2.7 to 4.0 V	$0.75V_{CC}$		V_{CC}	V
V_{IH}	"H" input voltage	$\overline{\text{RESET}}$		$0.8V_{CC}$		V_{CC}	V
V_{IH}	"H" input voltage	X_{IN}, X_{CIN}		$0.8V_{CC}$		V_{CC}	V
V_{IL}	"L" input voltage	$P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_5$, $P7_0$–$P7_7$, $P9_0$, $P9_1$	V_{CC} = 4.0 to 5.5 V	0		$0.25V_{CC}$	V
			V_{CC} = 2.7 to 4.0 V	0		$0.2V_{CC}$	V
V_{IL}	"L" input voltage	$P8_4$–$P8_7$		0		$0.16V_{CC}$	V
V_{IL}	"L" input voltage	$P0_0$–$P0_7$, $P2_0$–$P2_7$, $P8_0$–$P8_3$		0		$0.2V_{CC}$	V
V_{IL}	"L" input voltage	$\overline{\text{RESET}}$		0		$0.2V_{CC}$	V
V_{IL}	"L" input voltage	X_{IN}, X_{CIN}		0		$0.2V_{CC}$	V

Table 14 Recommended operating conditions (2)

(Vcc = 2.7 to 5.5 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
$\Sigma I_{OH(peak)}$	H” total peak output current **(Note 1)** $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P8_0$–$P8_3$				–240	mA
$\Sigma I_{OH(peak)}$	“H” total peak output current **(Note 1)** $P5_0$–$P5_7$, $P6_1$–$P6_5$, $P7_0$–$P7_7$, $P9_0$, $P9_1$				–60	mA
$\Sigma I_{OL(peak)}$	“L” total peak output current **(Note 1)** $P5_0$–$P5_7$, $P6_0$–$P6_5$, $P7_0$–$P7_7$, $P9_0$, $P9_1$				100	mA
$\Sigma I_{OL(peak)}$	“L” total peak output current **(Note 1)** $P4_0$–$P4_6$, $P8_4$–$P8_7$				60	mA
$\Sigma I_{OH(avg)}$	“H” total average output current **(Note 1)** $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P8_0$–$P8_7$				–120	mA
$\Sigma I_{OH(avg)}$	“H” total average output current **(Note 1)** $P5_0$–$P5_7$, $P6_1$–$P6_5$, $P7_0$–$P7_7$, $P9_0$, $P9_1$				–30	mA
$\Sigma I_{OL(avg)}$	“L” total average output current **(Note 1)** $P5_0$–$P5_7$, $P6_0$–$P6_5$, $P7_0$–$P7_7$, $P9_0$, $P9_1$				50	mA
$\Sigma I_{OL(avg)}$	“L” total average output current **(Note 1)** $P4_0$–$P4_6$, $P8_4$–$P8_7$				30	mA
$I_{OH(peak)}$	“H” peak output current **(Note 2)** $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P8_0$–$P8_3$				–40	mA
$I_{OH(peak)}$	“H” peak output current **(Note 2)** $P5_0$–$P5_7$, $P6_1$–$P6_5$, $P7_0$–$P7_7$, $P8_4$–$P8_7$, $P9_0$, $P9_1$				–10	mA
$I_{OL(peak)}$	“L” peak output current **(Note 2)** $P5_0$–$P5_7$, $P6_1$–$P6_5$, $P7_0$–$P7_7$, $P8_4$–$P8_7$, $P9_0$, $P9_1$				10	mA
$I_{OL(peak)}$	“L” peak output current **(Note 2)** $P4_0$–$P4_6$, $P6_0$				30	mA
$I_{OH(avg)}$	“H” average output current **(Note 3)** $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P8_0$–$P8_3$				–18	mA
$I_{OH(avg)}$	“H” average output current **(Note 3)** $P5_0$–$P5_7$, $P6_0$–$P6_5$, $P7_0$–$P7_7$, $P8_4$–$P8_7$, $P9_0$, $P9_1$				–5	mA
$I_{OL(avg)}$	“L” average output current **(Note 3)** $P5_0$–$P5_7$, $P6_1$–$P6_5$, $P7_0$–$P7_7$, $P8_4$–$P8_7$, $P9_0$, $P9_1$				5	mA
$I_{OL(avg)}$	“L” average output current **(Note 3)** $P4_0$–$P4_6$, $P6_0$				15	mA
$f(CNTR_0)$ $f(CNTR_1)$	Clock input frequency for timers 2, 4, and X (duty cycle 50 %)	V_{CC} = 4.0 to 5.5 V			250	kHz
		V_{CC} = 2.7 to 4.0 V			100	kHz
$f(X_{IN})$	Main clock input oscillation frequency **(Note 4)**	V_{CC} = 4.0 to 5.5 V			4.2	MHz
		V_{CC} = 2.7 to 4.0 V			2	MHz
$f(X_{CIN})$	Sub-clock input oscillation frequency **(Notes 4, 5)**			32.768	50	kHz

Notes 1: The total output current is the sum of all the currents flowing through all the applicable ports. The total average current is an average value measured over 100 ms. The total peak current is the peak value of all the currents.

2: The peak output current is the peak current flowing in each port.

3: The average output current I_{OL} (avg), I_{OH}(avg) in an average value measured over 100 ms.

4: When the oscillation frequency has a duty cycle of 50%.

5: When using the microcomputer in low-speed mode, set the sub-clock input oscillation frequency on condition that $f(X_{CIN}) < f(X_{IN})/3$.

ELECTRICAL CHARACTERISTICS

Table 15 Electrical characteristics (1)

(V_{CC} = 2.7 to 5.5 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter			Test conditions	Limits Min.	Limits Typ.	Limits Max.	Unit
V_{OH}	“H” output voltage	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P8_0$–$P8_3$	V_{CC} = 4.0 to 5.5 V	I_{OH} = –18 mA	V_{CC}–2.0			V
			V_{CC} = 2.7 to 4.0 V	I_{OH} = –10 mA	V_{CC}–1.5			V
V_{OH}	“H” output voltage	$P5_0$–$P5_7$, $P6_0$–$P6_5$, $P7_0$–$P7_7$, $P8_4$–$P8_7$, $P9_0$, $P9_1$	V_{CC} = 4.0 to 5.5 V	I_{OH} = –10 mA	V_{CC}–2.0			V
			V_{CC} = 2.7 to 4.0 V	I_{OH} = –10 mA	V_{CC}–1.0			V
V_{OL}	“L” output voltage	$P5_0$–$P5_7$, $P6_1$–$P6_5$, $P8_4$–$P8_7$, $P9_0$, $P9_1$	V_{CC} = 4.0 to 5.5 V	I_{OL} = 10 mA			2.0	V
			V_{CC} = 2.7 to 4.0 V	I_{OL} = 1.6 mA			0.4	V
V_{OL}	“L” output voltage	$P4_0$–$P4_6$, $P6_0$	V_{CC} = 4.0 to 5.5 V	I_{OL} = 15 mA		0.6	2.0	V
			V_{CC} = 2.7 to 4.0 V	I_{OL} = 5 mA		0.3	1.0	V
V_{T+}–V_{T-}	Hysteresis	$P4_0$–$P4_2$, $P4_5$–$P4_7$, P5, $P6_0$, $P6_1$,$P6_4$ **(Note 1)**				0.4		V
V_{T+}–V_{T-}	Hysteresis	$\overline{RESET}$, X_{IN}				0.5		V
V_{T+}–V_{T-}	Hysteresis	X_{CIN}				0.5		µA
I_{IH}	“H” input current	$P4_7$, $P5_0$–$P5_7$, $P6_1$–$P6_5$, $P7_0$–$P7_7$, $P8_4$–$P8_7$		V_I = V_{CC}			5.0	µA
I_{IH}	“H” input current	$P4_0$–$P4_6$, $P6_0$		V_I = 12 V			10.0	µA
I_{IH}	“H” input current	$P0_0$–$P0_7$, $P2_0$–$P2_7$, $P8_0$–$P8_3$ **(Note 2)**		V_I = V_{CC}			5.0	µA
I_{IH}	“H” input current	$\overline{RESET}$, X_{CIN}		V_I = V_{CC}			5.0	µA
I_{IH}	“H” input current	X_{IN}		V_I = V_{CC}		4.0		µA
I_{IL}	“L” input current	$P4_0$–$P4_7$, $P6_0$		V_I = V_{SS}			–5.0	µA
I_{IL}	“L” input current	$P5_0$–$P5_7$, $P6_1$–$P6_5$, $P7_0$–$P7_7$, $P8_4$–$P8_7$, $P9_0$, $P9_1$		V_I = V_{SS} Pull-up “off”			–5.0	µA
				V_{CC} = 5 V, V_I = V_{SS} Pull-up “on”		–70		µA
				V_{CC} = 3 V, V_I = V_{SS} Pull-up “on”		–25		µA
I_{IL}	“L” input current	$P0_0$–$P0_7$, $P2_0$–$P2_7$, $P8_0$–$P8_3$ **(Note 2)**		V_I = V_{SS}			–5.0	µA
I_{IL}	“L” input current	$\overline{RESET}$, X_{CIN}		V_I = V_{SS}			–5.0	µA
I_{IL}	“L” input current	X_{IN}		V_I = V_{SS}		–4.0		µA
R_{PULLD}	Pull-down resistor	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P3_0$–$P3_7$ ($P2_0$–$P2_7$, $P8_0$–$P8_3$ at option)		V_{EE} = V_{CC}–43 V, V_{OL} =V_{CC} Output transistors “off”	143	72	47	kΩ
I_{LEAK}	Output leak current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P8_0$–$P8_3$		V_{EE} = V_{CC}–43 V, V_{OL} =V_{CC}–43 V Output transistors “off”			–10	µA
I_{READH}	“H” read current	$P0_0$–$P0_7$, $P2_0$–$P2_7$, $P8_0$–$P8_3$		V_I = 5 V		1		µA
V_{RAM}	RAM hold voltage			When clock is stopped	2		Vcc	V

Notes 1: $P4_2$, $P4_5$, $P4_6$, and $P6_0$ of the mask option type P do not have hysteresis characteristics.
2: Except when reading ports P0, P2, or P8.

Table 16 Electrical characteristics (2)
(V_{CC} =2.7 to 5.5 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits Min.	Typ.	Max.	Unit
I_{CC}	Power source current	High-speed mode f(X_{IN}) = 4.2 MHz f(X_{CIN}) = 32 kHz Output transistors "off"			7.5		mA
		High-speed mode f(X_{IN}) = 4.2 MHz (in WIT state) f(X_{CIN}) = 32 kHz Output transistors "off"			1		mA
		Middle-speed mode f(X_{IN}) = 4.2 MHz f(X_{CIN}) = stopped Output transistors "off"			3		mA
		Middle-speed mode f(X_{IN}) = 4.2 MHz (in WIT state) f(X_{CIN}) = stopped Output transistors "off"			1		mA
		Low-speed mode f(X_{IN}) = stopped f(X_{CIN}) = 32 kHz Low-power dissipation mode (CM_3 = 0) Output transistors "off"			60		µA
		Low-speed mode f(X_{IN}) = stopped f(X_{CIN}) = 32 kHz (in WIT state) Low-power dissipation mode (CM_3 = 0) Output transistors "off"			20		µA
		Increment when A-D conversion is executed			0.6		mA
		All oscillation stopped (in STP state) Output transistors "off"	Ta = 25 °C		0.1	1	µA
			Ta = 85 °C			10	µA

A-D converter characteristics

Table 17 A-D converter characteristics (1)
(V_{CC} = 4.0 to 5.5 V, V_{SS} = 0 V, Ta = –20 to 85 °C, f(X_{IN}) = 250 kHz to 4.2 MHz in high-speed mode, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min.	Typ.	Max.	Unit
—	Resolution				10	Bits
—	Absolute accuracy (excluding quantization error)	V_{CC} = V_{REF} = 5.12 V		±1	±2.5	LSB
T_{CONV}	Conversion time		61		62	tc(ϕ)
I_{VREF}	Reference input current	V_{REF} = 5.0 V	50	150	200	µA
I_{IA}	Analog port input current			0.5	5.0	µA
R_{LADDER}	Ladder resistor			35		kΩ

Table 18 A-D converter characteristics (2)
(V_{CC} = 2.7 to 4.0 V, V_{SS} = 0 V, Ta = –20 to 85 °C, f(X_{IN}) = 250 kHz to 2 MHz in high-speed mode, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min.	Typ.	Max.	Unit
—	Resolution				10	Bits
—	Absolute accuracy (excluding quantization error)	V_{CC} = V_{REF} = 3.3 V		±3	±6	LSB
T_{CONV}	Conversion time		61		62	tc(ϕ)
I_{VREF}	Reference input current	V_{REF} = 3.3 V	30	95	120	µA
I_{IA}	Analog port input current			0.5	5.0	µA
R_{LADDER}	Ladder resistor			35		kΩ

TIMING REQUIREMENTS

Table 19 Timing requirements (1)
(V_{CC} = 4.0 to 5.5 V, V_{SS} = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_W(\overline{RESET})$	Reset input “L” pulse width	2.0			µs
$t_C(X_{IN})$	Main clock input cycle time (X_{IN} input)	238			ns
$t_{WH}(X_{IN})$	Main clock input “H” pulse width	60			ns
$t_{WL}(X_{IN})$	Main clock input “L” pulse width	60			ns
$t_C(X_{CIN})$	Sub-clock input cycle time (X_{CIN} input)	20			µs
$t_{WH}(X_{CIN})$	Sub-clock input “H” pulse width	5.0			µs
$t_{WL}(X_{CIN})$	Sub-clock input “L” pulse width	5.0			µs
$t_C(CNTR)$	$CNTR_0$, $CNTR_1$ input cycle time	4.0			µs
$t_{WH}(CNTR)$	$CNTR_0$, $CNTR_1$ input “H” pulse width	1.6			µs
$t_{WL}(CNTR)$	$CNTR_0$, $CNTR_1$ input “L” pulse width	1.6			µs
$t_{WH}(INT)$	INT_0 to INT_4 input “H” pulse width	80			ns
$t_{WL}(INT)$	INT_0 to INT_4 input “L” pulse width	80			ns
$t_C(S_{CLK})$	Serial I/O clock input cycle time	0.95			µs
$t_{WH}(S_{CLK})$	Serial I/O clock input “H” pulse width	400			ns
$t_{WL}(S_{CLK})$	Serial I/O clock input “L” pulse width	400			ns
$t_{su}(S_{CLK}–S_{IN})$	Serial I/O input set up time	200			ns
$t_h(S_{CLK}–S_{IN})$	Serial I/O input hold time	200			ns

Table 20 Timing requirements (2)
(V_{CC} = 2.7 to 5.5 V, V_{SS} = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_W(\overline{RESET})$	Reset input “L” pulse width	2.0			µs
$t_C(X_{IN})$	Main clock input cycle time (X_{IN} input)	500			ns
$t_{WH}(X_{IN})$	Main clock input “H” pulse width	120			ns
$t_{WL}(X_{IN})$	Main clock input “L” pulse width	120			ns
$t_C(X_{CIN})$	Sub-clock input cycle time (X_{CIN} input)	20			µs
$t_{WH}(X_{CIN})$	Sub-clock input “H” pulse width	5.0			µs
$t_{WL}(X_{CIN})$	Sub-clock input “L” pulse width	5.0			µs
$t_C(CNTR)$	$CNTR_0$, $CNTR_1$ input cycle time	10			µs
$t_{WH}(CNTR)$	$CNTR_0$, $CNTR_1$ input “H” pulse width	4.0			µs
$t_{WL}(CNTR)$	$CNTR_0$, $CNTR_1$ input “L” pulse width	4.0			µs
$t_{WH}(INT)$	INT_0 to INT_4 input “H” pulse width	230			ns
$t_{WL}(INT)$	INT_0 to INT_4 input “L” pulse width	230			ns
$t_C(S_{CLK})$	Serial I/O clock input cycle time	2.0			µs
$t_{WH}(S_{CLK})$	Serial I/O clock input “H” pulse width	950			ns
$t_{WL}(S_{CLK})$	Serial I/O clock input “L” pulse width	950			ns
$t_{su}(S_{CLK}–S_{IN})$	Serial I/O input set up time	400			ns
$t_h(S_{CLK}–S_{IN})$	Serial I/O input hold time	300			ns

SWITCHING CHARACTERISTICS

Table 21 Switching characteristics (1)

(V_{CC} = 4.0 to 5.5 V, V_{SS} = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{WH}(S_{CLK})$	Serial I/O clock output “H” pulse width	C_L = 100 pF	$t_C(S_{CLK})$/2–160			ns
$t_{WL}(S_{CLK})$	Serial I/O clock output “L” pulse width	C_L = 100 pF	$t_C(S_{CLK})$/2–160			ns
$t_d(S_{CLK}–S_{OUT})$	Serial I/O output delay time				0.2 tc	ns
$t_v(S_{CLK}–S_{OUT})$	Serial I/O output valid time		0			ns
$t_r(S_{CLK})$	Serial I/O clock output rising time	C_L = 100 pF			40	ns
$t_f(S_{CLK})$	Serial I/O clock output falling time	C_L = 100 pF			40	ns
t_r(Pch–strg)	P-channel high-breakdown voltage output rising time **(Note 1)**	C_L = 100 pF V_{EE} = V_{CC}–43 V		55		ns
t_r(Pch–weak)	P-channel high-breakdown voltage output rising time **(Note 2)**	C_L = 100 pF V_{EE} = V_{CC}–43 V		1.8		µs

Notes 1: When bit 7 of the FLDC mode register (address $0EF4_{16}$) is at “0”.
2: When bit 7 of the FLDC mode register (address $0EF4_{16}$) is at “1”.

Table 22 Switching characteristics (2)

(V_{CC} = 2.7 to 4.0 V, V_{SS} = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{WH}(S_{CLK})$	Serial I/O clock output “H” pulse width	C_L = 100 pF	$t_C(S_{CLK})$/2–240			ns
$t_{WL}(S_{CLK})$	Serial I/O clock output “L” pulse width	C_L = 100 pF	$t_C(S_{CLK})$/2–240			ns
$t_d(S_{CLK}–S_{OUT})$	Serial I/O output delay time				0.4 tc	ns
$t_v(S_{CLK}–S_{OUT})$	Serial I/O output valid time		0			ns
$t_r(S_{CLK})$	Serial I/O clock output rising time	C_L = 100 pF			60	ns
$t_f(S_{CLK})$	Serial I/O clock output falling time	C_L = 100 pF			60	ns
t_r(Pch–strg)	P-channel high-breakdown voltage output rising time **(Note 1)**	C_L = 100 pF V_{EE} = V_{CC}–40 V		140		ns
t_r(Pch–weak)	P-channel high-breakdown voltage output rising time **(Note 2)**	C_L = 100 pF V_{EE} = V_{CC}–40 V		3.6		µs

Notes 1: When bit 7 of the FLDC mode register (address $0EF4_{16}$) is at “0”.
2: When bit 7 of the FLDC mode register (address $0EF4_{16}$) is at “1”.

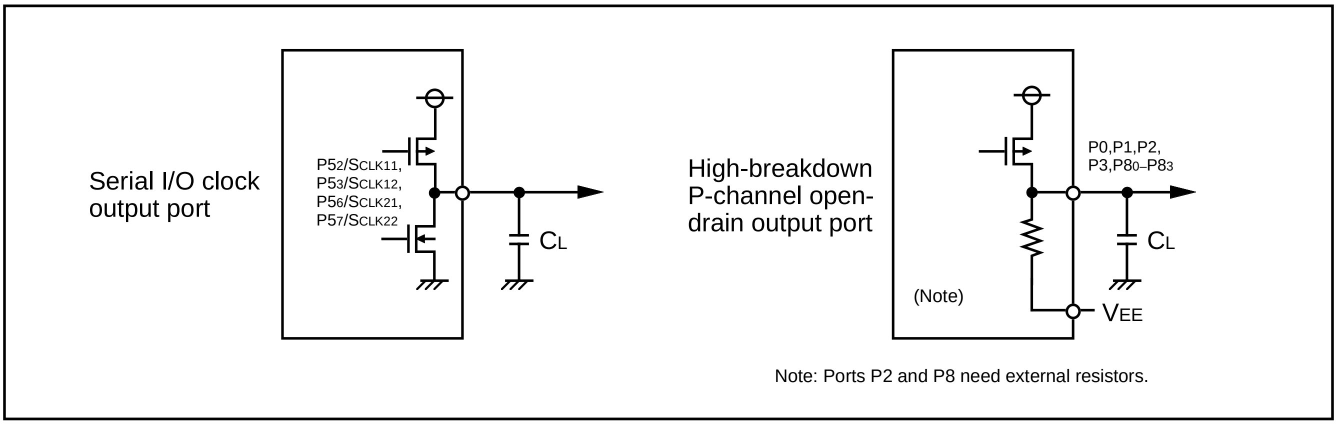


Fig. 77 Circuit for measuring output switching characteristics

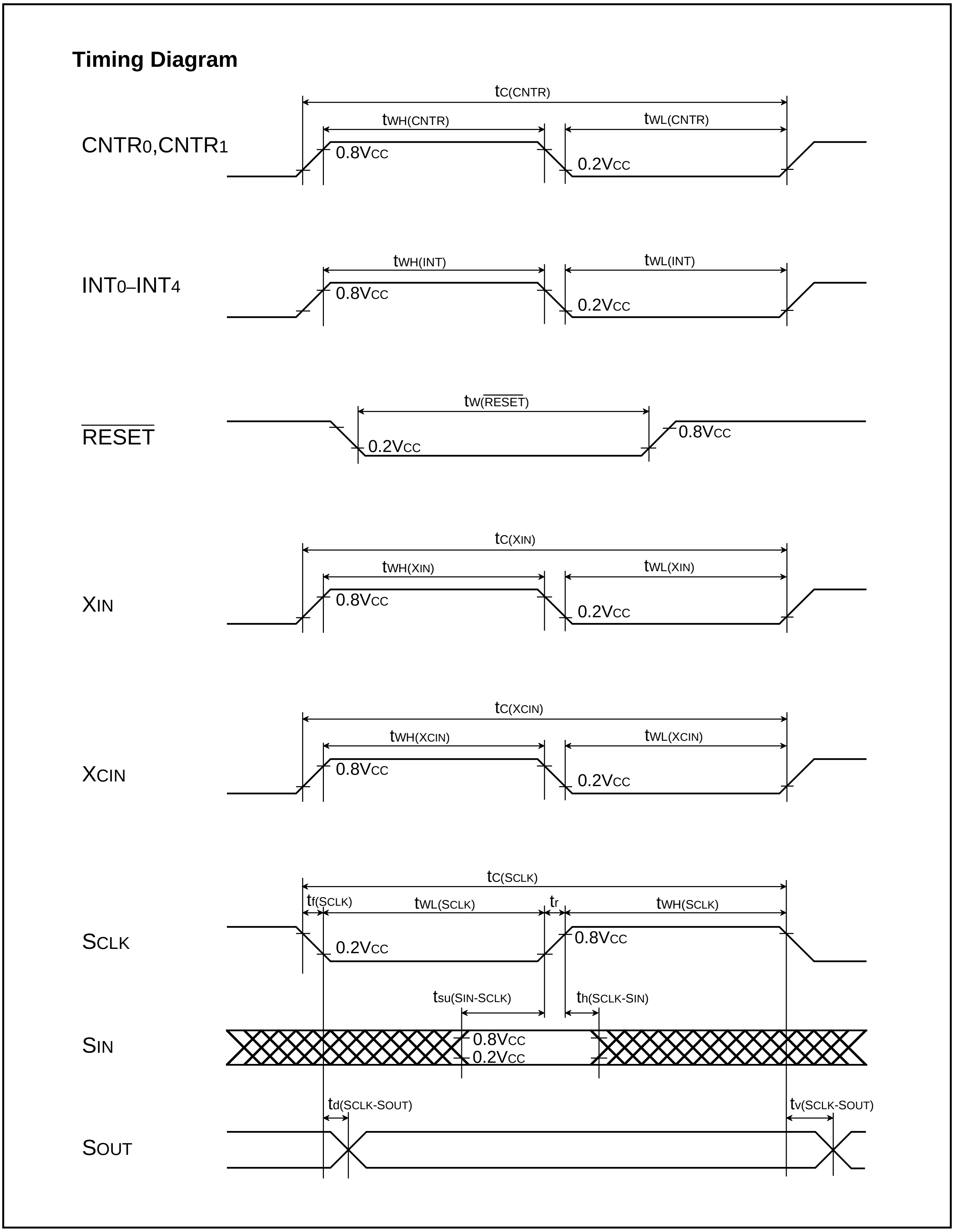


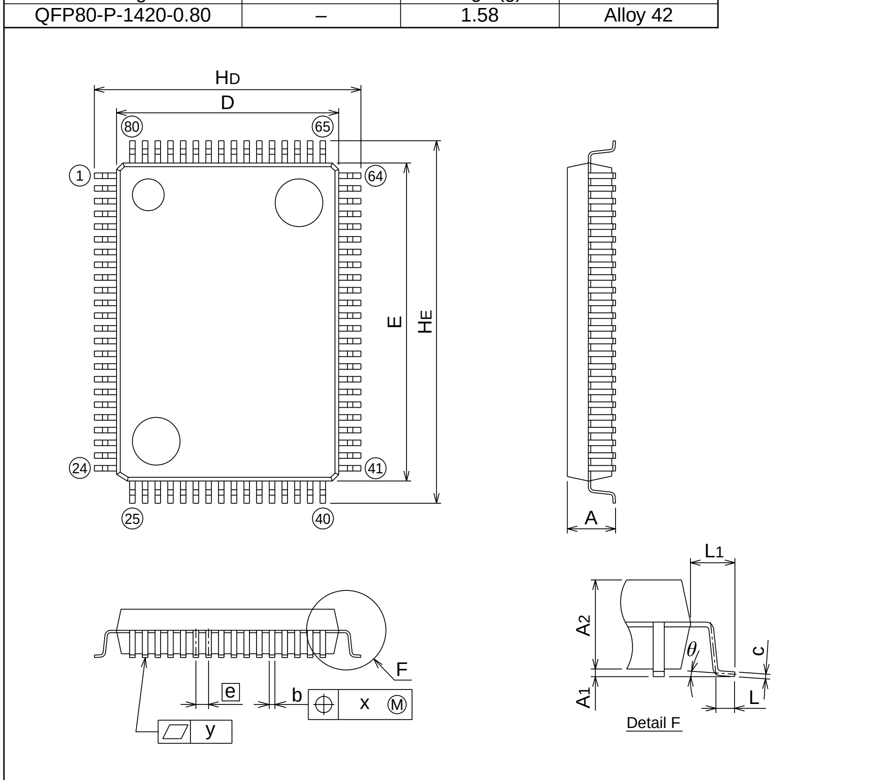
Fig. 78 Timing diagram

PACKAGE OUTLINE

80P6N-A

Plastic 80pin 14×20mm body QFP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
QFP80-P-1420-0.80	–	1.58	Alloy 42



Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	3.05
A_1	0	0.1	0.2
A_2	–	2.8	–
b	0.3	0.35	0.45
c	0.13	0.15	0.2
D	13.8	14.0	14.2
E	19.8	20.0	20.2
e	–	0.8	–
H_D	16.5	16.8	17.1
H_E	22.5	22.8	23.1
L	0.4	0.6	0.8
L_1	–	1.4	–
x	–	–	0.2
y	–	–	0.1
θ	0°	–	10°
b_2	–	0.5	–
I_2	1.3	–	–
M_D	–	14.6	–
M_E	–	20.6	–

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