DS04-21305-3aE

FUJITSU

DATA SHEET

MB87014A ASSP

CMOS PLL Frequency Synthesizer

CMOS SERIAL INPUT PHASE-LOCKED-LOOP (PLL) FREQUENCY SYNTHESIZER

The Fujitsu MB87014A, fabricated in advanced CMOS technology, is a serial input phase locked loop (PLL) frequency synthesizer with an on chip 180MHz dual modulus prescaler.

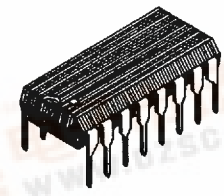
The MB87014A contains a dual modulus prescaler, inverter for an external oscillator, programmable reference divider, control circuit, phase detectors, charge pump, programmable divider (binary 6-bit swallow counter and binary 10-bit programmable counter).

The MB87014A can make up PLL frequency synthesizer operating up to 180MHz.

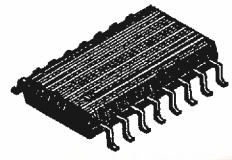
- Single Power Supply Voltage: V_{DD} = 4.5V to 5.5V
- Wide Temperature Range: Ta = −30 to 60°C
- 180MHz input capability @5V (fin input)
- On-chip Inverter for oscillator
- Programmable divider with input amplifier consisting of;
  Binary 6-bit swallow counter
  Binary 10-bit programmable counter
- Programmable reference divider with input amplifier consisting of;
  Binary 16-bit programmable reference counter
- Divide factor of programmable divider and programmable reference divider are set by serial data input. (The last data bit is a control bit.)
- 3-type of phase detector outputs
  On-chip charge pump output for active LPF
  On-chip charge pump output for passive LPF
  Output for external charge pump
- 16-pin Standard Dual-in-line Package (Suffix: -P)
  16-pin Standard Flat Package (Suffix: -PF)
- Pulse Swallow Function

$f_{VCO} = [(N \times M) + A] \times (f_{OSC} \div R)$ (N > A)

f_{VCO} : Output frequency of external voltage controlled oscillator (VCO)
N : Preset divide factor of binary 10-bit programmable counter (5 to 1023)
M : Preset modulus factor of internal dual modulus prescaler (64/65)
A : Preset divide factor of binary 6-bit swallow counter (0 to 63)
f_{OSC} : Output frequency of the external oscillator
R : Preset divide factor of binary 16-bit programmable reference counter (5 to 65535)

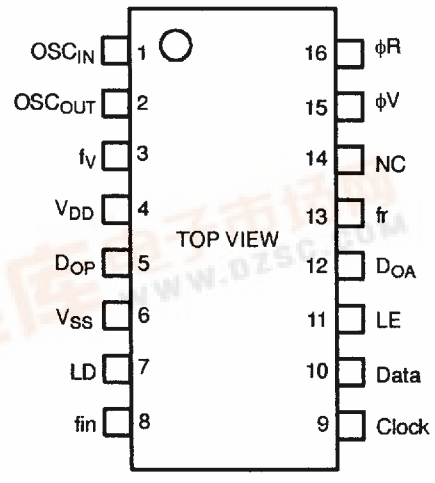


PLASTIC PACKAGE
DIP-16P-M04



PLASTIC PACKAGE
FPT-16P-M06

PIN ASSIGNMENT



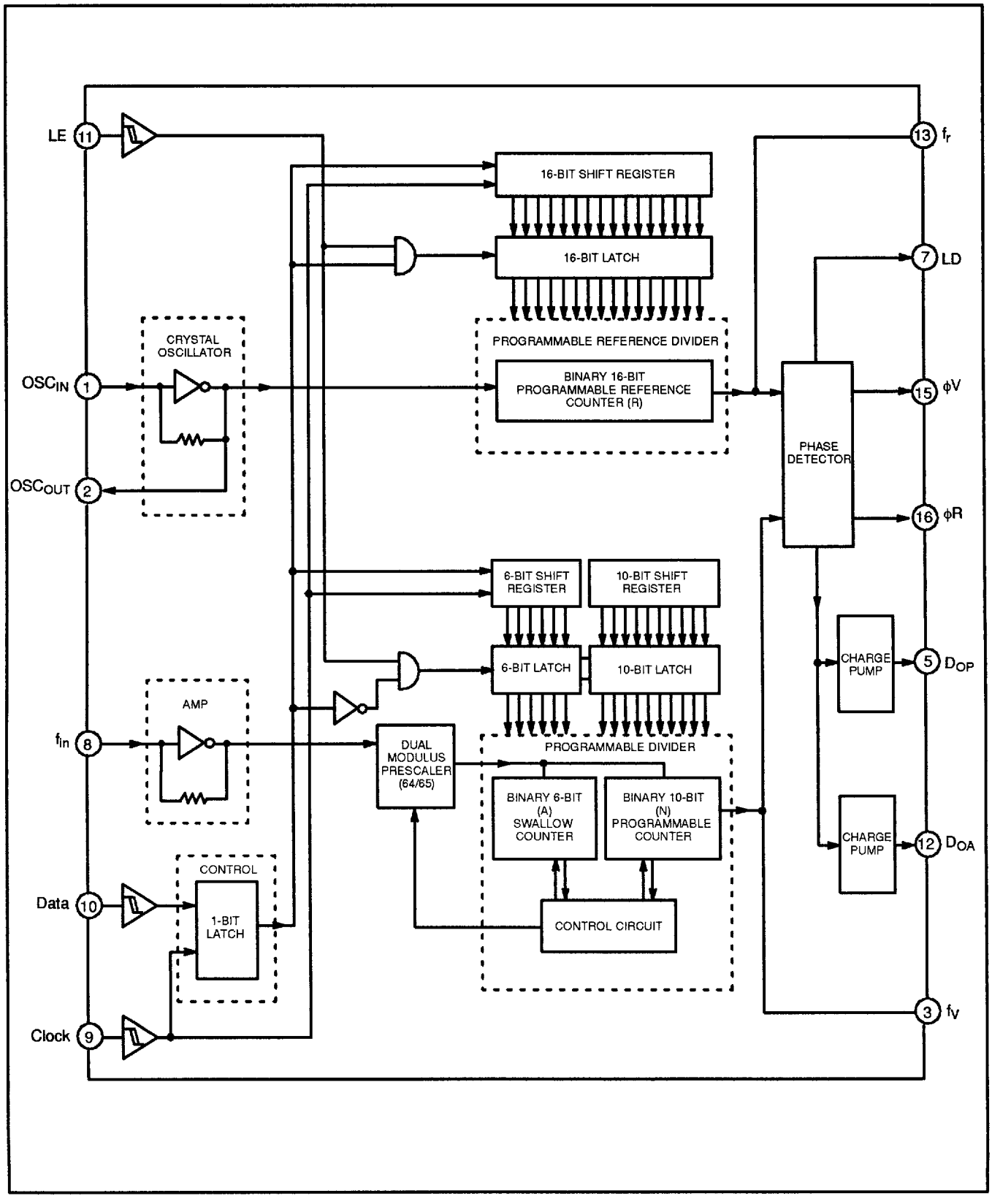
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{DD}	V_{SS} −0.3 to V_{SS} +6.0	V
Input Voltage	V_{IN}	V_{SS} −0.3 to V_{DD} +0.3	V
Output Voltage	V_{OUT}	V_{SS} −0.3 to V_{DD} +0.3	V
Output Current	I_{OUT}	±10	mA
Operating Ambient Temperature	Ta	−30 to +80	°C
Storage Temperature	T_{STG}	−40 to +125	°C
Power Dissipation	P_D	300	mW

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

BLOCK DIAGRAM



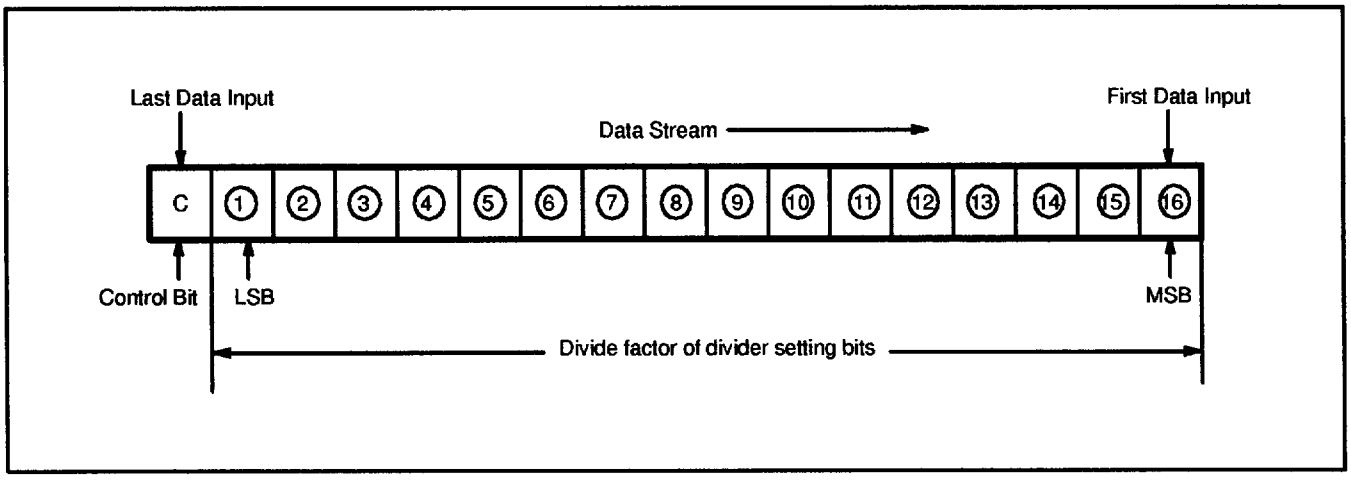
PIN DESCRIPTION

Pin No.	Symbol	I/O	Description
1	OSC_{IN}	I	Input pin for crystal oscillator. Input to the inverting amplifier that forms part of the oscillator. This pin receives the oscillator signal as AC coupled when an external oscillator is used, but for large amplitude signals (standard CMOS levels) DC coupling may also be used.
2	OSC_{OUT}	O	Output pin for crystal oscillator. Output of the inverting amplifier. This pin should be left open when an external oscillator is used.
3	f_V	O	Monitor pin for the phase detector input. This pin is tied to the programmable divider output.
4	V_{DD}	-	Power supply voltage input.
5	D_{OP}	O	Output pin for low pass filter (Passive type). The mode of D_{OP} is changed by the combination of programmable reference divider output frequency f_r, and programmable divider output frequency f_V as listed below: $f_r > f_V$: Drive mode (D_{OP} = High level) $f_r = f_V$: High-impedance $f_r < f_V$: Sink mode (D_{OP} = Low level)
6	V_{SS}	-	Ground.
7	LD	O	Output of phase detector. It is high level when f_r and f_V are coherent, and when the loop is locked. Otherwise it outputs negative pulse signal.
8	f_{in}	I	Frequency input to an internal prescaler from VCO. The connection with VCO should be AC connection.
9	Clock	I	Clock signal input for shift registers. Each rising edge of the clock makes one bit of the data shift into the shift registers.
10	Data	I	Serial data input for shift registers. The last bit of the data is the controlbit The control data determines which latch is activated.
11	LE	I	Load enable input. When this pin is high, the data from shift register is latched into programmable reference divider or programmable divider depending upon a control bit setting.
12	D_{OA}	O	Output pin for low pass filter (Active type). The mode of D_{OA} is changed by the combination of programmable reference divider output frequency f_r, and programmable divider output frequency f_V as listed below: $f_r > f_V$: Sink mode (D_{OA} = Low level) $f_r = f_V$: High-impedance $f_r < f_V$: Drive mode (D_{OA} = High level)
13	f_r	O	Monitor pin for the phase detector input. This pin is tied to the programmable reference divider output.
14	NC	-	No connection.
15 16	ϕV ϕR	O O	Output pins for low pass filter (differential filter type). Outputs for external charge pump are changed by the combination of programmable reference divider output frequency f_r, and programmable divider output frequency f_V as listed below. ϕV / ϕR $f_r > f_V$: High level / Low level $f_r = f_V$: High level / High level $f_r < f_V$: Low level / High level

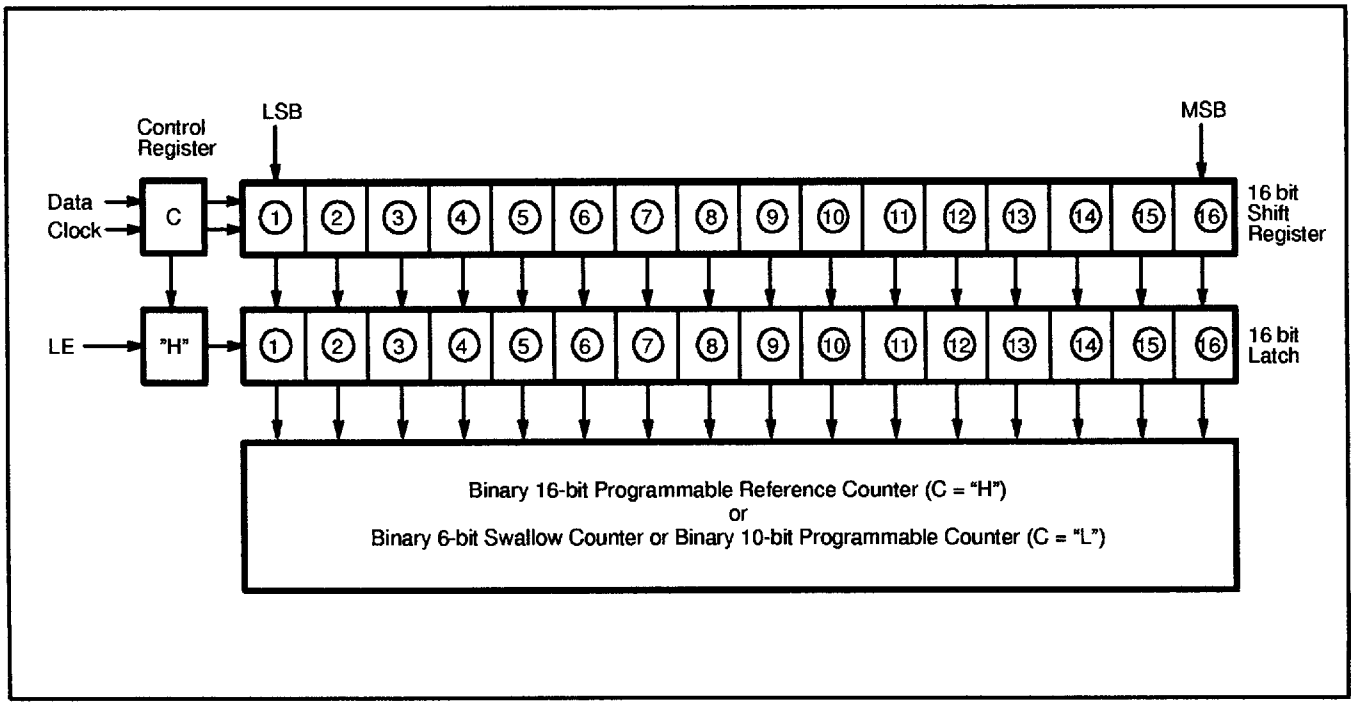
FUNCTIONAL DESCRIPTIONS

DIVIDE FACTOR OF DIVIDER

Serial data of binary code is input to Data pin. On rising edge of clock shifts one bit of data into the shift registers. Input data consists of 16-bit data and 1-bit of control data. The control data determines which latch is activated. When control bit is high, 16-bit latch is selected. When low, 6-bit latch and 10-bit latch is selected.



The serial data is input to 16-bit shift registers and 1-bit control register. When load enable is high, the data from the shift register is latched into the programmable reference divider (binary 16-bit programmable reference counter) or programmable divider (binary 6-bit swallow counter and binary 10-bit programmable counter) depending upon a control bit setting.



FUNCTIONAL DESCRIPTIONS (Continued)

BINARY 6-BIT SWALLOW COUNTER DATA INPUT

Divide Factor	①	②	③	④	⑤	⑥
0	0	0	0	0	0	0
1	1	0	0	0	0	0
2	0	1	0	0	0	0
. .	. .	. .	. .	. .	. .	. .
63	1	1	1	1	1	1

• Divide factor A: 0 to 63

BINARY 10-BIT PROGRAMMABLE COUNTER DATA INPUT

Divide Factor	⑦	⑧	⑨	⑩	⑪	⑫	⑬	⑭	⑮	⑯
5	1	0	1	0	0	0	0	0	0	0
6	0	1	1	0	0	0	0	0	0	0
7	1	1	1	0	0	0	0	0	0	0
. .	. .	. .	. .	. .	. .	. .	. .	. .	. .	. .
1023	1	1	1	1	1	1	1	1	1	1

• Divide factor N: 5 to 1023
• Divide factor less than 5 is prohibited.

BINARY 16-BIT PROGRAMMABLE COUNTER DATA INPUT

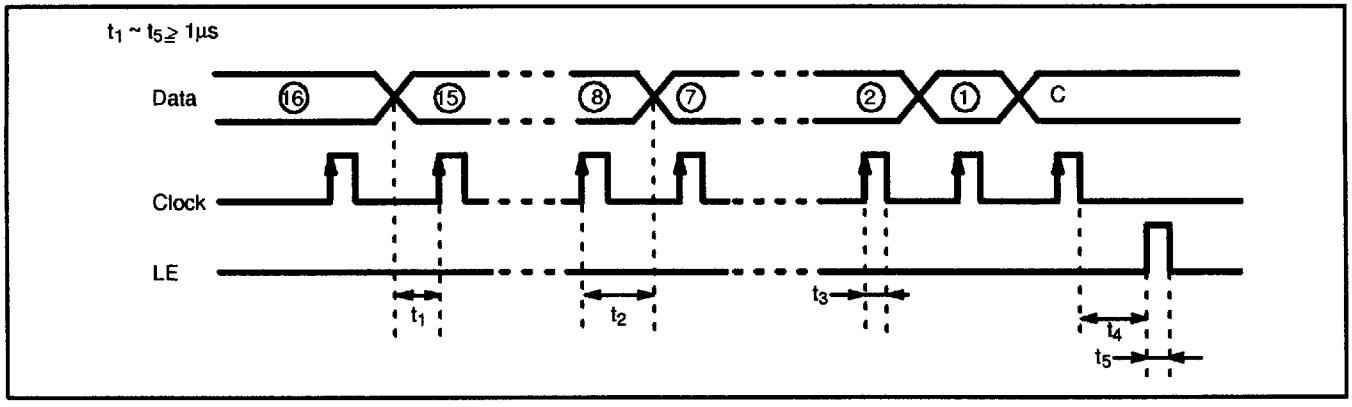
Divide Factor	①	②	③	④	⑤	⑥	⑦	⑧	⑨	⑩	⑪	⑫	⑬	⑭	⑮	⑯
5	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
6	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
7	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
. .	. .	. .	. .	. .	. .	. .	. .	. .	. .	. .	. .	. .	. .	. .	. .	. .
65535	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

• Divide factor R: 5 to 65535
• Divide factor less than 5 is prohibited.

STAND-BY MODE

When all zero of 16-bit serial data is input, the MB87014A goes to stand-by mode. During stand-by mode, internal circuit stops operation and f_{in} and OSC_{IN} are forced to high level. Thus, low supply current is achieved. Stand-by down mode is release, when the data except all zero data is input.

SERIAL DATA INPUT TIMING

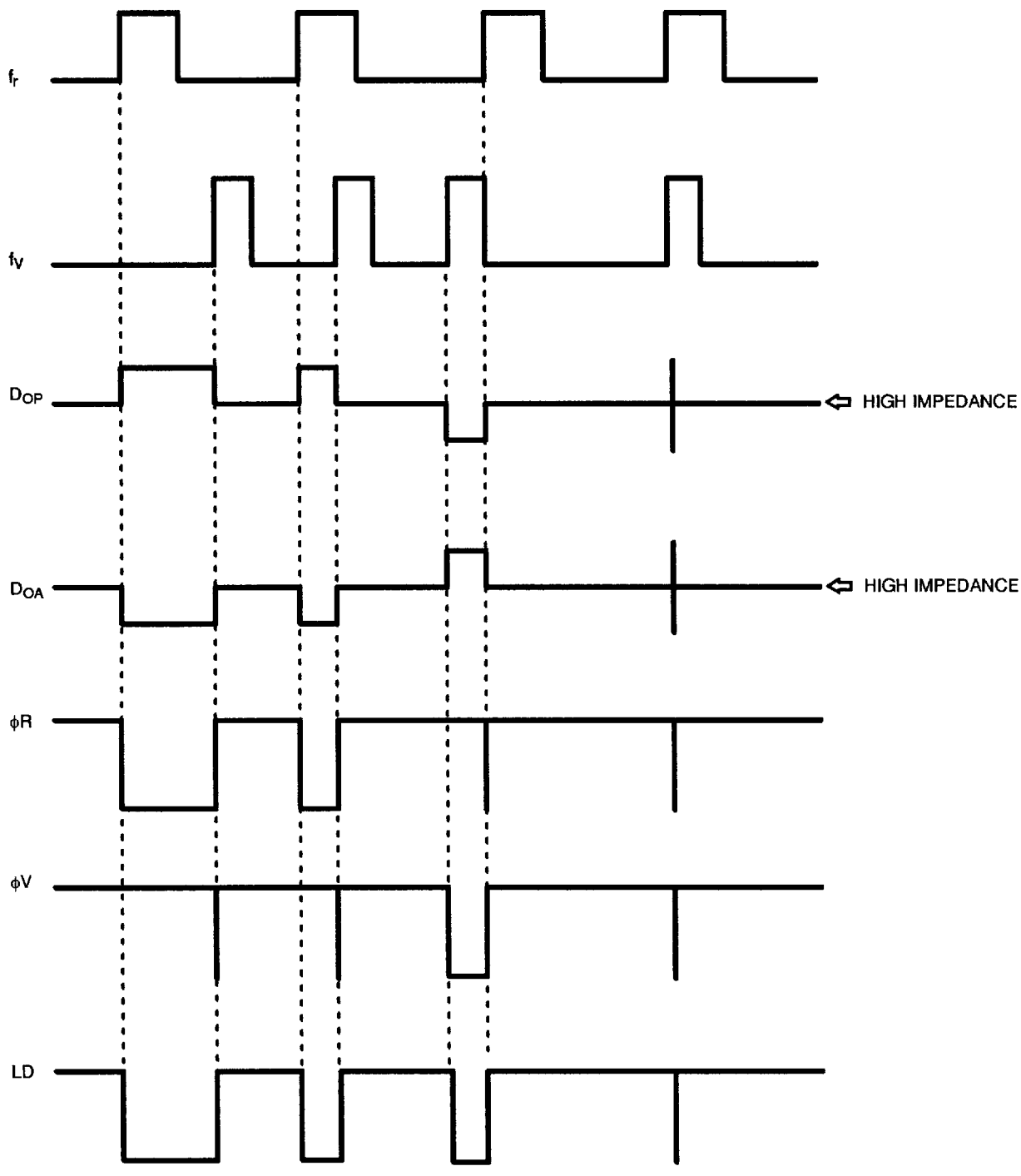


Notes: Data: Serial data input is used for setting divide factor of programmable reference divider or programmable divider.
Data is input from MSB and last bit data is control bit.
Control bit is high level when divide factor of programmable reference divider is set. Control bit is set low level when divide factor of programmable divider is set.

Clock: Clock input for 16-bit shift registers and control register. Data is input into internal shift registers by rising edge of the clock.

LE: Load enable input:
When LE is high, the data from shift register is latched into programmable reference divider or programmable divider depending upon the control bit setting.

PHASE DETECTOR OUTPUT WAVEFORM



RECOMMENDED OPERATING CONDITIONS

(V_{SS} = 0V)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power Supply Voltage	V_{DD}	4.5	5.0	5.5	V
Input Voltage	V_{IN}	V_{SS}		V_{DD}	V
Operating Temperature	Ta	-30		+60	°C

ELECTRICAL CHARACTERISTICS

(V_{SS} = 0V, V_{DD} = 5V, Ta = -30 to 60°C)

Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
High-level Input Voltage	Except fin and OSC_{IN}	V_{IH}		3.5	-	-	V
Low-level Input Voltage		V_{IL}		-	-	1.5	
Input Sensitivity	f_{in}	V_{fin}	Amplitude in AC coupling, Sine wave	1.0	-	-	V_{P-P}
	OSC_{IN}	V_{OSC}		1.0	-	-	
High-level Input Current	Except fin and OSC_{IN}	I_{IH}	$V_{IH} = V_{DD}$	-	1.0	-	µA
Low-level Input Current		I_{IL}	$V_{IL} = V_{SS}$	-	-1.0	-	
Input Current	f_{in}	I_{fin}	$V_{IN} = V_{SS}$ to V_{DD}	-	±50	-	µA
	OSC_{IN}	I_{OSC}	$V_{IN} = V_{SS}$ to V_{DD}	-	±50	-	
High-level Output Voltage	Except OSC_{OUT}	V_{OH}	I_{OH} = 0µA	4.95	-	-	V
Low-level Output Voltage		V_{OL}	I_{OL} = 0µA	-	-	0.05	
High-level Output Current	Except OSC_{OUT}	I_{OH}	V_{OH} = 4.6V	-1.0	-	-	mA
Low-level Output Current		I_{OL}	V_{OL} = 0.4V	1.0	-	-	
Power Dissipation*1		I_{DDOP}		-	8.0	-	mA
Stand-by Current*2		I_{DDS}		-	100	-	µA
Maximum Operating*3 Frequency	REF Section	f_{maxd}		40	60	-	MHz
	PD Section	f_{maxp}		180	250	-	MHz

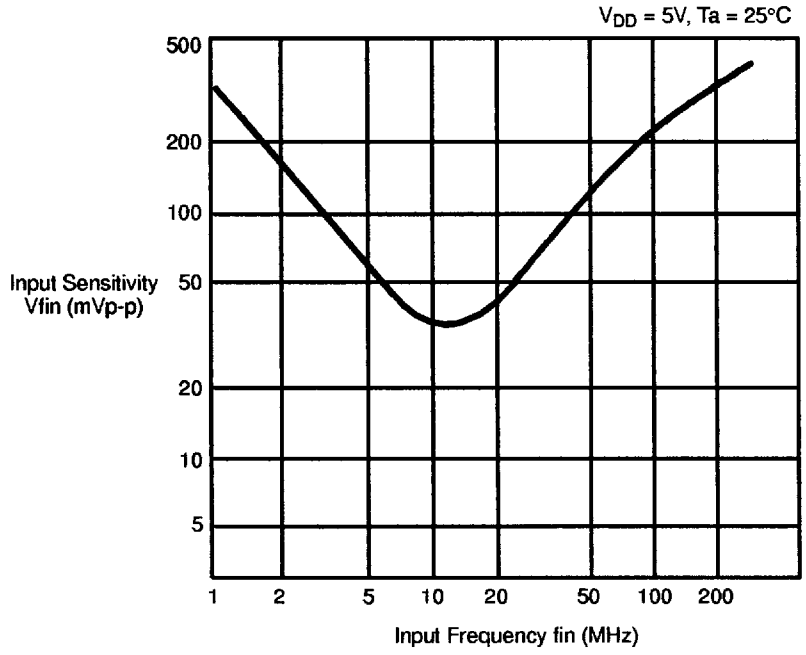
Notes: *1: f_{in} = 180MHz, 22MHz crystal is connected between OSC_{IN} and OSC_{OUT} pins. Inputs are grounded except f_{in} and OSC_{IN}. Outputs are open.

*2 All serial data is set to zero. Input are grounded except f_{in} and OSC_{IN}. Output are open.

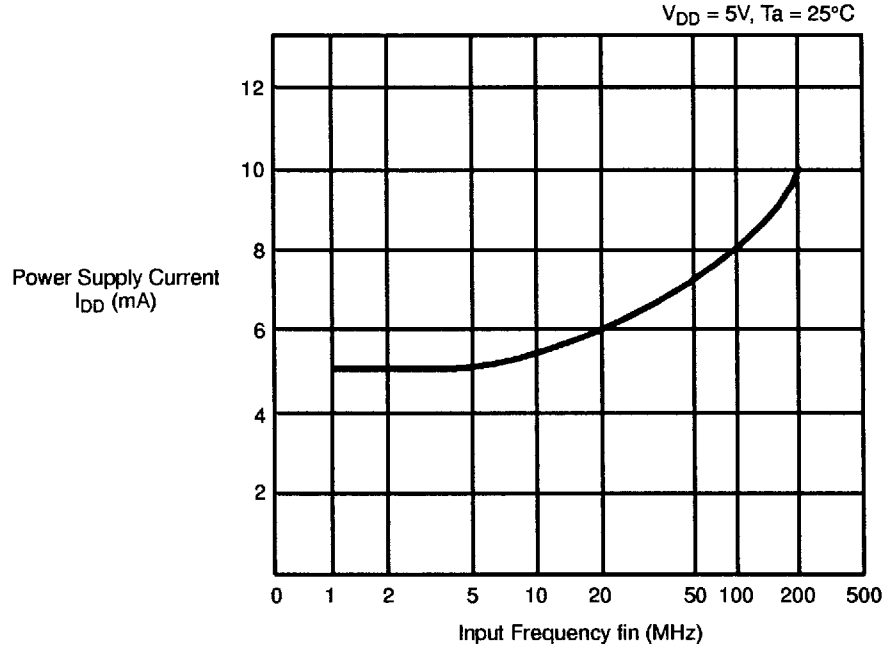
*3 REF Section :Maximum operating frequency of programmable reference divider.
PD Section :Maximum operating frequency of programmable divider.

TYPICAL CHARACTERISTICS CURVES

Input Sensitivity vs. Input Frequency (fin Section)

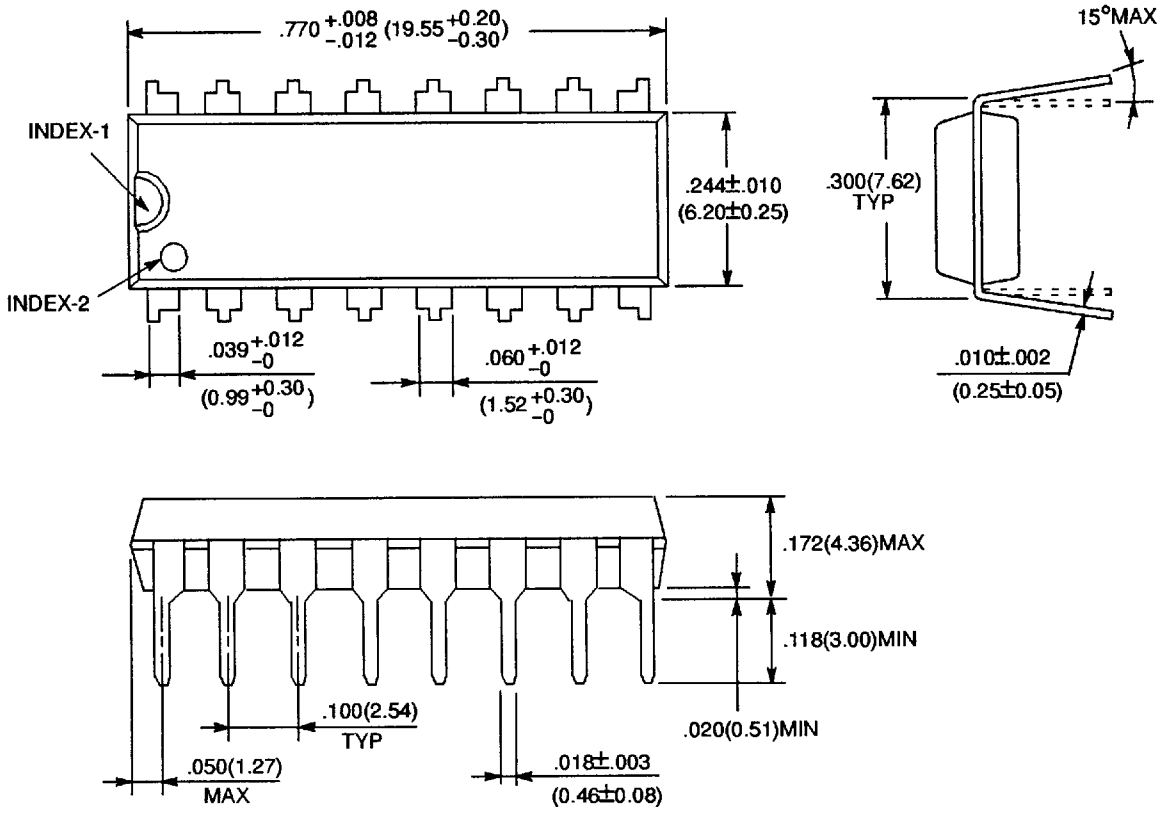


Power Supply Current vs. Input Frequency



PACKAGE DIMENSION

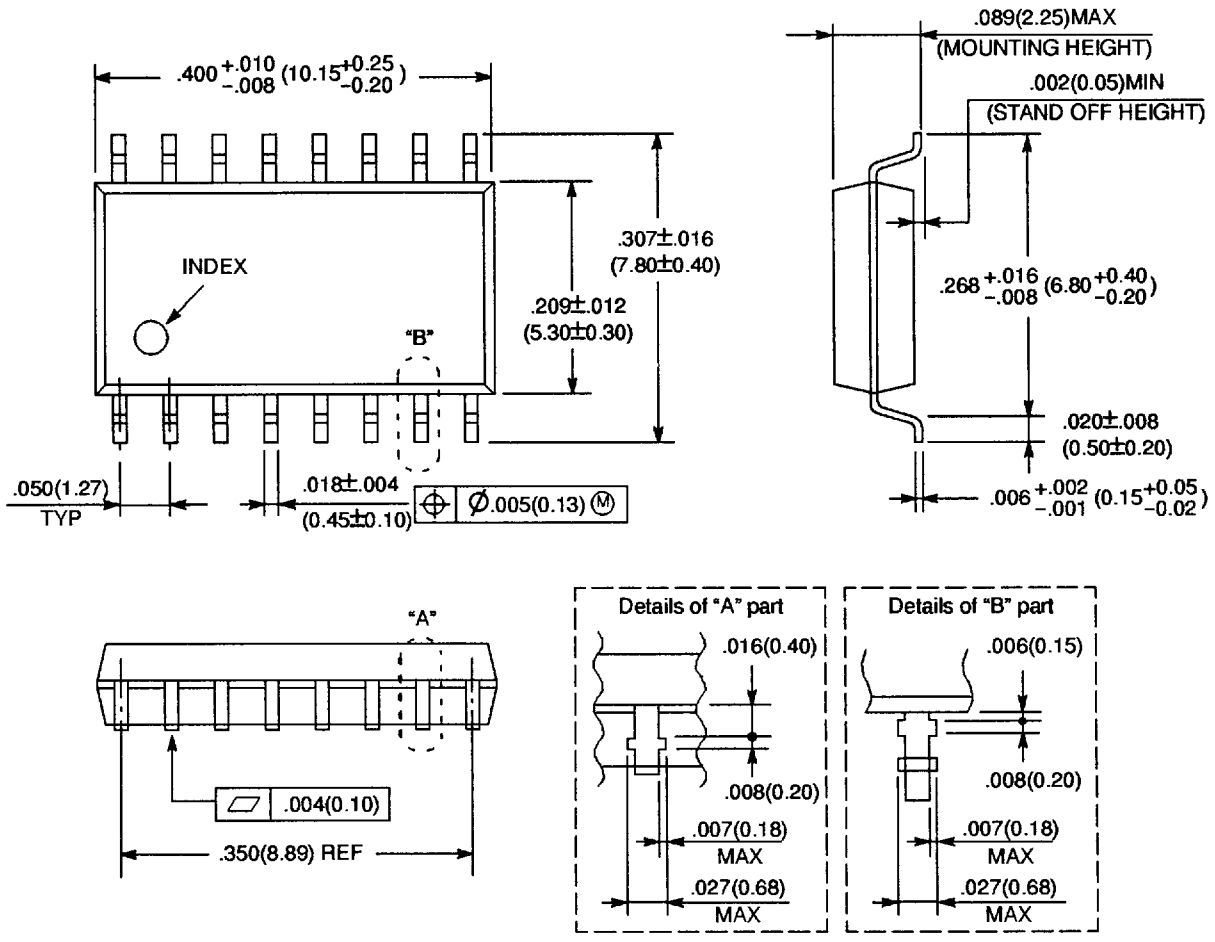
16-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-16P-M04)



Dimensions in
inches (millimeters)

PACKAGE DIMENSION (Continued)

16-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-16P-M06)



Dimensions in
inches (millimeters)

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