

## LINEAR IC

# R-2R TYPE 8-BIT D/A CONVERTER WITH OPERATIONAL AMPLIFIER OUTPUT BUFFERS

## MB88346B

### ■ DESCRIPTION

The Fujitsu MB88346B is an R-2R type 8-bit resolution digital-to-analog converter (DAC), designed for interface with a wide range of general 4-bit and 8-bit microcontrollers including Fujitsu's MB88200 family, MB8850 family, and MB88500 family 4-bit single-chip microcontrollers.

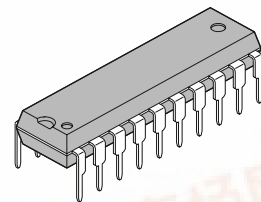
The MB88346B has an 8-bit x 12-channel D/A converter with operational amplifier output buffers. Digital data are input serially by individual channel units. The loaded digital data are converted into analog DC voltages by the D/A converter in 20  $\mu$ s settling time. Also, the MB88346B has operational amplifier output buffers. These operational amplifier output buffers are connected to each channel of the D/A converter, and provide high current drive capability. The MB88346B is suitable for electronic volumes and replacement for potentiometers for adjustment, in addition to normal D/A converter applications.

### ■ FEATURES

- Conversion method : R-2R resistor ladder
- 8-bit x 12-channel D/A converter with operational amplifier output buffers
- Max. 2.5MHz Serial data input
- Serial data output for cascade connection
- Max. 20  $\mu$ s DAC output settling time
- Max. +1.0/-1.0 mA analog output sink/source current
- Two separate power supply/ground lines for MCU interface block/operational amplifier output buffer block and D/A converter block
- Pin compatible with MB88341
- Single +5V power supply
- Wide operating temperature range: -20°C to +85°C
- Silicon-gate CMOS process
- Three package options :

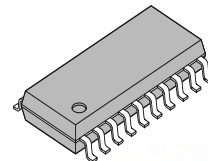
20-pin plastic DIP (Suffix : -P), 20-pin plastic SOP (Suffix : -PF),  
20-pin plastic SSOP (Suffix : -PFV)

MB88346B-P



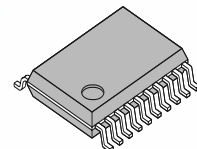
PLASTIC DIP  
(DIP-20P-M02)

MB88346B-PF



PLASTIC SOP  
(FPT-20P-M01)

MB88346B-PFV



PLASTIC SSOP  
(FPT-20P-M03)

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

# MB88346B

## ■ PIN ASSIGNMENT

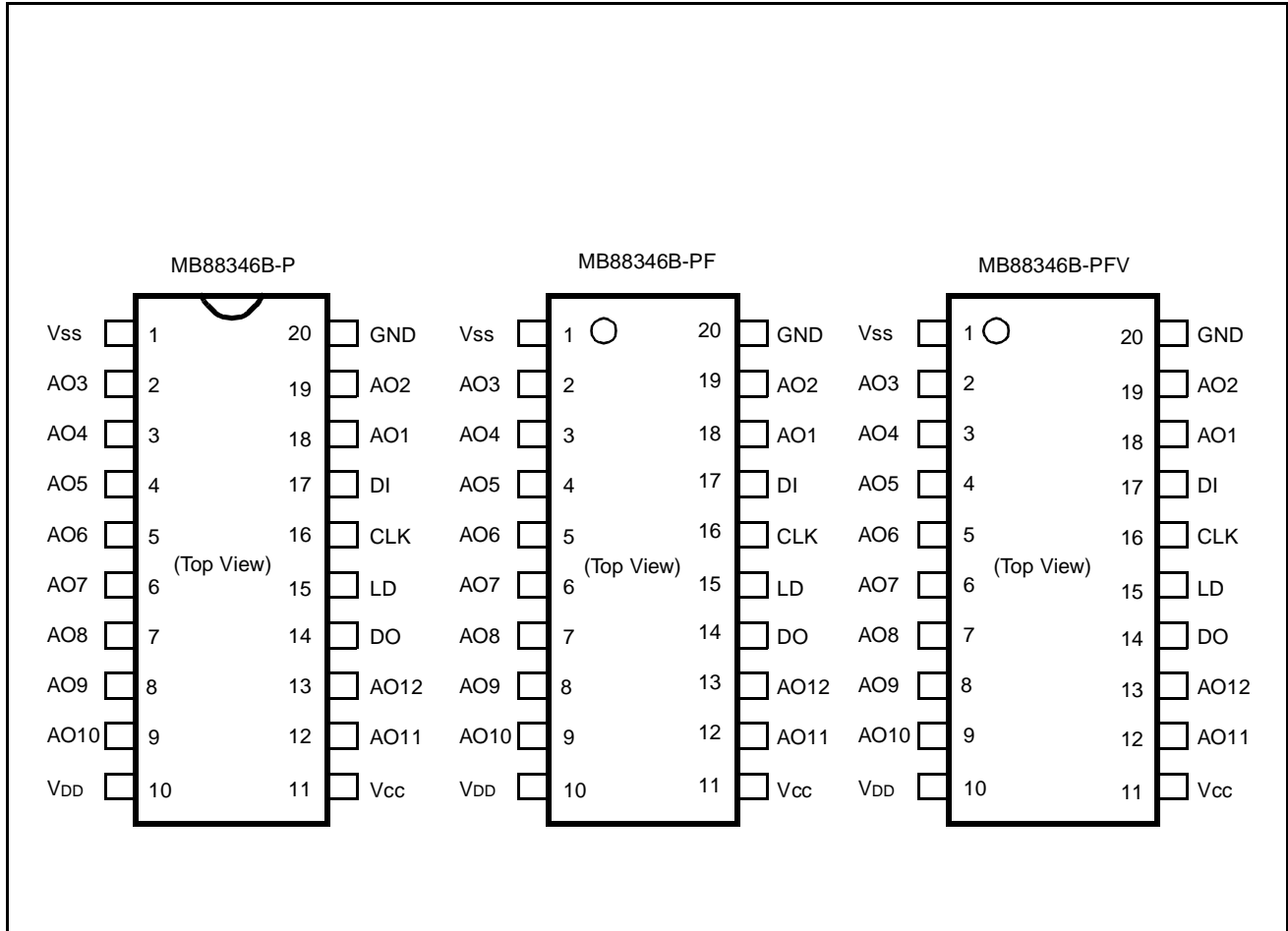
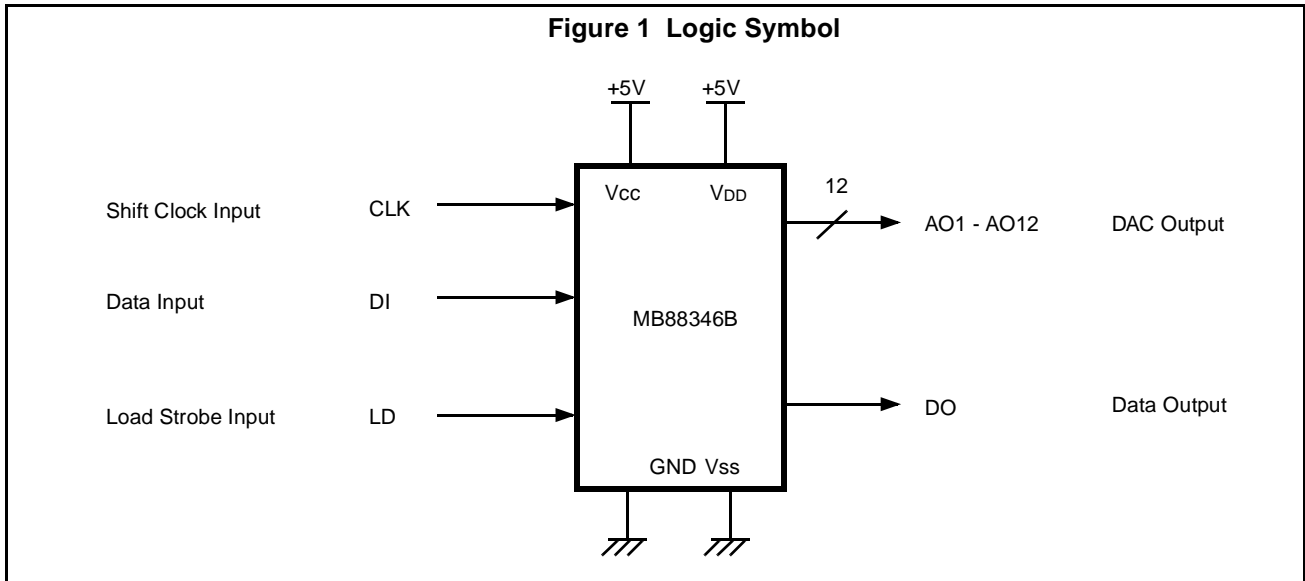
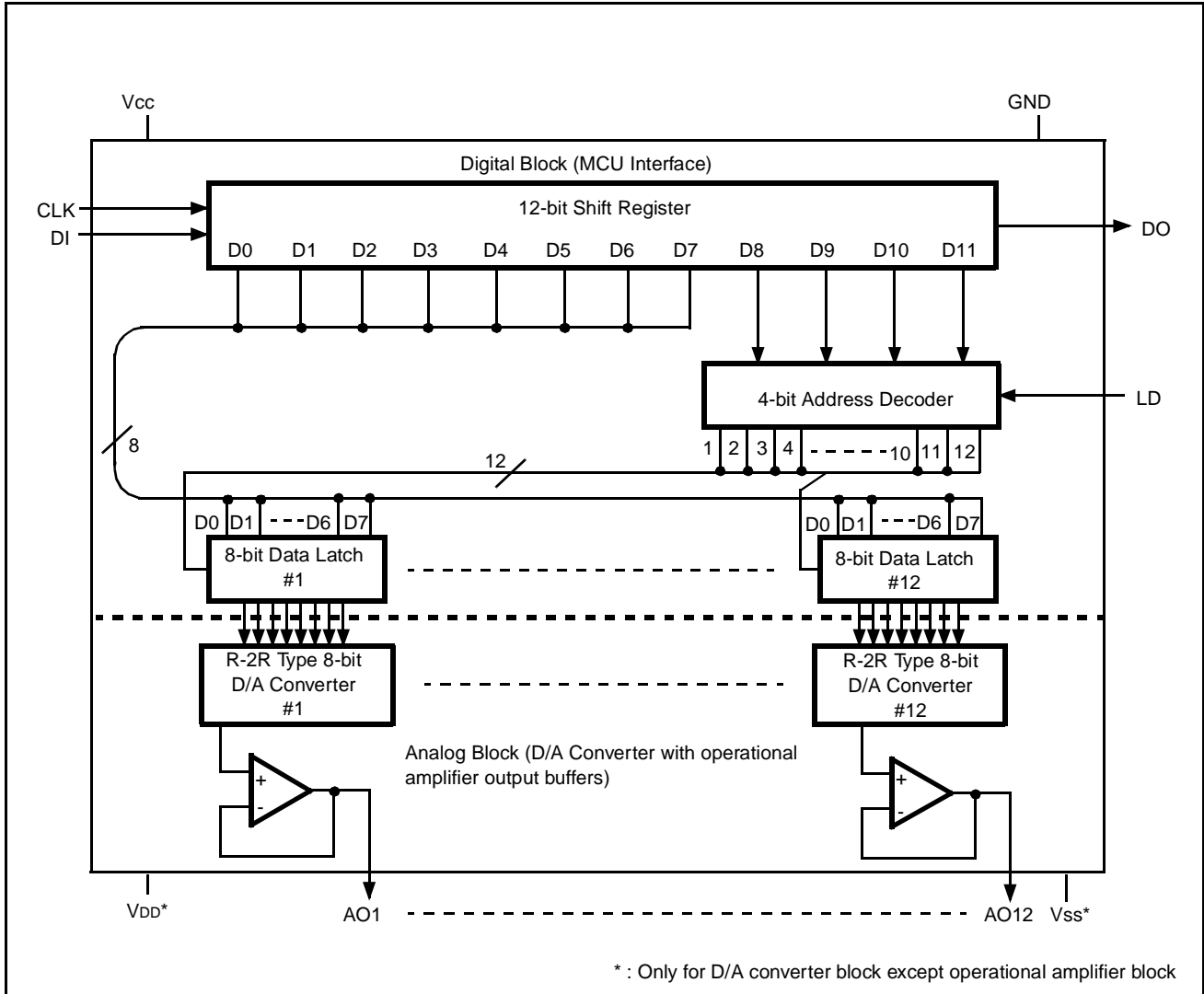


Figure 1 Logic Symbol



## ■ BLOCK DIAGRAM



# MB88346B

## ■ PIN DESCRIPTION

PIN ASSIGNMENT and Tables show the pin assignment and pin description of the MB88346B.

**Table 1 Pin Description**

Symbol	Pin No.	Type	Name & Function
<b>Power Supply</b>			
VCC	11	-	+5V DC power supply pin for the digital block (MCU interface) and operational amplifier output buffers.
GND	20	-	Ground pin for the digital block (MCU interface) and operational amplifier output buffers.
VDD	10	-	DC power supply pin for the analog block (D/A converter) except operational amplifier output buffers.
VSS	1	-	Ground pin for the analog block (D/A converter) except operational amplifier output buffers.
<b>Control Input</b>			
CLK	16	I	Shift clock input to the internal 12-bit shift register: At the rising edge of CLK data on the DI pin is shifted into the LSB of the shift register and contents of the shift register are shifted right (to the MSB).
LD	15	I	Load strobe input for a 12-bit address/data : A high level on the LD pin latches a 4-bit address (upper 4 bits: D11 to D8) of the internal 12-bit shift register into the internal address decoder, and writes 8-bit data (lower 8 bits: D7 to D0) of the shift register into an internal data latch selected by the latched address.
<b>Data Input/Output</b>			
DI	17	I	Serial address/data input to the internal 12-bit shift register: The address/data format is that upper 4 bits (D11 to D8) indicate an address and lower 8 bits (D7 to D0) indicate data. The D11 (MSB) is the first-in bit and D0 (LSB) is the last-in bit.
DO	14	O	Serial address/data output from the internal 12-bit shift register: This is an output pin of the MSB bit data of the 12-bit shift register. This pin allows a cascade connection of the device.
<b>DAC Output</b>			
AO1	18	O	8-bit resolution D/A converter outputs : 12 channels of DAC outputs (AO1 to AO12) are provided.  Each output channel has an operational amplifier output buffer for analog output data.
AO2	19		
AO3	2		
AO4	3		
AO5	4		
AO6	5		
AO7	6		
AO8	7		
AO9	8		
AO10	9		
AO11	12		
AO12	13		

## ■ FUNCTIONAL DESCRIPTION

### OVERVIEW

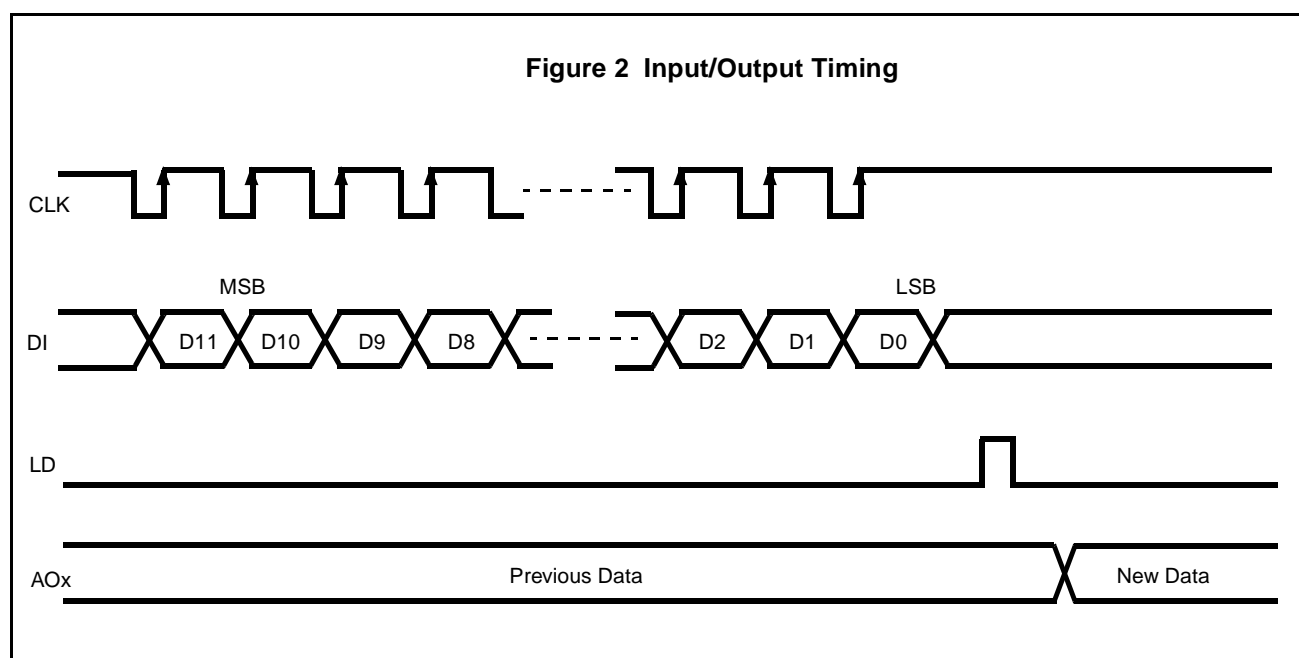
The MB88346B is an R-2R resistor ladder type, 8-bit resolution digital-to-analog converter (DAC) device. The MB88346B has 12 channels of D/A converters with operational amplifier output buffers. 8-bit digital data are loaded into internal data latches by individual DAC channel units. The loaded digital data are converted into analog DC voltages through the internal D/A converter in max. 20  $\mu$ s settling time. And the analog DC voltages source/sink the output current through the operational amplifier output buffers. For cascade connection, a serial data output is provided.

### DEVICE CONFIGURATION

As illustrated in BLOCK DIAGRAM, the MB88346B device is composed by the digital block (MCU interface) and analog block (D/A converter with operational amplifier output buffers). The digital block consists of a 12-bit shift register, a 4-bit address decoder, and 12-channels of 8-bit data latches. The analog block includes 12 channels of 8-bit D/A converters with operational amplifier output buffers connecting to the data latches. For electrically stable operation the power supply and ground lines are separate between the digital block (MCU interface) and operational amplifier output buffers, and analog block except operational amplifier output buffers.

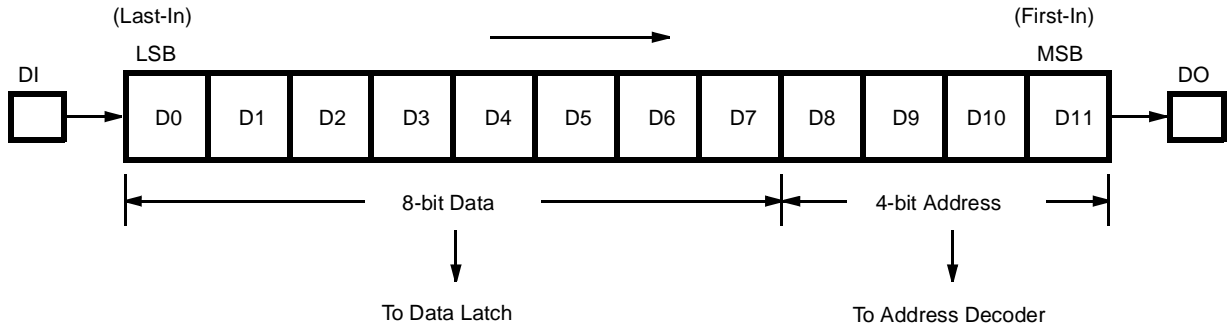
### DEVICE OPERATION

Figure 2 shows the input/output timing. A 12-bit address/data is serially input into the shift register through the DI pin synchronously with the rising edge of CLK. The format of the shift register is shown in Figure 3. The lower 8 bits (D7 to D0) are data bits to be converted, and the upper 4 bits (D11 to D8) are address bits (D11 to D8) to select a data latch to be written. A high level on the LD pin loads the address decoder with the 4-bit address to select a data latch, and writes the 8-bit data into a selected data latch. Figure 4 shows the data latch address map, and Table, address decoding. 8-bit data written into individual data latches are converted into analog DC voltages, dividing the supply voltage  $|V_{DD}-V_{SS}|$  through R-2R resistor ladders of D/A converters. The operational amplifier output buffers at individual D/A converter outputs can source up to 1.0 mA of the output current. Figure 5 shows a configuration of the R-2R resistor ladder D/A converter with operational amplifier, and Table 3 analog DC voltages corresponding to each digital data.



# MB88346B

**Figure 3 Shift Register Format**



**Figure 4 Data Latch Address Map**

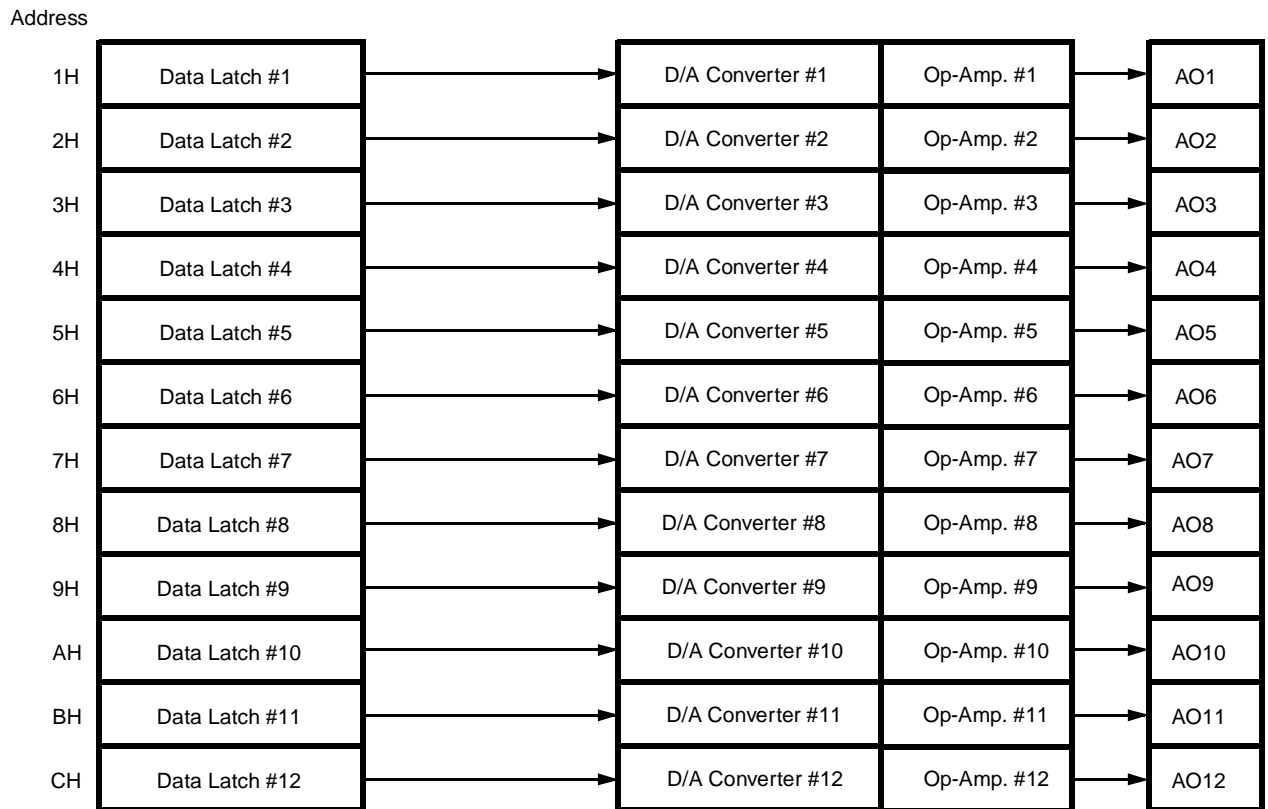
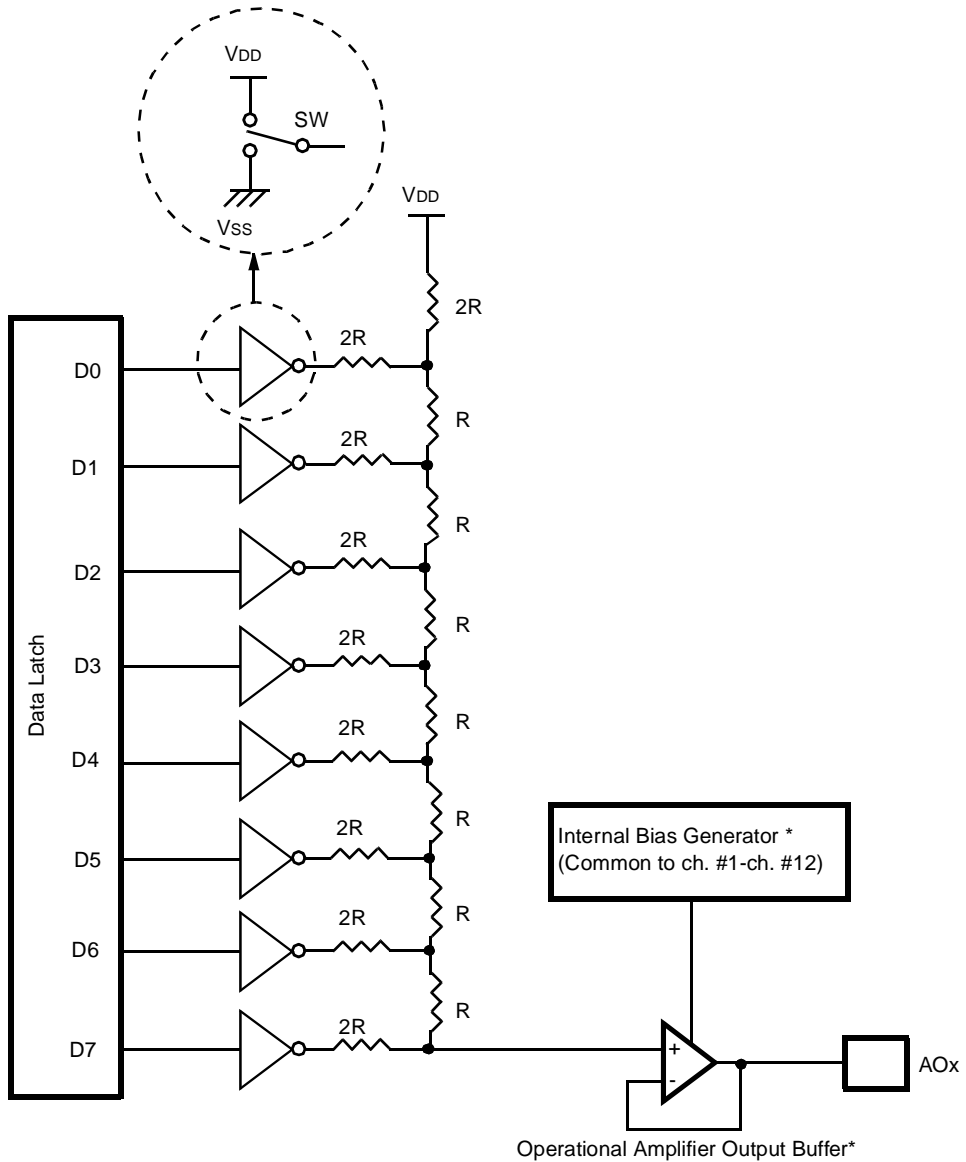


Figure 5 Configuration of R-2R Resistor Ladder D/A Converter



\* : Powered/grounded by the Vcc and GND pins.

# MB88346B

Table 2 Address Decoding

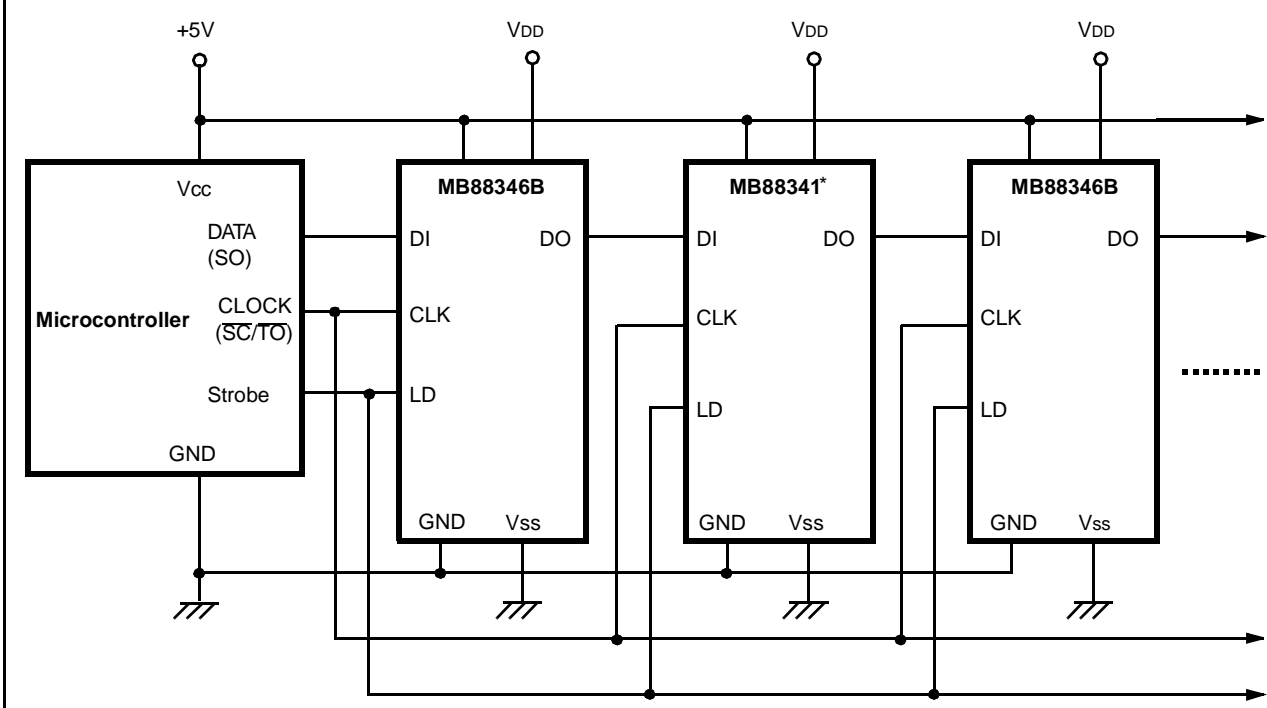
Address				Data Latch Selected
D8	D9	D10	D11	MB88346B
0	0	0	0	Deselected
0	0	0	1	Data Latch #1
0	0	1	0	Data Latch #2
0	0	1	1	Data Latch #3
0	1	0	0	Data Latch #4
0	1	0	1	Data Latch #5
0	1	1	0	Data Latch #6
0	1	1	1	Data Latch #7
1	0	0	0	Data Latch #8
1	0	0	1	Data Latch #9
1	0	1	0	Data Latch #10
1	0	1	1	Data Latch #11
1	1	0	0	Data Latch #12
1	1	0	1	Deselected
1	1	1	0	Deselected
1	1	1	1	Deselected

Table 3 Data Conversion

Data								DAC Output Level
D7	D6	D5	D4	D3	D2	D1	D0	AOx
0	0	0	0	0	0	0	0	$\approx V_{SS}$
0	0	0	0	0	0	0	1	$\approx (V_{DD}-V_{SS}) \times 1/255 + V_{SS}$
0	0	0	0	0	0	1	0	$\approx (V_{DD}-V_{SS}) \times 2/255 + V_{SS}$
0	0	0	0	0	0	1	1	$\approx (V_{DD}-V_{SS}) \times 3/255 + V_{SS}$
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	1	1	1	1	1	1	0	$\approx (V_{DD}-V_{SS}) \times 254/255 + V_{SS}$
1	1	1	1	1	1	1	1	$\approx V_{DD}$



Figure 6 Cascade Connection Example

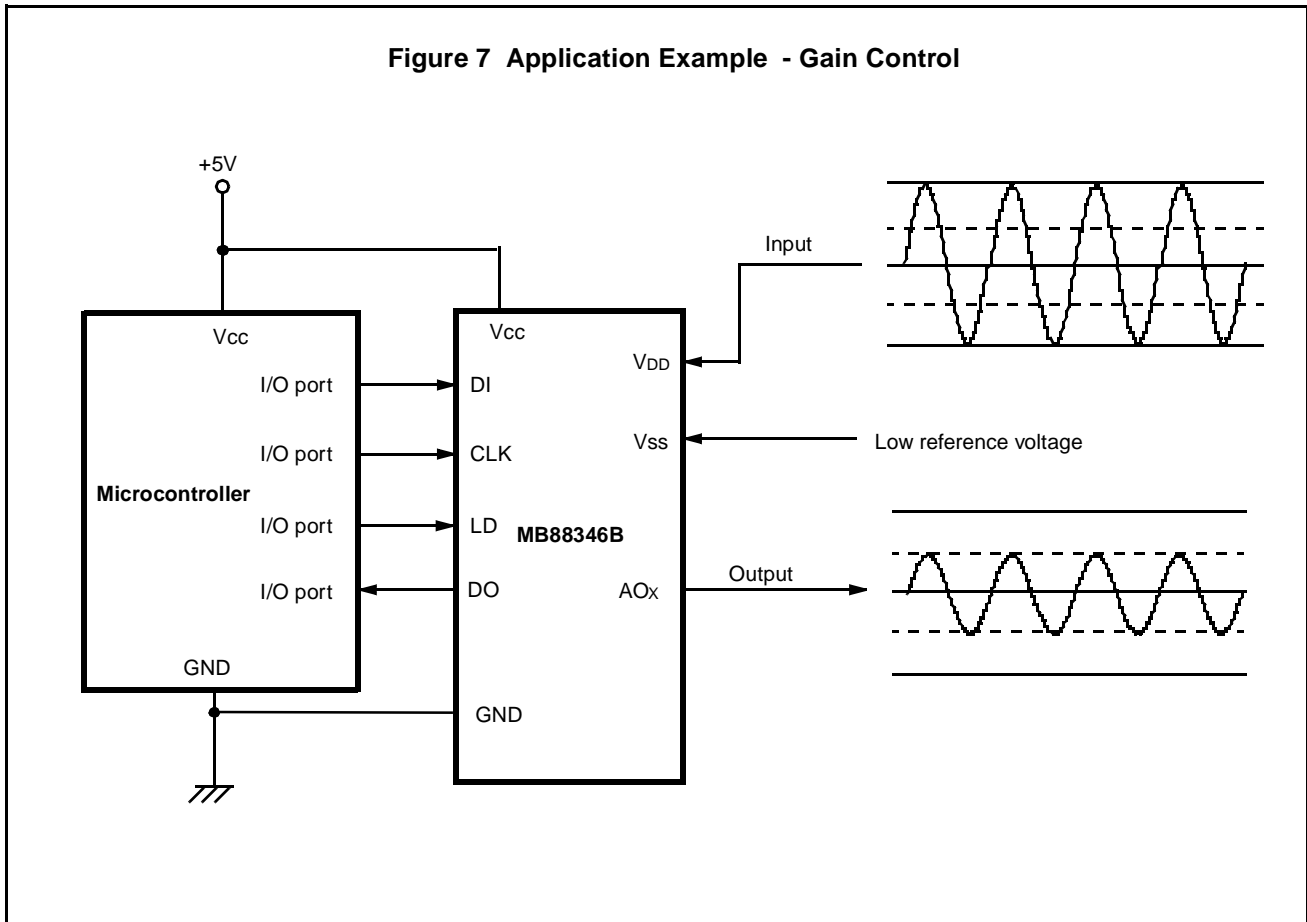


\* : MB88346B can be used mixed with MB88341.

# MB88346B

## ■ APPLICATION DESCRIPTION

The MB88346B is suitable for electronic volumes and replacement for adjustment potentiometers, in addition to normal D/A converter applications. Figure 7 illustrates application example for a gain control.



## ■ ELECTRICAL CHARACTERISTICS

### ABSOLUTE MAXIMUM RATINGS (See NOTE)

Parameter	Symbol	Rating			Unit	Condition
		Min	Typ	Max		
Supply Voltage	V <sub>CC</sub>	-0.3	-	7.0	V	T <sub>a</sub> = +25°C GND = 0 V V <sub>DD</sub> ≤ V <sub>CC</sub> ,
	V <sub>DD</sub>	-0.3	-	7.0	V	
Input Voltage	V <sub>IN</sub>	-0.3	-	V <sub>CC</sub> +0.3	V	T <sub>a</sub> = +25°C GND = 0 V
Output Voltage	V <sub>OUT</sub>	-0.3	-	V <sub>CC</sub> +0.3	V	
Power Dissipation	P <sub>D</sub>	-	-	250	mW	
Operating Ambient Temperature	T <sub>a</sub>	-20	-	+85	°C	
Storage Temperature	T <sub>STG</sub>	-55	-	+150	°C	

NOTE : Permanent device damage may occur if the above ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit	Condition
		Min	Typ	Max		
Supply Voltage (for MCU Interface/Op.-Amp. Block)	V <sub>CC</sub>	4.5	5.0	5.5	V	V <sub>CC</sub> ≥ V <sub>DD</sub>
	GND	-	0	-	V	
Supply Voltage (for Analog Block*)	V <sub>CC</sub>	2.0	-	V <sub>CC</sub>	V	V <sub>DD</sub> -V <sub>SS</sub> ≥ 2.0V
	V <sub>SS</sub>	GND	-	V <sub>CC</sub> -2.0	V	
Analog Output Source Current	I <sub>AL</sub>	-	-	+1.0	mA	
Analog Output Sink Current	I <sub>AH</sub>	-	-	+1.0	mA	
Analog Output Load Capacitance for oscillation limit	C <sub>AL</sub>	-	-	1.0	μF	
Operating Ambient Temperature	T <sub>a</sub>	-20	-	+85	°C	

\* : Except operational amplifier output buffer block

# MB88346B

## ■ DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

### Digital Block (MCU Interface)

Parameter	Symbol	Value			Unit	Condition
		Min	Typ	Max		
Active Supply Current (V <sub>CC</sub> ) *	I <sub>CC</sub>	-	2.5	4.5	mA	CLK = 1MHz, Unloaded
Input Leakage Current (CLK, DI, and LD)	I <sub>ILK</sub>	-10	-	+10	μA	V <sub>IN</sub> = 0 to V <sub>CC</sub>
Input Low Voltage (CLK, DI, and LD)	V <sub>IL</sub>	-	-	0.2•V <sub>CC</sub>	V	
Input High Voltage (CLK, DI, and LD)	V <sub>IH</sub>	0.5•V <sub>CC</sub>	-	-	V	
Output Low Voltage (DO)	V <sub>OL</sub>	-	-	0.4	V	I <sub>OL</sub> = 2.5 mA
Output High Voltage (DO)	V <sub>OH</sub>	V <sub>CC</sub> -0.4	-	-	V	I <sub>OH</sub> = -400 μA

\* : Including the supply current to the operational amplifier block

### Analog Block (D/A Converters with Operational Amplifier Output Buffers)

Parameter	Symbol	Value			Unit	Condition
		Min	Typ	Max		
Supply Current (V <sub>DD</sub> ) **	I <sub>DD</sub>	-	0.2	0.5	mA	Unloaded
Min. Analog Output Voltage 1 (AO <sub>x</sub> )	VAOL1	V <sub>SS</sub>	-	V <sub>SS</sub> +0.1	V	V <sub>DD</sub> =V <sub>CC</sub> , V <sub>SS</sub> =GND=0V Unloaded, Digital Data=#00
Min. Analog Output Voltage 2 (AO <sub>x</sub> )	VAOL2	V <sub>SS</sub> -0.2	V <sub>SS</sub>	V <sub>SS</sub> +0.2	V	V <sub>DD</sub> =V <sub>CC</sub> =5.0V, V <sub>SS</sub> =GND=0V I <sub>AL</sub> =+500μA, Digital Data=#00
Min. Analog Output Voltage 3 (AO <sub>x</sub> )	VAOL3	V <sub>SS</sub>	-	V <sub>SS</sub> +0.2	V	V <sub>DD</sub> =V <sub>CC</sub> =5.0V, V <sub>SS</sub> =GND=0V I <sub>AH</sub> =+500μA, Digital Data=#00
Min. Analog Output Voltage 4 (AO <sub>x</sub> )	VAOL4	V <sub>SS</sub> -0.3	V <sub>SS</sub>	V <sub>SS</sub> +0.3	V	V <sub>DD</sub> =V <sub>CC</sub> =5.0V, V <sub>SS</sub> =GND=0V I <sub>AL</sub> =+1.0mA, Digital Data=#00
Min. Analog Output Voltage 5 (AO <sub>x</sub> )	VAOL5	V <sub>SS</sub>	-	V <sub>SS</sub> +0.3	V	V <sub>DD</sub> =V <sub>CC</sub> =5.0V, V <sub>SS</sub> =GND=0V I <sub>AH</sub> =+1.0mA, Digital Data=#00
Max. Analog Output Voltage 1 (AO <sub>x</sub> )	VAOH1	V <sub>DD</sub> -0.1	-	V <sub>DD</sub>	V	V <sub>DD</sub> =V <sub>CC</sub> , V <sub>SS</sub> =GND=0V Unloaded, Digital Data=#FF
Max. Analog Output Voltage 2 (AO <sub>x</sub> )	VAOH2	V <sub>DD</sub> -0.2	-	V <sub>DD</sub>	V	V <sub>DD</sub> =V <sub>CC</sub> =5.0V, V <sub>SS</sub> =GND=0V I <sub>AL</sub> =+500μA, Digital Data=#FF
Max. Analog Output Voltage 3 (AO <sub>x</sub> )	VAOH3	V <sub>DD</sub> -0.2	V <sub>DD</sub>	V <sub>DD</sub> +0.2	V	V <sub>DD</sub> =V <sub>CC</sub> =5.0V, V <sub>SS</sub> =GND=0V I <sub>AH</sub> =+500μA, Digital Data=#FF

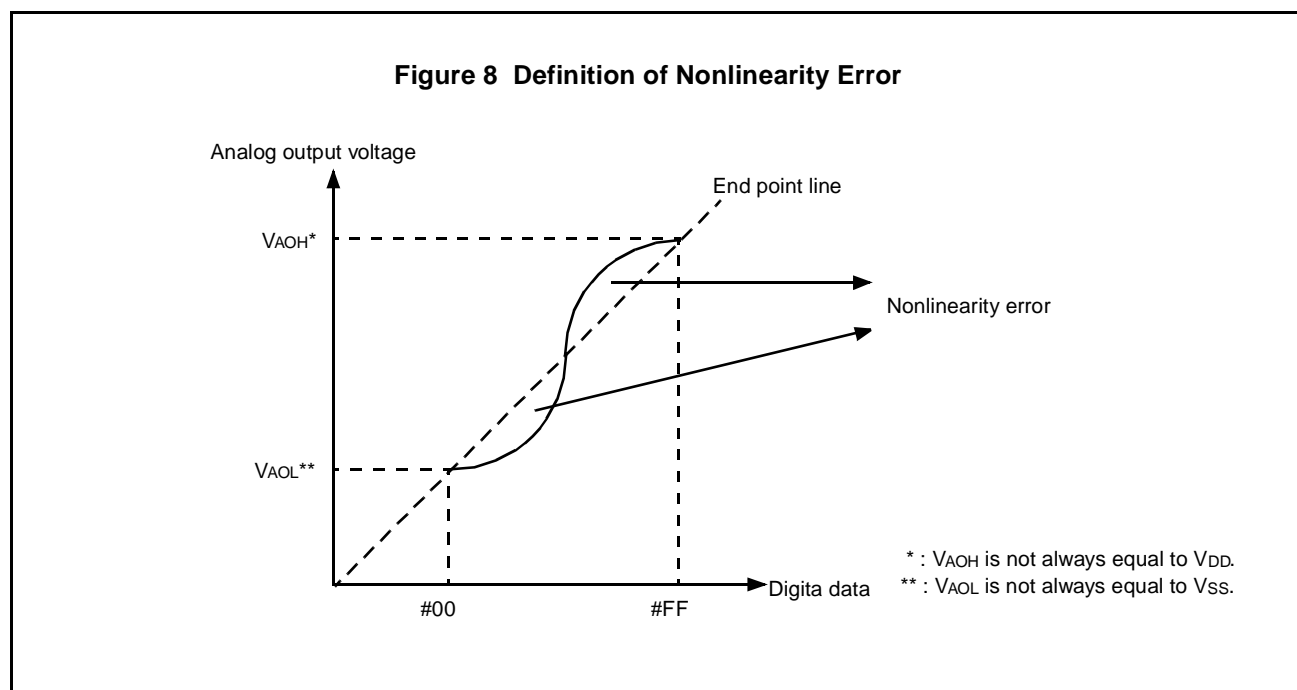
\*\* : Excluding the supply current to the operational amplifier block

## Analog Block (D/A Converters with Operational Amplifier Output Buffers) - Continued

Parameter	Symbol	Value			Unit	Condition
		Min	Typ	Max		
Max. Analog Output Voltage 4 (AO <sub>x</sub> )	VAOH4	V <sub>DD</sub> -0.3	-	V <sub>DD</sub>	V	V <sub>DD</sub> =V <sub>CC</sub> =5V, V <sub>SS</sub> =GND=0V, I <sub>AL</sub> =+1.0mA, Digital Data=#FF
Max. Analog Output Voltage 5 (AO <sub>x</sub> )	VAOH5	V <sub>DD</sub> -0.3	V <sub>DD</sub>	V <sub>DD</sub> +0.3	V	V <sub>DD</sub> =V <sub>CC</sub> =5V, V <sub>SS</sub> =GND=0V, I <sub>AH</sub> =+1.0mA, Digital Data=#FF
Resolution (AO <sub>x</sub> )	Res	-	8	-	bit	Monotonicity
Differential Error* (AO <sub>x</sub> )	DE	-1.0	0	+1.0	LSB	Unloaded, V <sub>DD</sub> ≤V <sub>CC</sub> -0.1V, V <sub>SS</sub> ≥0.1V
Nonlinearity Error** (AO <sub>x</sub> )	LE	-1.5	0	+1.5	LSB	Unloaded, V <sub>DD</sub> ≤V <sub>CC</sub> -0.1V, V <sub>SS</sub> ≥0.1V, See Figure 8.

\* : The difference from the ideal increment value when the digital data is increased by 1 bit.

\*\* : The difference between the input-output curve for the straight line (ideal line) that connects the output voltage of the channel when #00 is set, and the output voltage when #FF is set.



# MB88346B

## ■ AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Value		Unit	Condition
		Min	Max		
Clock Low Time	tCLK	200	-	ns	
Clock High Time	tCKH	200	-	ns	
Clock Rise Time	tCr	-	200	ns	
Clock Fall Time	tCf	-	200	ns	
Data Setup Time	tDCH	30	-	ns	
Data Hold Time	tCHD	60	-	ns	
Load Strobe High Time	tLDH	100	-	ns	
Load Strobe Setup Time	tCHL	200	-	ns	
Load Strobe Hold Time	tLDC	100	-	ns	
DAC Output Settling Time	tLDD	-	20	μs	*RAL = 10 kΩ , CAL = 50 pF
Data Output Delay Time	tDO	70	350	ns	**CL = 20 pF (Min.), 100 pF (Max.)

Figure 9 AC Test Conditions

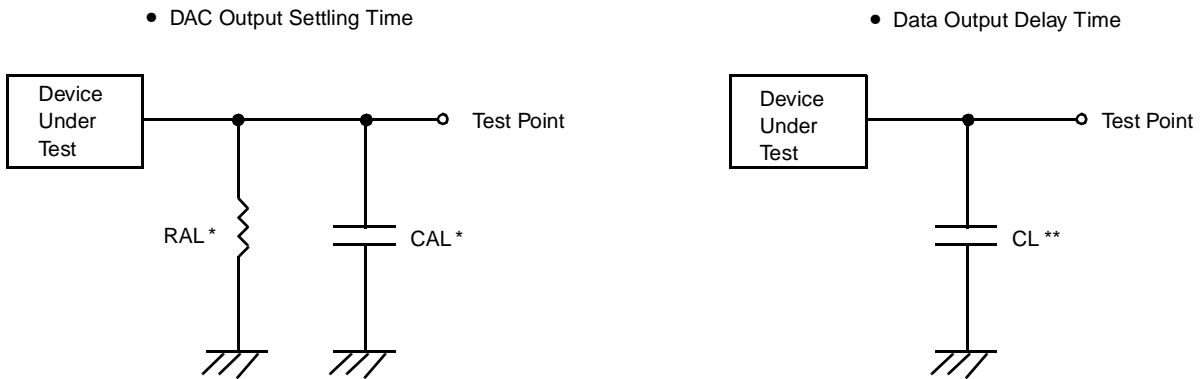
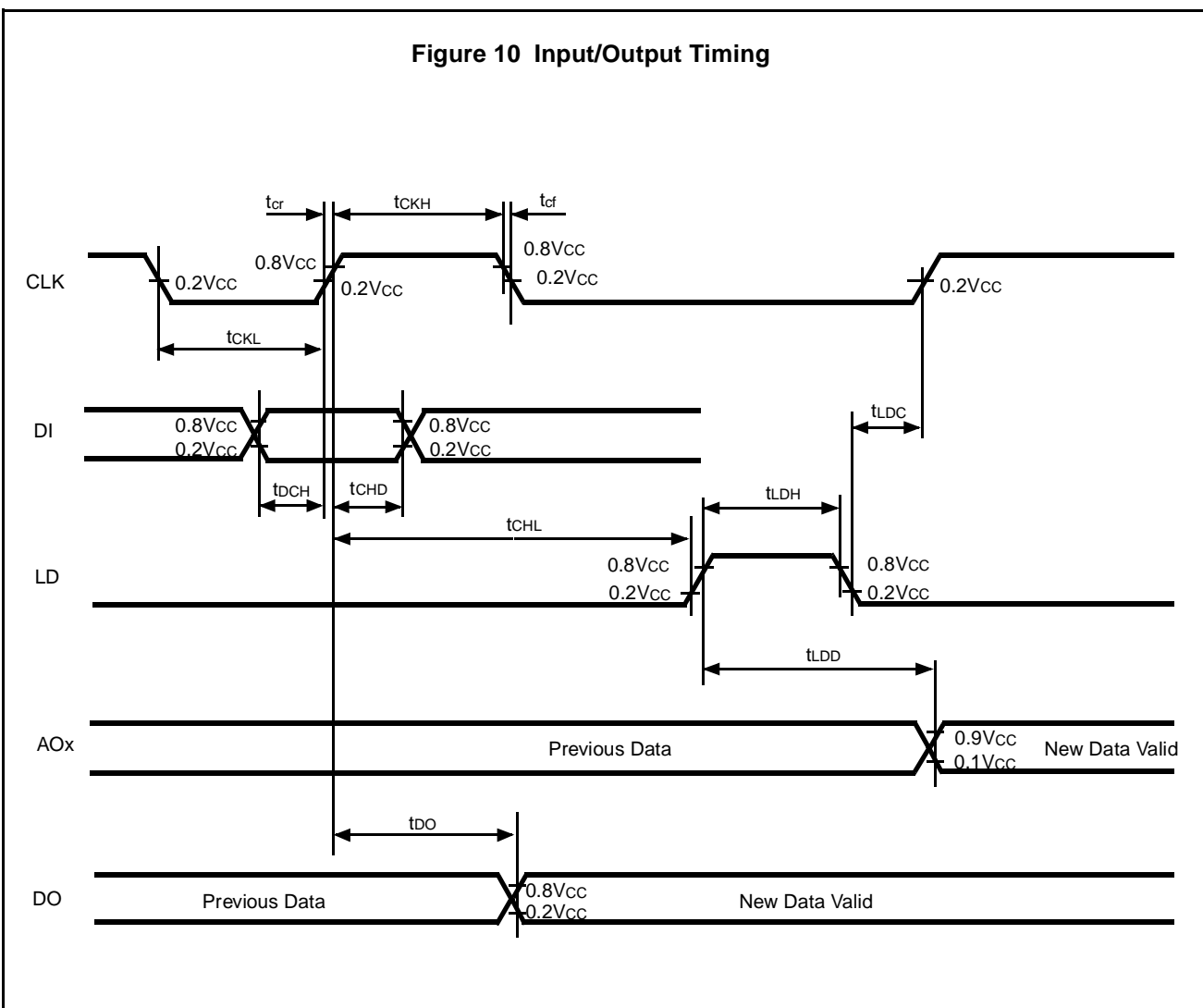
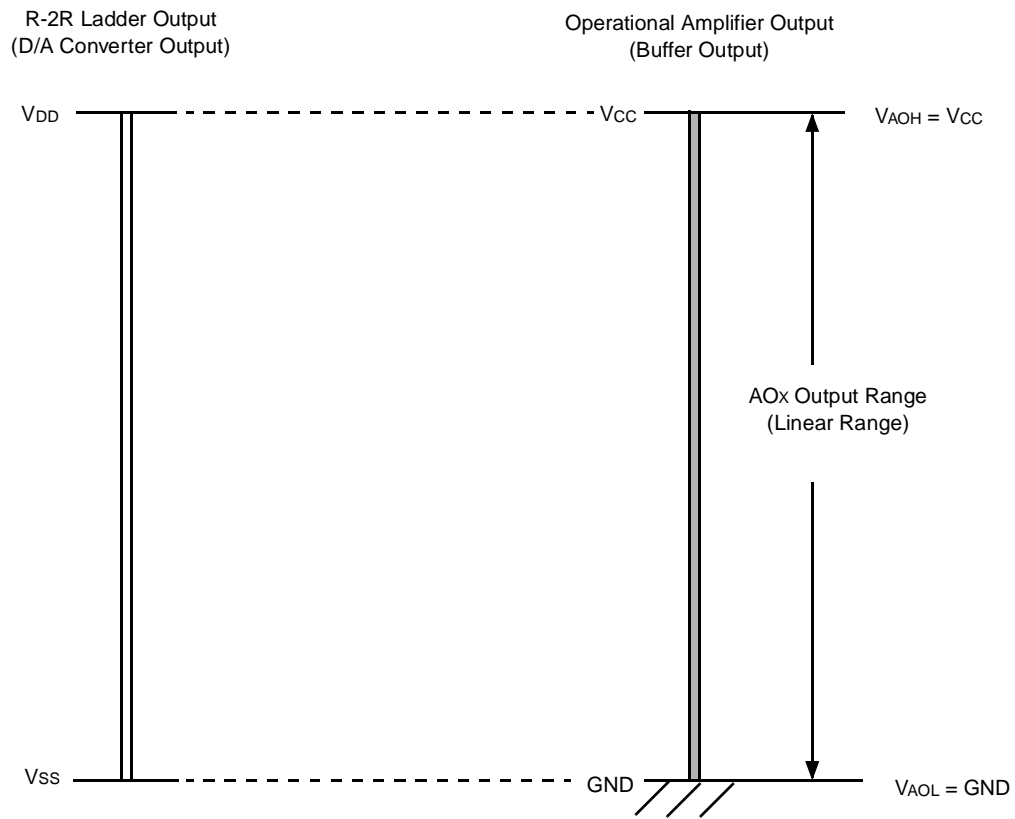


Figure 10 Input/Output Timing



# MB88346B

Figure 11 Analog Output Voltage Range



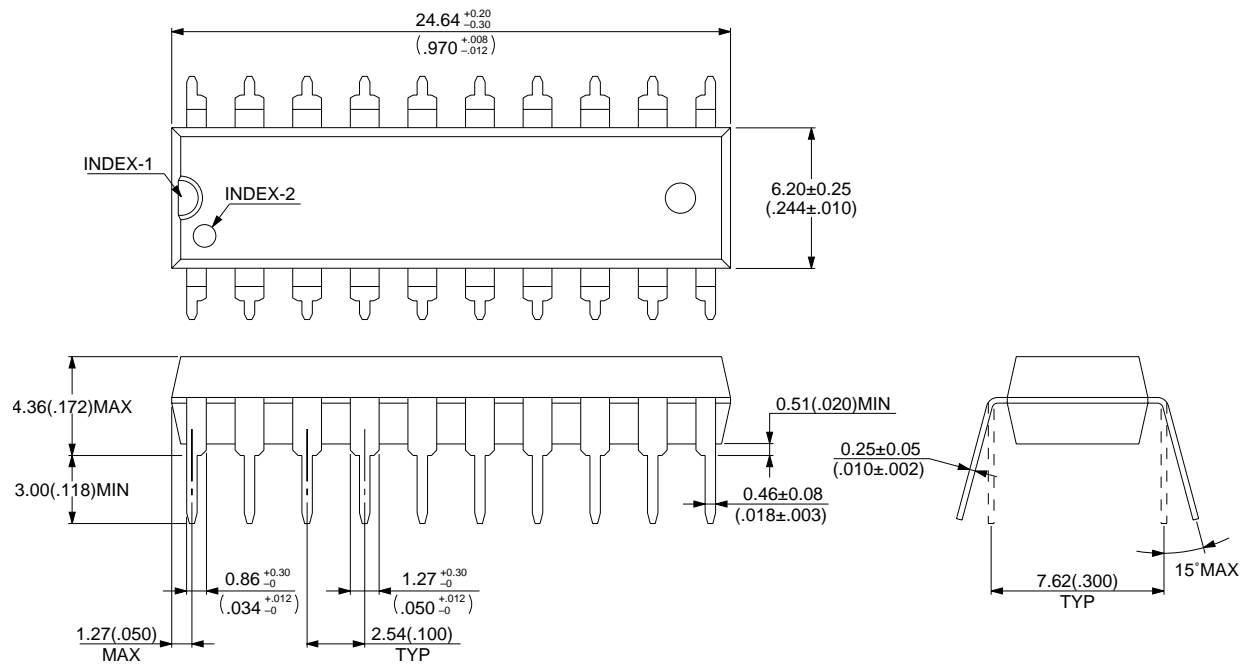
Notes:  $V_{DD}=V_{CC}$   
 $V_{SS}=GND$



## ■ PACKAGE DIMENSIONS

### MB88346B-P

20 pin, Plastic DIP  
(DIP-20P-M02)



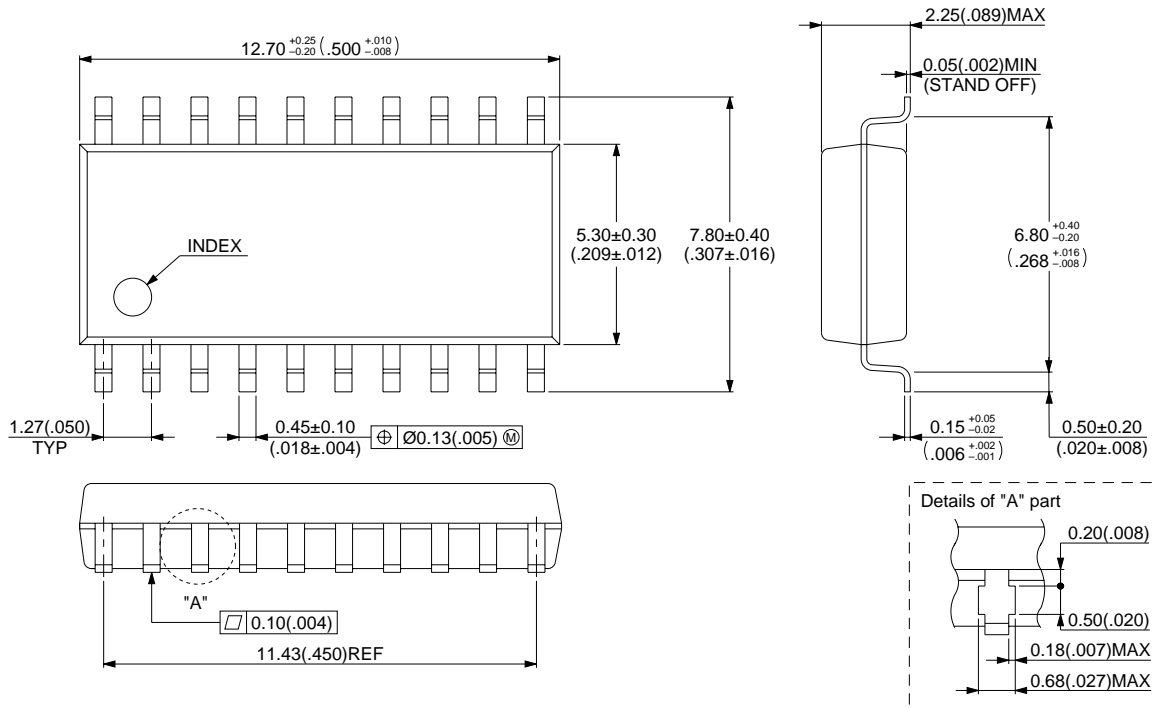
© 1994 FUJITSU LIMITED D20003S-3C-4

Dimensions in mm(inches).

# MB88346B

## MB88346B-PF

20 pin, Plastic SOP  
(FPT 20P-M01)

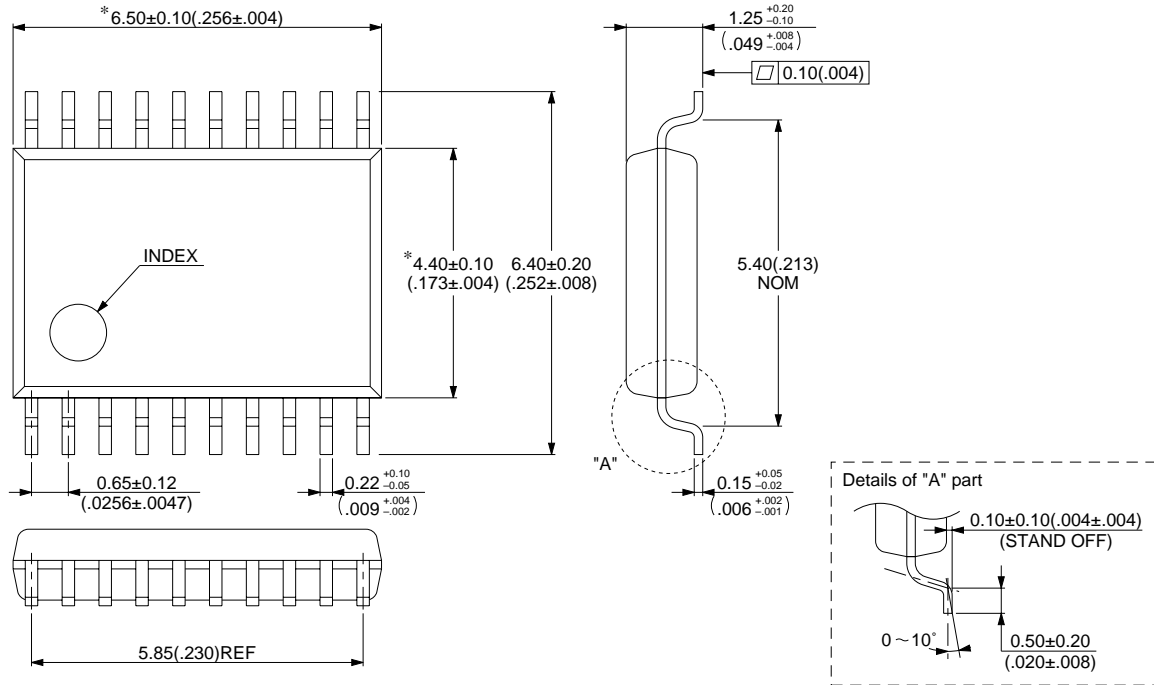


© 1994 FUJITSU LIMITED F20003S-5C-4

Dimensions in mm(inches).

## MB88346B-PFV

20 pin, Plastic SSOP  
(FPT-20P-M03)



© 1994 FUJITSU LIMITED F20012S-2C-4

Dimensions in mm(inches).

## FUJITSU LIMITED

*For further information please contact:*

### **Japan**

FUJITSU LIMITED  
Corporate Global Business Support Division  
Electronic Devices  
KAWASAKI PLANT, 4-1-1, Kamikodanaka  
Nakahara-ku, Kawasaki-shi  
Kanagawa 211-8588, Japan  
Tel: (044) 754-3763  
Fax: (044) 754-3329

<http://www.fujitsu.co.jp/>

### **North and South America**

FUJITSU MICROELECTRONICS, INC.  
Semiconductor Division  
3545 North First Street  
San Jose, CA 95134-1804, USA  
Tel: (408) 922-9000  
Fax: (408) 922-9179

Customer Response Center  
*Mon. - Fri.: 7 am - 5 pm (PST)*  
Tel: (800) 866-8608  
Fax: (408) 922-9179

<http://www.fujitsumicro.com/>

### **Europe**

FUJITSU MIKROELEKTRONIK GmbH  
Am Siebenstein 6-10  
D-63303 Dreieich-Buchsschlag  
Germany  
Tel: (06103) 690-0  
Fax: (06103) 690-122

<http://www.fujitsu-edc.com/>

### **Asia Pacific**

FUJITSU MICROELECTRONICS ASIA PTE LTD  
#05-08, 151 Lorong Chuan  
New Tech Park  
Singapore 556741  
Tel: (65) 281-0770  
Fax: (65) 281-0220

<http://www.fmap.com.sg/>

All Rights Reserved.

The contents of this document are subject to change without notice. Customers are advised to consult with FUJITSU sales representatives before ordering.

The information and circuit diagrams in this document presented as examples of semiconductor device applications, and are not intended to be incorporated in devices for actual use. Also, FUJITSU is unable to assume responsibility for infringement of any patent rights or other rights of third parties arising from the use of this information or circuit diagrams.

FUJITSU semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

#### **CAUTION:**

Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with FUJITSU sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

If any products described in this document represent goods or technologies subject to certain restrictions on export under the Foreign Exchange and Foreign Trade Control Law of Japan, the prior authorization by Japanese government should be required for export of those products from Japan.