FUJITSU SEMICONDUCTOR
DATA SHEET

DS07-12517-2E

8-bit Proprietary Microcontroller

CMOS

F²MC-8L MB89628R/629R/P629

MB89628R/629R/P629

■ **DESCRIPTION**

The MB89628R/629R/P629 have been developed as a general-purpose version of the F²MC*-8L family consisting of proprietary 8-bit, single-chip microcontrollers.

In addition to the F²MC-8L CPU core which can operate at low voltage but at high speed, the microcontrollers contain a variety of peripheral functions such as timers, serial interfaces, an A/D converter, and an external interrupt.

The MB89628R/629R/P629 are applicable to a wide range of applications from welfare to industrial equipment, including portable devices.

*: F²MC stands for FUJITSU Flexible Microcontroller.

■ **FEATURES**

- Large-size RAM
  MB89P629: 4 Kbytes
  MB89628R: 3 Kbytes
  MB89629R: 3 Kbytes
- High-speed processing at low voltage
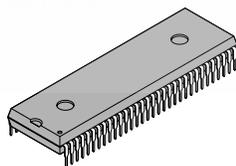 Minimum execution time: 0.4 μs/3.5 V, 0.8 μs/2.7 V
- F²MC-8L family CPU core

  Instruction set optimized for controllers
  {
  Multiplication and division instructions
  16-bit arithmetic operations
  Test and branch instructions
  Bit manipulation instructions, etc.
  }

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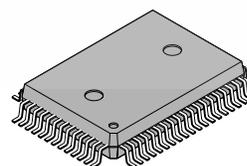
■ **PACKAGE**

64-pin Plastic SH-DIP

64-pin Plastic QFP

(DIP-64P-M01)

(FPT-64P-M06)

(Continued)

- Four types of timers
  8-bit PWM timer (also usable as a reload timer)
  8-bit pulse width count timer (Continuous measurement capable, applicable to remote control, etc.)
  16-bit timer/counter
  20-bit time-base timer
- Two serial interfaces
  Swichable the transfer direction allows communication with various equipment.
- 8-bit A/D converter
  Sense mode function enabling comparison at 5 μs
  Activation by an external input capable
- External interrupt: 4 channels
  Four channels are independent and capable of wake-up from low-power consumption modes (with an edge detection function).
- Low-power consumption modes
  Stop mode (Oscillation stops to reduce the current consumption.)
  Sleep mode (The CPU stops to reduce the current consumption to approx. 1/3 of normal.)

■ PRODUCT LINEUP

Part number / Parameter	MB89628R	MB89629R	MB89P629	MB89PV620*1
Classification	Mass production products (mask ROM products)		One-time PROM product for evaluation and development	Piggyback/evaluation product for evaluation and development
ROM size	24 K × 8 bits (internal mask ROM)	32 K × 8 bits (internal mask ROM)	32 K × 8 bits (internal PROM, programming with general-purpose EPROM programmer)	32 K × 8 bits (external ROM)
RAM size	3072 × 8 bits		4096 × 8 bits	1 K × 8 bits
CPU functions	Number of instructions: 136 Instruction bit length: 8 bits Instruction length: 1 to 3 bytes Data bit length: 1, 8, 16 bits Minimum execution time: 0.4 μs/10 MHz Interrupt processing time: 3.6 μs/10 MHz			
Ports	Input ports: 5 (4 ports also serve as peripherals.) Output ports (N-ch open-drain): 8 (All also serve as peripherals.) I/O ports (N-ch open-drain): 8 (4 ports also serve as peripherals.) Output ports (CMOS): 8 I/O ports (CMOS): 24 Total: 53			
8-bit PWM timer	8-bit reload timer operation (toggled output capable, operating clock cycle: 0.4 μs to 3.3 ms) 8-bit resolution PWM operation (conversion cycle: 102 μs to 839 ms)			
8-bit pulse width count timer	8-bit timer operation (overflow output capable, operating clock cycle: 0.4 to 12.8 μs) 8-bit reload timer operation (toggled output capable, operating clock cycle: 0.4 to 12.8 μs) 8-bit pulse width measurement operation (Continuous measurement "H" pulse width/"L" pulse width/from ↑ to ↑/from ↓ to ↓ capable)			
16-bit timer/counter	16-bit timer operation (operating clock cycle: 0.4 μs) 16-bit event counter operation (Rising/falling/both edges selectability)			
8-bit serial I/O 1, 8-bit serial I/O 2	8-bits LSB first/MSB first transfer selectability One clock selectable from four transfer clocks (one external shift clock, three internal shift clocks: 0.8 μs, 3.2 μs, 12.8 μs)			
8-bit A/D converter	8-bit resolution × 8 channels A/D conversion mode (conversion time: 18 μs) Sense mode (conversion time: 5 μs) Continuous activation by an external activation or an internal timer capable Reference voltage input			
External interrupt	4 independent channels (edge selection, interrupt vector, source flag) Rising edge/falling edge selectability Used also for wake-up from stop/sleep mode. (Edge detection is also permitted in stop mode.)			
Standby modes	Sleep mode, stop mode			
Process	CMOS			
Operating voltage*2	2.2 V to 6.0 V		2.7 V to 6.0 V	
EPROM for use				MBM27C256A-20

*1: The piggyback/evaluation product is applicable to the MB89620 series.
*2: Varies with conditions such as the operating frequency. (See section "■ Electrical Characteristics.") In the case of the MB89PV620, the voltage varies with the restrictions of the EPROM for use.

■ PACKAGE AND CORRESPONDING PRODUCTS

Package	MB89628R MB89629R MB89P629	MB89PV620
DIP-64P-M01	○	×
FPT-64P-M06	○	×
MDP-64C-P02	×	○
MQP-64C-P01	×	○

○ : Available   × : Not available

Note: For more information about each package, see section "■ Package Dimensions."

■ DIFFERENCES AMONG PRODUCTS

1. Memory Size

Before evaluating using the piggyback product, verify its differences from the product that will actually be used. Take particular care on the following points:

- On the MB89P629, the program area starts from address 8007$_H$ but on the MB89PV620, MB89628R, and MB89629R starts from 8000$_H$. (On the MB89P629, addresses 8000$_H$ to 8006$_H$ comprise the option setting area, option settings can be read by reading these addresses. On the MB89PV620, MB89628R, and MB89629R, addresses 8000$_H$ to 8006$_H$ could also be used as a program ROM. However, do not use these addresses in order to maintain compatibility of the MB89P629.)

2. Current Consumption

- In the case of the MB89PV620, add the current consumed by the EPROM which is connected to the top socket.
- When operated at low speed, the product with an OTPROM (one-time PROM) or an EPROM will consume more current than the product with a mask ROM.

  However, the current consumption in sleep/stop modes is the same. (For more information, see section "■ Electrical Characteristics".)

3. Mask Options

Functions that can be selected as options and how to designate these options vary by the product.
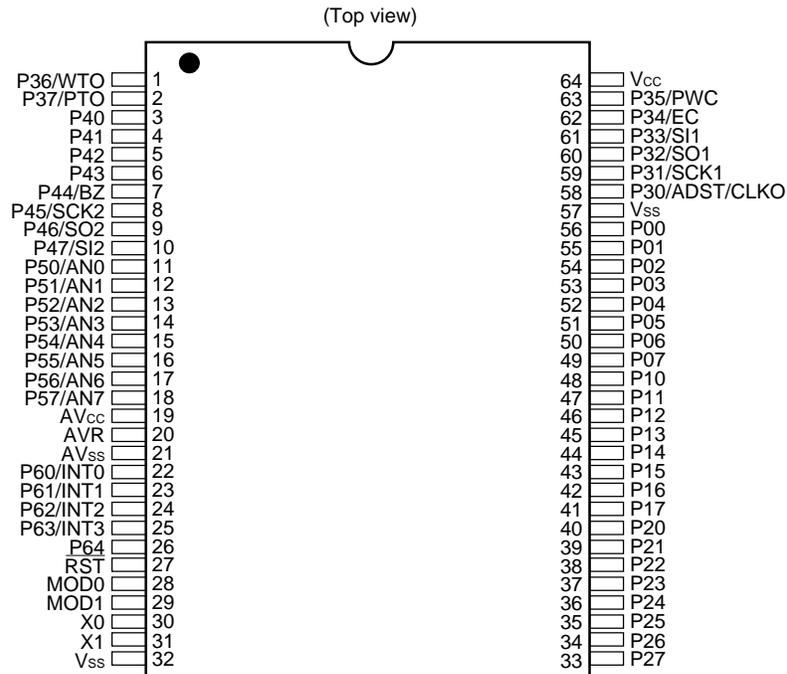
Before using options check section "■ Mask Options."
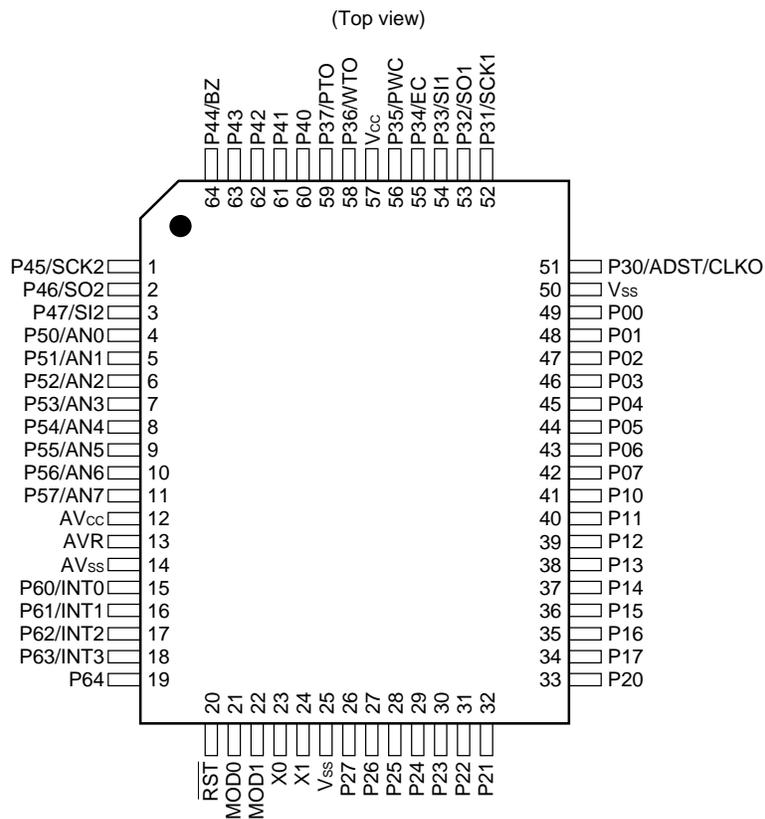
Take particular care on the following points:

- A pull-up resistor cannot be set for P40 to P47 on the MB89P629.
- A pull-up resistor is not selected for P50 to P57 when the A/D converter is used.
- Options are fixed on the MB89PV620.

■ PIN ASSIGNMENT

(Top view)

Pin	Signal		Pin	Signal
1	P36/WTO		64	Vcc
2	P37/PTO		63	P35/PWC
3	P40		62	P34/EC
4	P41		61	P33/SI1
5	P42		60	P32/SO1
6	P43		59	P31/SCK1
7	P44/BZ		58	P30/ADST/CLKO
8	P45/SCK2		57	Vss
9	P46/SO2		56	P00
10	P47/SI2		55	P01
11	P50/AN0		54	P02
12	P51/AN1		53	P03
13	P52/AN2		52	P04
14	P53/AN3		51	P05
15	P54/AN4		50	P06
16	P55/AN5		49	P07
17	P56/AN6		48	P10
18	P57/AN7		47	P11
19	AVcc		46	P12
20	AVR		45	P13
21	AVss		44	P14
22	P60/INT0		43	P15
23	P61/INT1		42	P16
24	P62/INT2		41	P17
25	P63/INT3		40	P20
26	P64		39	P21
27	RST		38	P22
28	MOD0		37	P23
29	MOD1		36	P24
30	X0		35	P25
31	X1		34	P26
32	Vss		33	P27

(DIP-64P-M01)

(Top view)

Top pins (left to right): 64 P44/BZ, 63 P43, 62 P42, 61 P41, 60 P40, 59 P37/PTO, 58 P36/WTO, 57 Vcc, 56 P35/PWC, 55 P34/EC, 54 P33/SI1, 53 P32/SO1, 52 P31/SCK1

Pin	Signal		Pin	Signal
1	P45/SCK2		51	P30/ADST/CLKO
2	P46/SO2		50	Vss
3	P47/SI2		49	P00
4	P50/AN0		48	P01
5	P51/AN1		47	P02
6	P52/AN2		46	P03
7	P53/AN3		45	P04
8	P54/AN4		44	P05
9	P55/AN5		43	P06
10	P56/AN6		42	P07
11	P57/AN7		41	P10
12	AVcc		40	P11
13	AVR		39	P12
14	AVss		38	P13
15	P60/INT0		37	P14
16	P61/INT1		36	P15
17	P62/INT2		35	P16
18	P63/INT3		34	P17
19	P64		33	P20

Bottom pins (left to right): 20 RST, 21 MOD0, 22 MOD1, 23 X0, 24 X1, 25 Vss, 26 P27, 27 P26, 28 P25, 29 P24, 30 P23, 31 P22, 32 P21

(FPT-64P-M06)

■ PIN DESCRIPTION

Pin no.		Pin name	Circuit type	Function
SH-DIP[*1]	QFP[*2]			
30	23	X0	A	Cystal oscillator pins
31	24	X1		
28	21	MOD0	B	Operating mode selection pins Connect directly to V_{CC} or V_{SS}.
29	22	MOD1		
27	20	$\overline{RST}$	C	Reset I/O pin This pin is an N-ch open-drain output type with a pull-up resistor, and a hysteresis input type. "L" is output from this pin by an internal reset source. The internal circuit is initialized by the input of "L".
56 to 49	49 to 42	P00 to P07	D	General-purpose I/O ports
48 to 41	41 to 34	P10 to P17	D	
40, 39	33, 32	P20, P21	F	General-purpose output-only ports
38, 37	31, 30	P22, P23	D	
36 to 33	29 to 26	P24 to P27	F	
58	51	P30/ADST/ CLKO	E	General-purpose I/O port Also serves as an A/D converter external activation and an oscillation monitor clock output. This port is a hysteresis input type.
59	52	P31/SCK1	E	General-purpose I/O port Also serves as the clock I/O for the 8-bit serial I/O 1. This port is a hysteresis input type.
60	53	P32/SO1	E	General-purpose I/O port Also serves as the data output for the 8-bit serial I/O 1. This port is a hysteresis input type.
61	54	P33/SI1	E	General-purpose I/O port Also serves as the data input for the 8-bit serial I/O 1. This port is a hysteresis input type.
62	55	P34/EC	E	General-purpose I/O port Also serves as the external clock input for the 16-bit timer/ counter. This port is a hysteresis input type.
63	56	P35/PWC	E	General-purpose I/O port Also serves as the measured pulse input for the 8-bit pulse width count timer. This port is a hysteresis input type.
1	58	P36/WTO	E	General-purpose I/O port Also serves as the toggle output for the 8-bit pulse width count timer. This port is a hysteresis input type.

*1: DIP-64P-M01
*2: FPT-64P-M06

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Pin no.		Pin name	Circuit type	Function
SH-DIP[*1]	QFP[*2]			
2	59	P37/PTO	E	General-purpose I/O port Also serves as the toggle output for the 8-bit PWM timer. This port is a hysteresis input type.
3 to 6	60 to 63	P40 to P43	G	N-ch open-drain I/O ports These ports are a hysteresis input type.
7	64	P44/BZ	G	N-ch open-drain I/O port Also serves as a buzzer output. This port is a hysteresis input type.
8	1	P45/SCK2	G	N-ch open-drain I/O port Also serves as the clock I/O for the 8-bit serial I/O 2. This port is a hysteresis input type.
9	2	P46/SO2	G	N-ch open-drain I/O port Also serves as the data output for the 8-bit serial I/O 2. This port is a hysteresis input type.
10	3	P47/SI2	G	N-ch open-drain I/O port Also serves as the data input for the 8-bit serial I/O 2. This port is a hysteresis input type.
11 to 18	4 to 11	P50/AN0 to P57/AN7	H	N-ch open-drain output-only port Also serves as the analog input for the A/D converter.
22 to 25	15 to 18	P60/INT0 to P63/INT2	I	General-purpose input-only ports Also serve as an external interrupt input. These ports are a hysteresis input type.
26	19	P64	I	General-purpose input-only port This port is a hysteresis input type.
64	57	V_{CC}	—	Power supply pin
32, 57	25, 50	V_{SS}	—	Power supply (GND) pins
19	12	AV_{CC}	—	A/D converter power supply pin
20	13	AVR	—	A/D converter reference voltage input pin
21	14	AV_{SS}	—	A/D converter power supply (GND) pin. Use this pin at the same voltage as V_{SS}.

*1: DIP-64P-M01
*2: FPT-64P-M06

■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A	X1, X0, Standby control signal	• At an oscillation feedback resistor of approximately 1 MΩ/5.0 V
B		
C	R, P-ch, N-ch	• At an output pull-up resistor (P-ch) of approximately 50 MΩ/5.0 V • CMOS hysteresis input
D	R, P-ch, P-ch, N-ch	• CMOS output • CMOS input • Pull-up resistor optional (except P22 and P23)
E	R, P-ch, P-ch, N-ch	• CMOS output • Hysteresis input • Pull-up resistor optional
F	P-ch, N-ch	• CMOS output

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Type	Circuit	Remarks
G		• N-ch open-drain output • Hysteresis input • Pull-up resistor optional (MB89628R and MB89629R only)
H		• N-ch open-drain output • Analog input
I		• Hysteresis input • Pull-up resistor optional

■ HANDLING DEVICES

1. Preventing Latchup

Latchup may occur on CMOS ICs if voltage higher than V_{CC} or lower than V_{SS} is applied to input and output pins other than medium- to high-voltage pins or if higher than the voltage which shows on "1. Absolute Maximum Ratings" in section "■ Electrical Characteristics" is applied between V_{CC} and V_{SS}.

When latchup occurs, power supply current increases rapidly and might thermally damage elements. When using, take great care not to exceed the absolute maximum ratings.

Also, take care to prevent the analog power supply (AV_{CC} and AVR) and analog input from exceeding the digital power supply (V_{CC}) when the analog system power supply is turned on and off.

2. Treatment of Unused Input Pins

Leaving unused input pins open could cause malfunctions. They should be connected to a pull-up or pull-down resistor.

3. Treatment of Power Supply Pins on Microcontrollers with A/D and D/A Converters

Connect to be AV_{CC} = DAVC = V_{CC} and AV_{SS} = AVR = V_{SS} even if the A/D and D/A converters are not in use.

4. Treatment of N.C. Pins

Be sure to leave (internally connected) N.C. pins open.

5. Power Supply Voltage Fluctuations

Although V_{CC} power supply voltage is assured to operate within the rated range, a rapid fluctuation of the voltage could cause malfunctions, even if it occurs within the rated range. Stabilizing voltage supplied to the IC is therefore important. As stabilization guidelines, it is recommended to control power so that V_{CC} ripple fluctuations (P-P value) will be less than 10% of the standard V_{CC} value at the commercial frequency (50 to 60 Hz) and the transient fluctuation rate will be less than 0.1 V/ms at the time of a momentary fluctuation such as when power is switched.

6. Precautions when Using an External Clock

Even when an external clock is used, oscillation stabilization time is required for power-on reset (optional) and wake-up from stop mode.

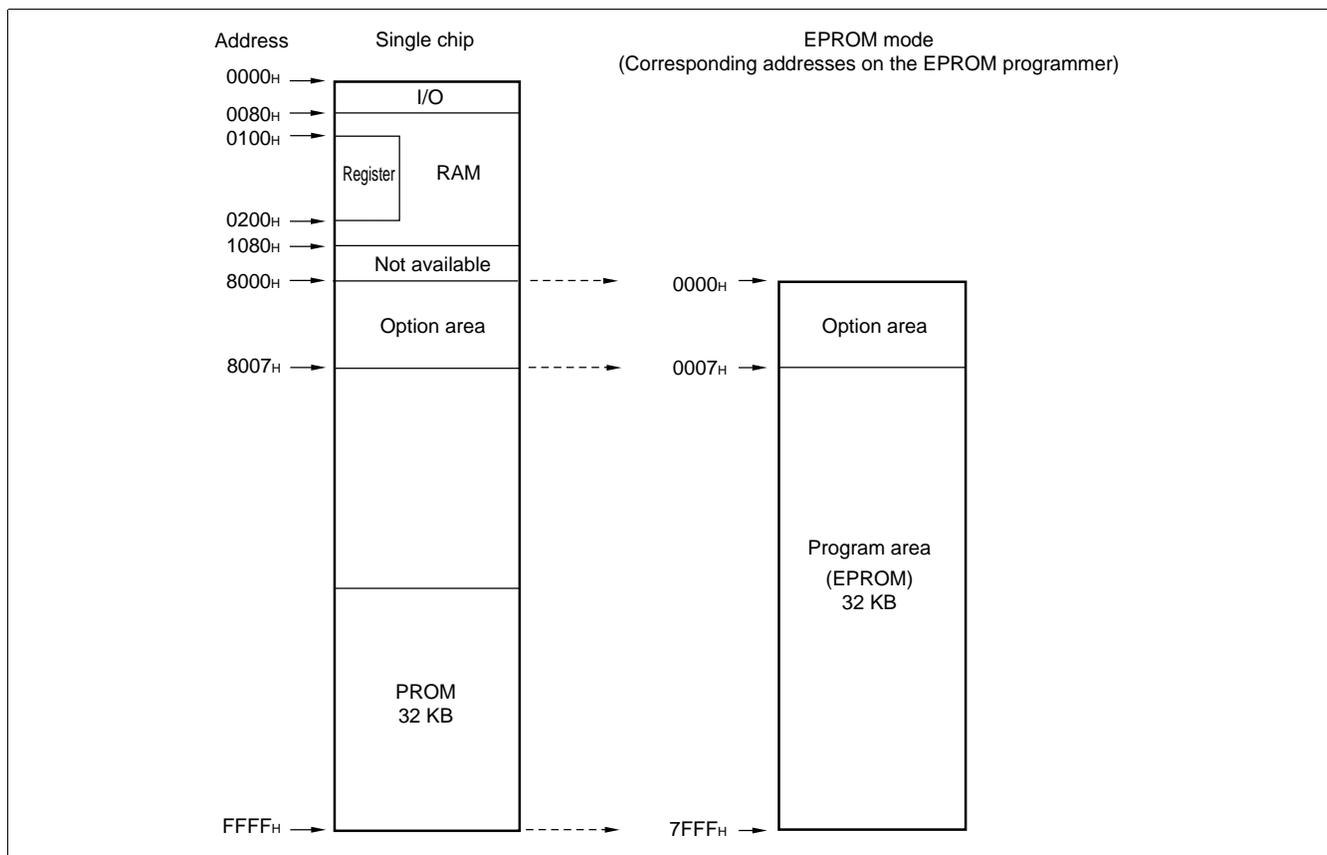## ■ PROGRAMMING TO THE EPROM ON THE MB89P629

The MB89P629 is an OTPROM version of the MB89628R and MB89629R.

1. Features

- 16-Kbyte PROM on chip
- Options can be set using the EPROM programmer.
- Equivalency to the MBM27C256A in EPROM mode (when programmed with the EPROM programmer)

2. Memory Space

Memory space in EPROM mode, option area is diagrammed below.

3. Programming to the EPROM

In EPROM mode, the MB89P629 functions equivalent to the MBM27C256A. This allows the PROM to be programmed with a general-purpose EPROM programmer (the electronic signature mode cannot be used) by using the dedicated socket adapter.
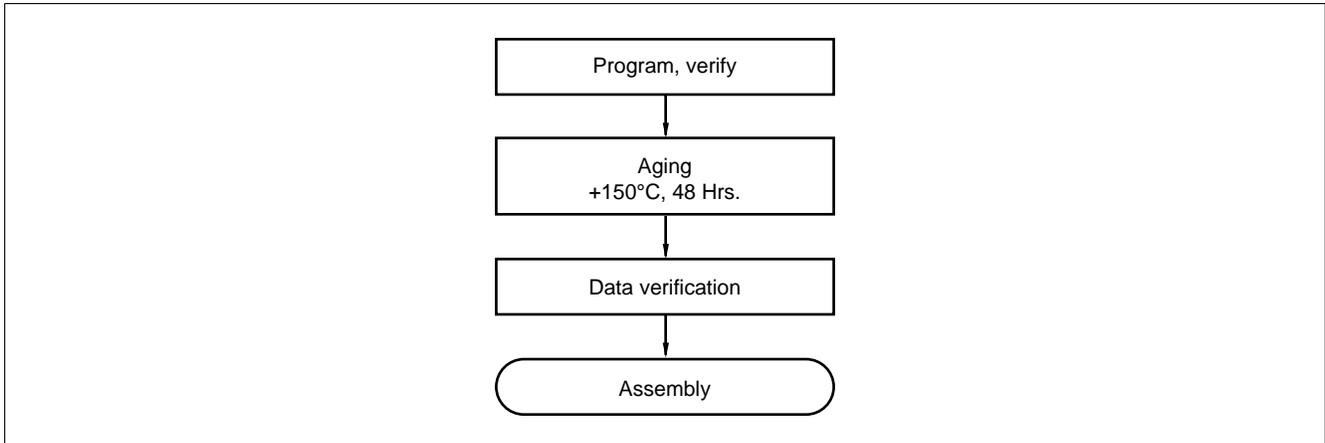
- **Programming procedure**

(1) Set the EPROM programmer to the MBM27C256A.

(2) Load program data into the EPROM programmer at 0000_H to $7FFF_H$ (note that addresses 8000_H to $FFFF_H$ while operating as a single chip assign to 0000_H to $7FFF_H$ in EPROM mode. For information about each corresponding option, see "7. Setting OTPROM Options.")

(3) Program to 0000_H to $7FFF_H$ with the EPROM programmer.

4. Recommended Screening Conditions

High-temperature aging is recommended as the pre-assembly screening procedure for a product with a blanked OTPROM microcomputer program.

```
┌─────────────────────────┐
│      Program, verify     │
└─────────────────────────┘
              │
              ▼
┌─────────────────────────┐
│          Aging           │
│     +150°C, 48 Hrs.      │
└─────────────────────────┘
              │
              ▼
┌─────────────────────────┐
│     Data verification    │
└─────────────────────────┘
              │
              ▼
      (     Assembly     )
```

5. Programming Yield

All bits cannot be programmed at Fujitsu shipping test to a blanked OTPROM microcomputer, due to its nature. For this reason, a programming yield of 100% cannot be assured at all times.

6. EPROM Programmer Socket Adapter

Package	Compatible socket adapter
DIP-64P-M01	ROM-64SD-28DP-8L
FPT-64P-M06	ROM-64QF-28DP-8L

Inquiry: Sun Hayato Co., Ltd.: TEL 81-3-3802-5760

7. Setting OTPROM Options

The programming procedure is the same as that for the PROM. Options can be set by programming values at the addresses shown on the memory map. The relationship between bits and options is shown on the following bit map:

• **OTPROM option bit map**

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
8000$_H$ (0000$_H$)	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Oscillation stabilization time 1: Crystal 0: Ceramic	Reset pin output 1: Yes 2: No	Power-on reset 1: Yes 0: No	Vacancy Readable and writable	Vacancy Readable and writable
8001$_H$ (0001$_H$)	P07 Pull-up 1: No 0: Yes	P06 Pull-up 1: No 0: Yes	P05 Pull-up 1: No 0: Yes	P04 Pull-up 1: No 0: Yes	P03 Pull-up 1: No 0: Yes	P02 Pull-up 1: No 0: Yes	P01 Pull-up 1: No 0: Yes	P00 Pull-up 1: No 0: Yes
8002$_H$ (0002$_H$)	P17 Pull-up 1: No 0: Yes	P16 Pull-up 1: No 0: Yes	P15 Pull-up 1: No 0: Yes	P14 Pull-up 1: No 0: Yes	P13 Pull-up 1: No 0: Yes	P12 Pull-up 1: No 0: Yes	P11 Pull-up 1: No 0: Yes	P10 Pull-up 1: No 0: Yes
8003$_H$ (0003$_H$)	P37 Pull-up 1: No 0: Yes	P36 Pull-up 1: No 0: Yes	P35 Pull-up 1: No 0: Yes	P34 Pull-up 1: No 0: Yes	P33 Pull-up 1: No 0: Yes	P32 Pull-up 1: No 0: Yes	P31 Pull-up 1: No 0: Yes	P30 Pull-up 1: No 0: Yes
8004$_H$ (0004$_H$)	P57 Pull-up 1: No 0: Yes	P56 Pull-up 1: No 0: Yes	P55 Pull-up 1: No 0: Yes	P54 Pull-up 1: No 0: Yes	P53 Pull-up 1: No 0: Yes	P52 Pull-up 1: No 0: Yes	P51 Pull-up 1: No 0: Yes	P50 Pull-up 1: No 0: Yes
8005$_H$ (0005$_H$)	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	P64 Pull-up 1: No 0: Yes	P63 Pull-up 1: No 0: Yes	P62 Pull-up 1: No 0: Yes	P61 Pull-up 1: No 0: Yes	P60 Pull-up 1: No 0: Yes
8006$_H$ (0006$_H$)	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Reserved bit Readable and writable

Notes: • Set each bit to 1 to erase.
• Do not write 0 to the vacant bit.
   The read value of the vacant bit is 1, unless 0 is written to it.
• Always write 0 to the reserved bit.

■ PROGRAMMING TO THE EPROM WITH PIGGYBACK/EVALUATION DEVICE

1. EPROM for Use

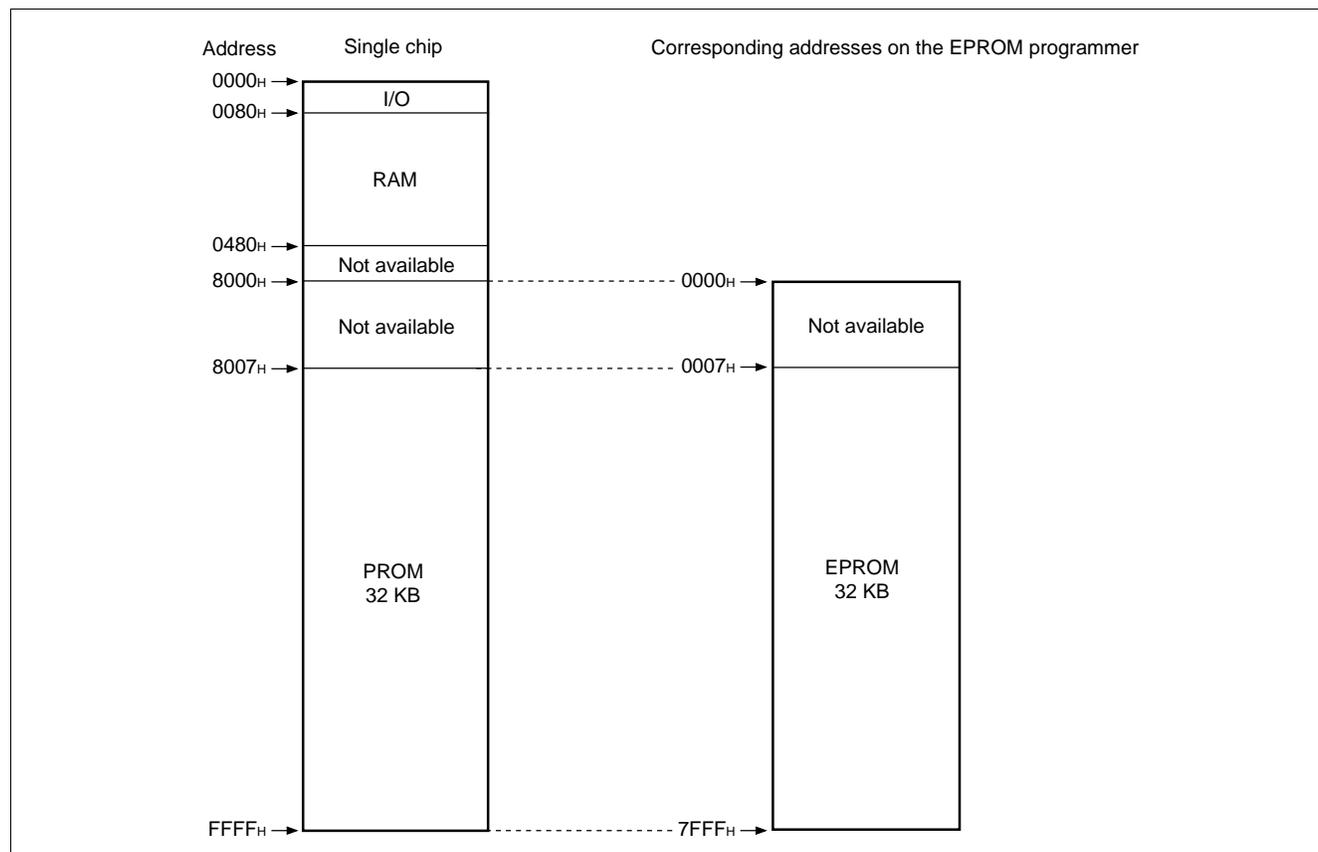MBM27C256A-20TV, MBM27C256A-20CZ

2. Programming Socket Adapter

To program to the PROM using an EPROM programmer, use the socket adapter (manufacturer: Sun Hayato Co., Ltd.) listed below.

Package	Adapter socket part number
LCC-32 (Rectangle)	ROM-32LC-28DP-YG

Inquiry: Sun Hayato Co., Ltd.: TEL 81-3-3802-5760

3. Memory Space

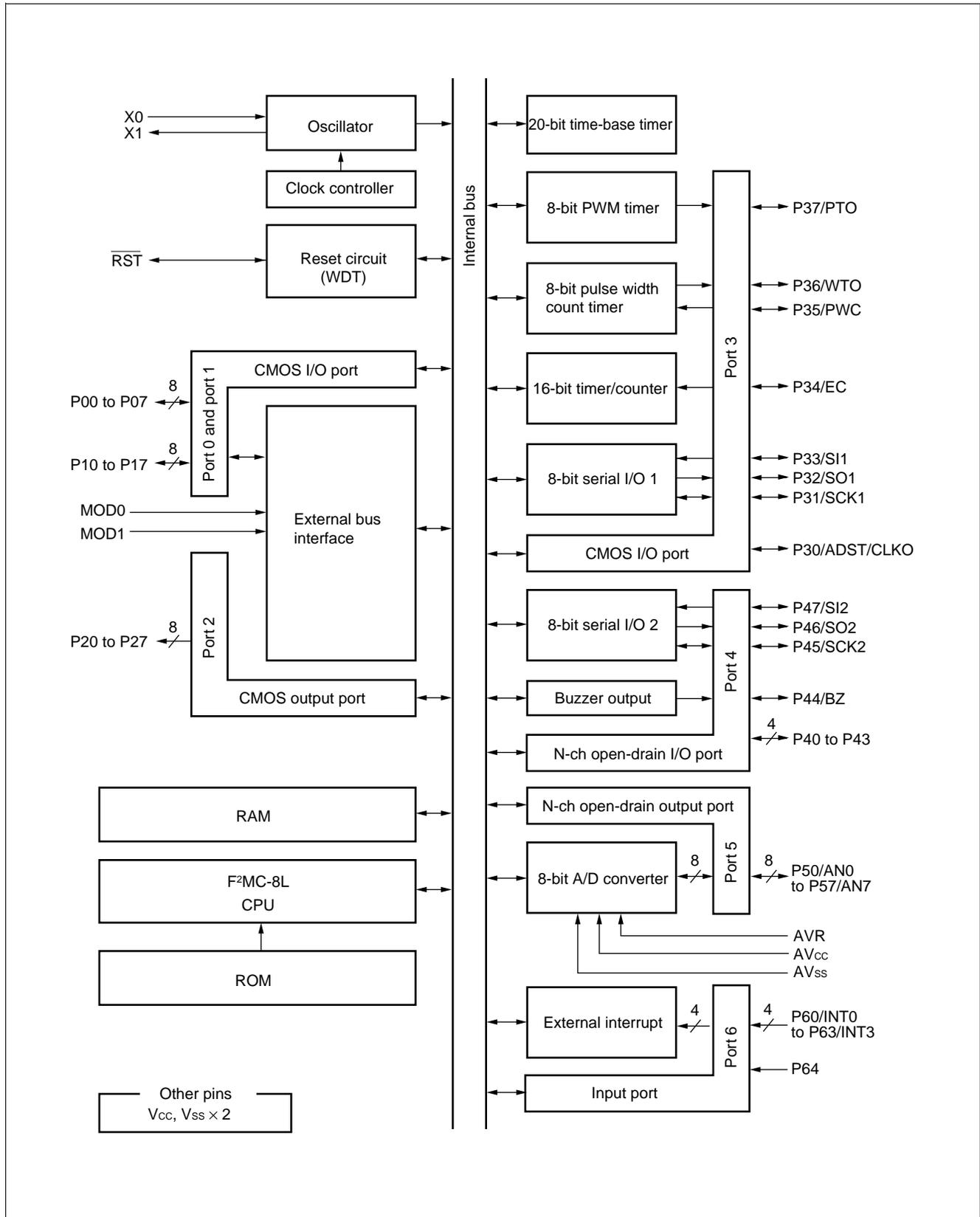Memory space in 32-Kbyte PROM on the EPROM programmer is diagrammed below.

4. Programming to the EPROM

(1)   Set the EPROM programmer to the MBM27C256A.

(2)   Load program data into the EPROM programmer at 0007_H to $7FFF_H$.

(3)   Program to 0000_H to $7FFF_H$ with the EPROM programmer.

■ BLOCK DIAGRAM

■ CPU CORE

1. Memory Space

The microcontrollers of the MB89628R/629R/P629 offer a memory space of 64 Kbytes for storing all of I/O, data, and program areas. The I/O area is located at the lowest address. The data area is provided immediately above the I/O area. The data area can be divided into register, stack, and direct areas according to the application. The program area is located at exactly the opposite end, that is, near the highest address. Provide the tables of interrupt reset vectors and vector call instructions toward the highest address within the program area. The memory space of the MB89628R/629R/P629 is structured as illustrated below.

Memory Space
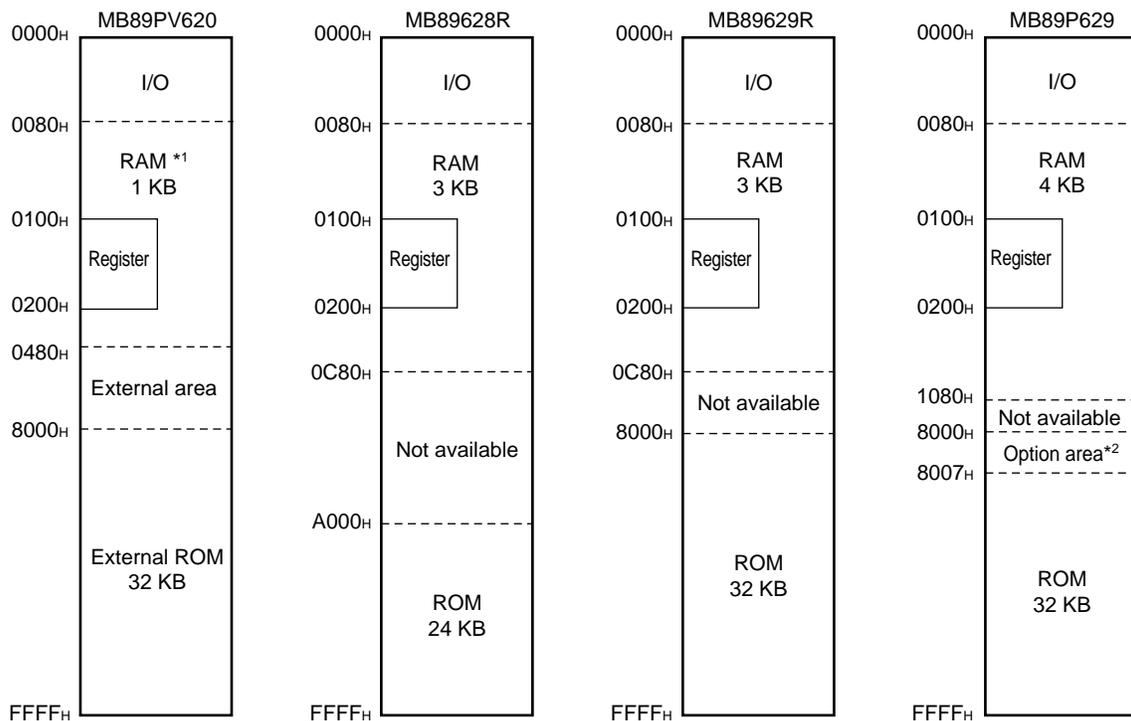
*1: The internal RAM of the MB89PV620 is 1 Kbyte. The RAM of a development tool can be substituted for that RAM when the tool is connected. If the MB89PV620 is used as a piggyback product, however, it runs out of RAM. Note, in addition, that some tools such as the MB2140 series cannot be used due to mapping restrictions.
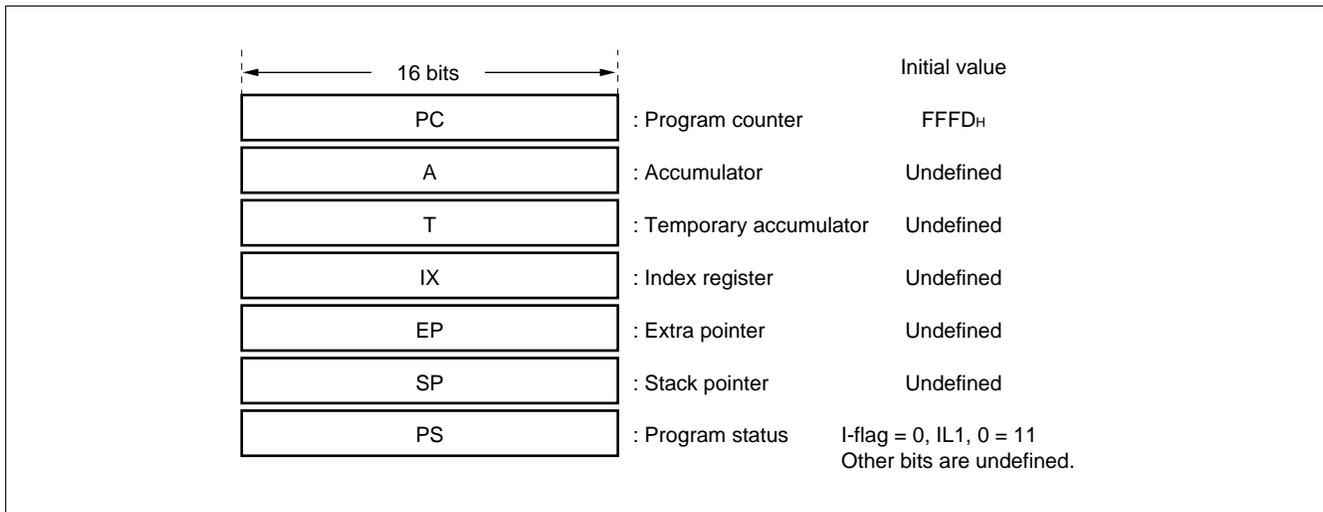
*2: Since addresses 8000_H to 8006_H for the MB89P629 comprise an option area, do not use this area for the MB89PV620, MB89628R, and MB89629R.
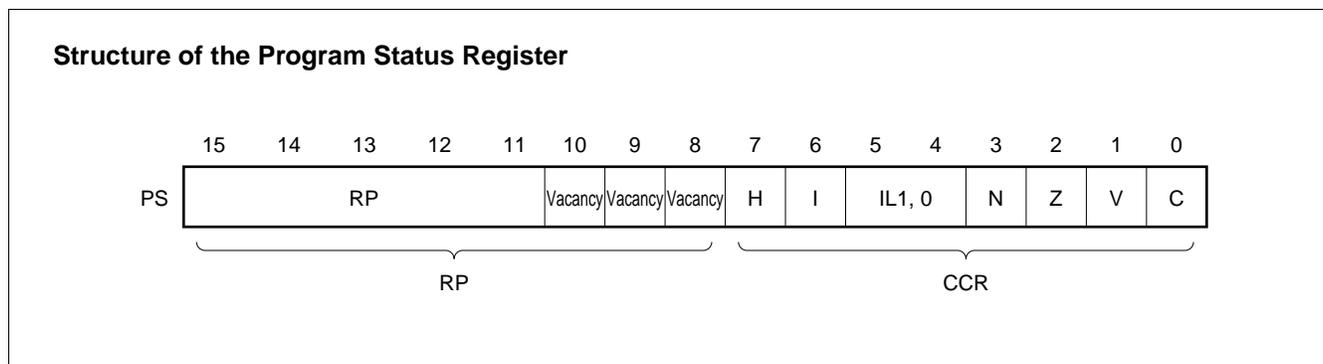
3. Registers

The F^{2}MC-8L family has two types of registers; dedicated registers in the CPU and general-purpose registers in the memory. The following dedicated registers are provided:

Program counter (PC):   A 16-bit register for indicating instruction storage positions

Accumulator (A):   A 16-bit temporary register for storing arithmetic operations, etc. When the instruction is an 8-bit data processing instruction, the lower byte is used.

Temporary accumulator (T):   A 16-bit register which performs arithmetic operations with the accumulator When the instruction is an 8-bit data processing instruction, the lower byte is used.

Index register (IX):   A 16-bit register for index modification

Extra pointer (EP):   A 16-bit pointer for indicating a memory address

Stack pointer (SP):   A 16-bit register for indicating a stack area

Program status (PS):   A 16-bit register for storing a register pointer, a condition code

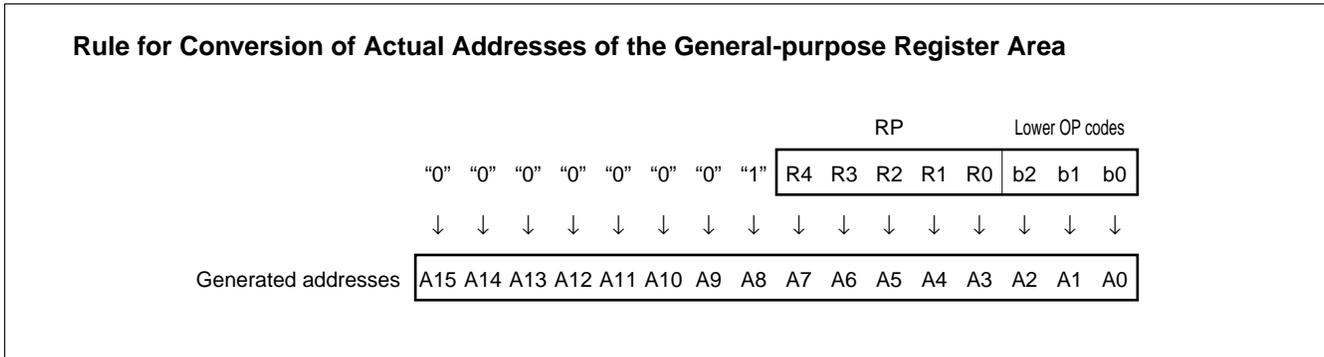|	16 bits		Initial value
PC	: Program counter	FFFD$_H$
A	: Accumulator	Undefined
T	: Temporary accumulator	Undefined
IX	: Index register	Undefined
EP	: Extra pointer	Undefined
SP	: Stack pointer	Undefined
PS	: Program status	I-flag = 0, IL1, 0 = 11 Other bits are undefined.

The PS can further be divided into higher 8 bits for use as a register bank pointer (RP) and the lower 8 bits for use as a condition code register (CCR). (See the diagram below.)

Structure of the Program Status Register

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PS			RP			Vacancy	Vacancy	Vacancy	H	I	IL1, 0		N	Z	V	C

RP   CCR

The RP indicates the address of the register bank currently in use. The relationship between the pointer contents and the actual address is based on the conversion rule illustrated below.

Rule for Conversion of Actual Addresses of the General-purpose Register Area

$$\begin{array}{ccccccccc} & & & & & & & & \text{RP} & & & & \text{Lower OP codes} \end{array}$$

| "0" | "0" | "0" | "0" | "0" | "0" | "0" | "1" | R4 | R3 | R2 | R1 | R0 | b2 | b1 | b0 |

↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓

Generated addresses

| A15 | A14 | A13 | A12 | A11 | A10 | A9 | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |

The CCR consists of bits indicating the results of arithmetic operations and the contents of transfer data and bits for control of CPU operations at the time of an interrupt.

H-flag: Set when a carry or a borrow from bit 3 to bit 4 occurs as a result of an arithmetic operation. Cleared otherwise. This flag is for decimal adjustment instructions.

I-flag: Interrupt is allowed when this flag is set to 1. Interrupt is prohibited when the flag is set to 0. Set to 0 when reset.

IL1, 0: Indicates the level of the interrupt currently allowed. Processes an interrupt only if its request level is higher than the value indicated by this bit.

IL1	IL0	Interrupt level	High-low
0	0	1	High
0	1		
1	0	2	
1	1	3	Low = no interrupt

N-flag: Set if the MSB is set to 1 as the result of an arithmetic operation. Cleared when the bit is set to 0.

Z-flag: Set when an arithmetic operation results in 0. Cleared otherwise.

V-flag: Set if the complement on 2 overflows as a result of an arithmetic operation. Reset if the overflow does not occur.

C-flag: Set when a carry or a borrow from bit 7 occurs as a result of an arithmetic operation. Cleared otherwise. Set to the shift-out value in the case of a shift instruction.

The following general-purpose registers are provided:

General-purpose registers: An 8-bit register for storing data

The general-purpose registers are 8 bits and located in the register banks of the memory. One bank contains eight registers and up to a total of 32 banks can be used on the MB89628R and MB89629R. The bank currently in use is indicated by the register bank pointer (RP).

Register Bank Configuration

This address = $0100_H + 8 \times (RP)$

R 0
R 1
R 2
R 3
R 4
R 5
R 6
R 7

32 banks

Memory area
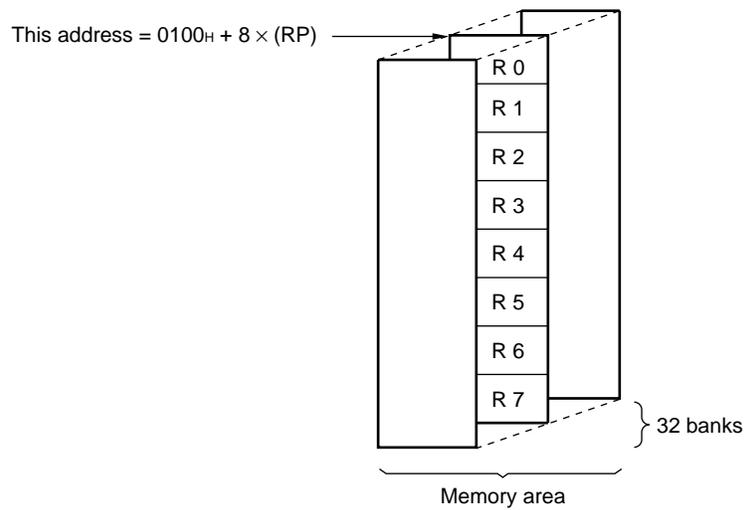
■ I/O MAP

Address	Read/write	Register name	Register description
00$_H$	(R/W)	PDR0	Port 0 data register
01$_H$	(W)	DDR0	Port 0 data direction register
02$_H$	(R/W)	PDR1	Port 1 data register
03$_H$	(W)	DDR1	Port 1 data direction register
04$_H$	(R/W)	PDR2	Port 2 data register
05$_H$	(R/W)	BCTR	External bus pin control register
06$_H$			Vacancy
07$_H$			Vacancy
08$_H$	(R/W)	STBC	Standby control register
09$_H$	(R/W)	WDTC	Watchdog timer control register
0A$_H$	(R/W)	TBTC	Time-base timer control register
0B$_H$			Vacancy
0C$_H$	(R/W)	PDR3	Port 3 data register
0D$_H$	(W)	DDR3	Port 3 data direction register
0E$_H$	(R/W)	PDR4	Port 4 data register
0F$_H$	(R/W)	BZCR	Buzzer register
10$_H$	(R/W)	PDR5	Port 5 data register
11$_H$	(R)	PDR6	Port 6 data register
12$_H$	(R/W)	CNTR	PWM control register
13$_H$	(W)	COMR	PWM compare register
14$_H$	(R/W)	PCR1	PWC pulse width control register 1
15$_H$	(R/W)	PCR2	PWC pulse width control register 2
16$_H$	(R/W)	RLBR	PWC reload buffer register
17$_H$			Vacancy
18$_H$	(R/W)	TMCR	16-bit timer control register
19$_H$	(R/W)	TCHR	16-bit timer count register (H)
1A$_H$	(R/W)	TCLR	16-bit timer count register (L)
1B$_H$			Vacancy
1C$_H$	(R/W)	SMR1	Serial I/O 1 mode register
1D$_H$	(R/W)	SDR1	Serial I/O 1 data register
1E$_H$	(R/W)	SMR2	Serial I/O 2 mode register
1F$_H$	(R/W)	SDR2	Serial I/O 2 data register

(Continued)

(Continued)

Address	Read/write	Register name	Register description
20$_H$	(R/W)	ADC1	A/D converter control register 1
21$_H$	(R/W)	ADC2	A/D converter control register 2
22$_H$	(R/W)	ADCD	A/D converter data register
23$_H$			Vacancy
24$_H$	(R/W)	EIC1	External interrupt control register 1
25$_H$	(R/W)	EIC2	External interrupt control register 2
26$_H$	(R/W)	CLKE	Clock output control register
27$_H$ to 7B$_H$			Vacancy
7C$_H$	(W)	ILR1	Interrupt level setting register 1
7D$_H$	(W)	ILR2	Interrupt level setting register 2
7E$_H$	(W)	ILR3	Interrupt level setting register 3
7F$_H$			Vacancy

Note: Do not use vacancies.

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

$(AV_{SS} = V_{SS} = 0.0 \text{ V})$

Parameter	Symbol	Value Min.	Value Max.	Unit	Remarks
Power supply voltage	V_{CC} AV_{CC}	$V_{SS} - 0.3$	$V_{SS} + 7.0$	V	*1
A/D converter reference input voltage	AVR	$V_{SS} - 0.3$	$V_{SS} + 7.0$	V	AVR must not exceed AV_{CC} + 0.3 V.
Input voltage	V_I	$V_{SS} - 0.3$	$V_{CC} + 0.3$	V	Except P40 to P47*2
	V_{I2}	$V_{SS} - 0.3$	$V_{SS} + 7.0$	V	P40 to P47
Output voltage	V_O	$V_{SS} - 0.3$	$V_{CC} + 0.3$	V	Except P40 to P47*2
	V_{O2}	$V_{SS} - 0.3$	$V_{SS} + 7.0$	V	P40 to P47
"L" level maximum output current	I_{OL}	—	20	mA	
"L" level average output current	I_{OLAV}	—	4	mA	Average value (operating current × operating rate)
"L" level total maximum output current	ΣI_{OL}	—	100	mA	
"L" level total average output current	ΣI_{OLAV}	—	40	mA	Average value (operating current × operating rate)
"H" level maximum output current	I_{OH}	—	−20	mA	
"H" level average output current	I_{OHAV}	—	−4	mA	Average value (operating current × operating rate)
"H" level total maximum output current	ΣI_{OH}	—	−50	mA	
"H" level total average output current	ΣI_{OHAV}	—	−20	mA	Average value (operating current × operating rate)
Power consumption	P_D	—	300	mW	
Operating temperature	T_A	−40	+85	°C	
Storage temperature	Tstg	−55	+150	°C	

*1: Use AV_{CC} and V_{CC} set at the same voltage.
Take care so that AV_{CC} does not exceed V_{CC}, such as when power is turned on.

*2: V_I and V_O must not exceed V_{CC} + 0.3 V.

Precautions: Permanent device damage may occur if the above "Absolute Maximum Ratings" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2. Recommended Operating Conditions

$(AV_{SS} = V_{SS} = 0.0\ V)$

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
Power supply voltage	V_{CC} AV_{CC}	2.2*	6.0*	V	Normal operation assurance range* (MB89628R/629R)
		2.7*	6.0*	V	Normal operation assurance range* (MB89P629/PV620)
		1.5	6.0	V	Retains the RAM state in stop mode
A/D converter reference input voltage	AVR	0.0	AV_{CC}	V	
Operating temperature	T_A	−40	+85	°C	

* : These values vary with the operating frequency and analog assurance range. See Figure 1 and "5. A/D Converter Electrical Characteristics."
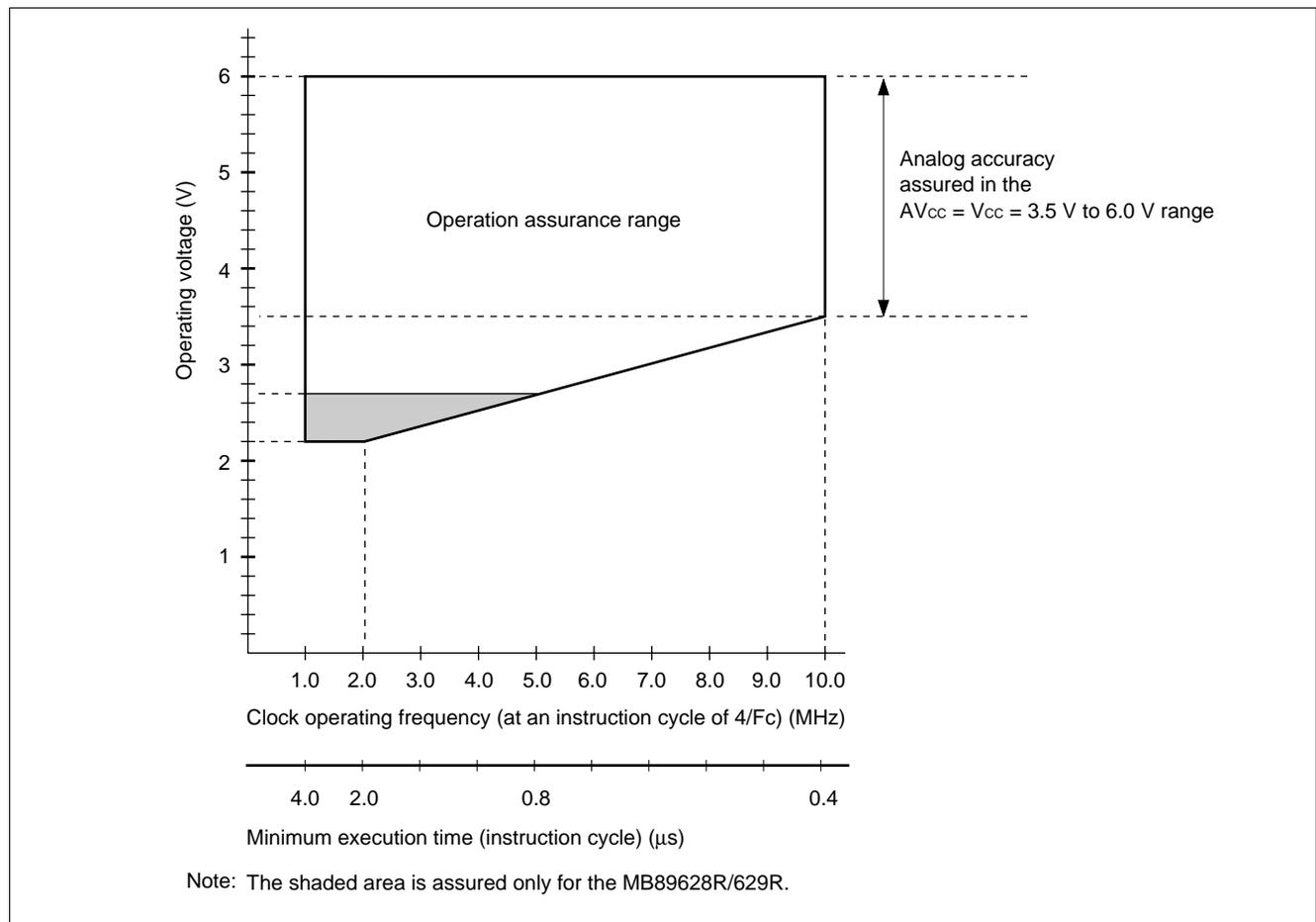
Figure 1   Operating Voltage vs. Clock Operating Frequency

Figure 1 indicates the operating frequency of the external oscillator at an instruction cycle of 4/Fc.

3. DC Characteristics

(AV$_{CC}$ = V$_{CC}$ = +5.0 V, AV$_{SS}$ = V$_{SS}$ = 0.0 V, T$_A$ = −40°C to +85°C)

Parameter	Symbol	Pin	Condition	Value Min.	Value Typ.	Value Max.	Unit	Remarks
"H" level input voltage	V$_{IH}$	P00 to P07, P10 to P17, P22, P23	—	0.7 V$_{CC}$	—	V$_{CC}$ + 0.3	V	
	V$_{IHS}$	$\overline{RST}$, MOD0, MOD1, P30 to P37, P60 to P64	—	0.8 V$_{CC}$	—	V$_{CC}$ + 0.3	V	
	V$_{IHS2}$	P40 to P47	—	0.8 V$_{CC}$	—	V$_{SS}$ + 6.0	V	
"L" level input voltage	V$_{IL}$	P00 to P07, P10 to P17, P22, P23	—	V$_{SS}$ − 0.3	—	0.3 V$_{CC}$	V	
	V$_{ILS}$	$\overline{RST}$, MOD0, MOD1, P30 to P37, P40 to P47, P60 to P64	—	V$_{SS}$ − 0.3	—	0.2 V$_{CC}$	V	
Open-drain output pin application voltage	V$_D$	P50 to P57	—	V$_{SS}$ − 0.3	—	V$_{SS}$ + 0.3	V	
	V$_{D2}$	P40 to P47	—	V$_{SS}$ − 0.3	—	V$_{SS}$ + 6.0	V	
"H" level output voltage	V$_{OH}$	P00 to P07, P10 to P17, P20 to P27, P30 to P37	I$_{OH}$ = −2.0 mA	4.0	—	—	V	
"L" level output voltage	V$_{OL}$	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57	I$_{OL}$ = +4.0 mA	—	—	0.4	V	
	V$_{OL2}$	$\overline{RST}$		—	—	0.4	V	
Input leakage current (Hi-z output leakage current)	I$_{LI1}$	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P60 to P64, MOD0, MOD1	0.0 V < V$_I$ < V$_{CC}$	—	—	±5	μA	Without pull-up resistor
Pull-up resistance	R$_{PULL}$	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P64, $\overline{RST}$	V$_I$ = 0.0 V	25	50	100	kΩ	

(Continued)

(Continued)

(AV$_{CC}$ = V$_{CC}$ = +5.0 V, AV$_{SS}$ = V$_{SS}$ = 0.0 V, T$_A$ = −40°C to +85°C)

| Parameter | Symbol | Pin | Condition | Value | | | Unit | Remarks |
				Min.	Typ.	Max.		
Power supply current*	I$_{CC}$	V$_{CC}$	F$_C$ = 10 MHz Normal operation mode (External clock)	—	9	15	mA	MB89628R, MB89629R
				—	10	18	mA	MB89P629
	I$_{CCS}$		F$_C$ = 10 MHz Sleep mode (External clock)	—	3	4	mA	
	I$_{CCH}$		Stop mode T$_A$ = +25°C	—	—	1	μA	
	I$_A$	AV$_{CC}$	F$_C$ = 10 MHz, when A/D conversion is activated	—	1	3	mA	
	I$_{AH}$		F$_C$ = 10 MHz, T$_A$ = +25°C, when A/D conversion is stopped	—	—	1	μA	
Input capacitance	C$_{IN}$	Other than AV$_{CC}$, AV$_{SS}$, V$_{CC}$, and V$_{SS}$	f = 1 MHz	—	10	—	pF	

* : In the case of the MB89PV620, the current consumed by the connected EPROM and ICE is not included.
The power supply current is measured at the external clock.

4. AC Characteristics
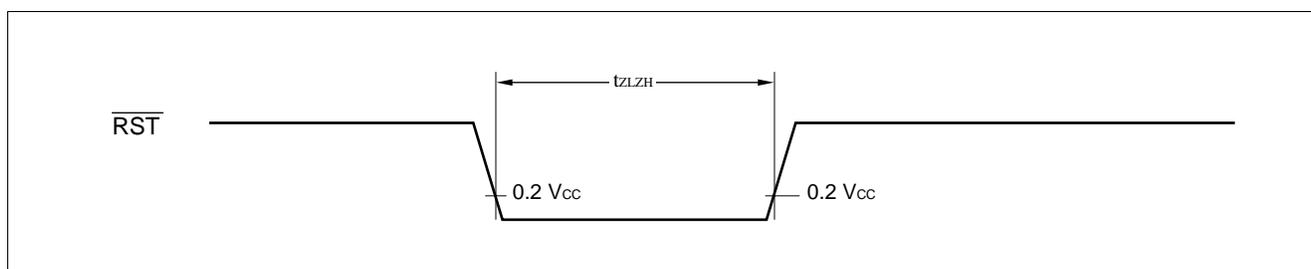
(1) Reset Timing

$(V_{CC} = +5.0\ V \pm 10\%, AV_{SS} = V_{SS} = 0.0\ V, T_A = -40°C\ to\ +85°C)$

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min.	Max.		
$\overline{RST}$ "L" pulse width	t_{ZLZH}	—	$16\ t_{XCYL}$	—	ns	

Note: t_{XCYL} is the oscillation cycle $(1/F_C)$ to input to the X0 pin.

(2) Power-on Reset

$(AV_{SS} = V_{SS} = 0.0\ V, T_A = -40°C\ to\ +85°C)$

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min.	Max.		
Power supply rising time	t_R	—	—	50	ms	Power-on reset function only
Power supply cut-off time	t_{OFF}		1	—	ms	Due to repeated operations

Note: Make sure that power supply rises within the selected oscillation stabilization time.
If power supply voltage needs to be varied in the course of operation, a smooth voltage rise is recommended.
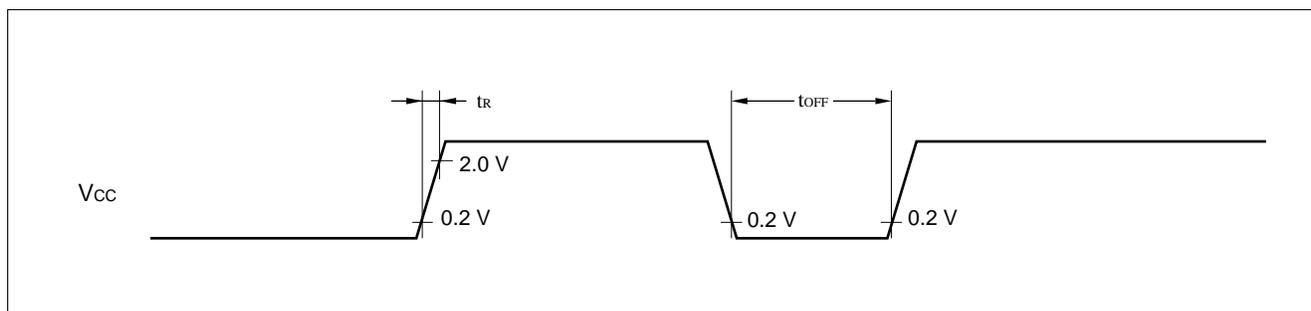
(3) Clock Timing

(AV$_{SS}$ = V$_{SS}$ = 0.0 V, T$_A$ = −40°C to +85°C)

Parameter	Symbol	Pin	Condition	Value Min.	Value Max.	Unit	Remarks
Clock frequency	F$_C$	X0, X1		1	10	MHz	
Clock cycle time	t$_{XCYL}$	X0, X1		100	1000	ns	
Input clock pulse width	P$_{WH}$ P$_{WL}$	X0	—	20	—	ns	External clock
Input clock rising/falling time	t$_{CR}$ t$_{CF}$	X0		—	10	ns	External clock

X0 and X1 Timing and Conditions
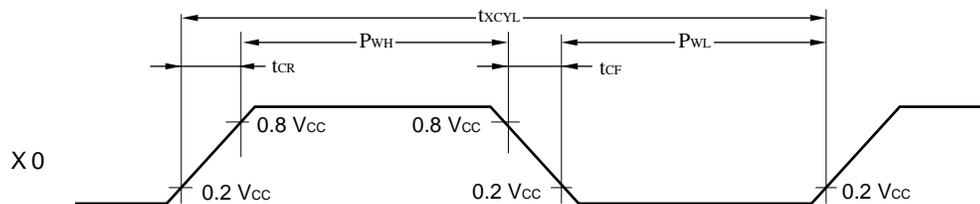
Clock Conditions
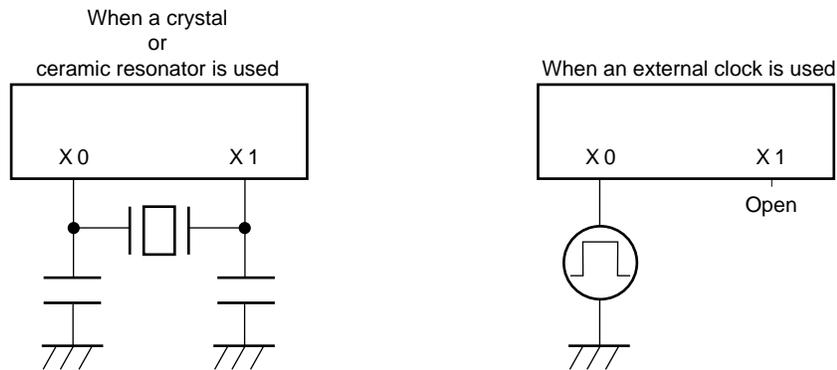
(4) Instruction Cycle

Parameter	Symbol	Value (typical)	Unit	Remarks
Instruction cycle (minimum execution time)	t$_{inst}$	4/F$_C$	μs	t$_{inst}$ = 0.4 μs when operating at F$_C$ = 10 MHz

(5) Serial I/O Timing

$(V_{CC} = +5.0\ V\pm10\%,\ AV_{SS} = V_{SS} = 0.0\ V,\ T_A = -40°C\ to\ +85°C)$

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min.	Max.		
Serial clock cycle time	t_{SCYC}	SCK1, SCK2	Internal shift clock mode	2 t_{inst}*	—	μs	
SCK1 ↓ → SO1 time SCK2 ↓ → SO2 time	t_{SLOV}	SCK1, SO1 SCK2, SO2		−200	200	ns	
Valid SI1 → SCK1 ↑ Valid SI2 → SCK2 ↑	t_{IVSH}	SI1, SCK1 SI2, SCK2		1/2 t_{inst}*	—	μs	
SCK1 ↑ → valid SI1 hold time SCK2 ↑ → valid SI2 hold time	t_{SHIX}	SCK1, SI1 SCK2, SI2		1/2 t_{inst}*	—	μs	
Serial clock "H" pulse width	t_{SHSL}	SCK1, SCK2	External shift clock mode	1 t_{inst}*	—	μs	
Serial clock "L" pulse width	t_{SLSH}	SCK1, SCK2		1 t_{inst}*	—	μs	
SCK1 ↓ → SO1 time SCK2 ↓ → SO2 time	t_{SLOV}	SCK1, SO1 SCK2, SO2		0	200	ns	
Valid SI1 → SCK1 ↑ Valid SI2 → SCK2 ↑	t_{IVSH}	SI1, SCK1 SI2, SCK2		1/2 t_{inst}*	—	μs	
SCK1 ↑ → valid SI1 hold time SCK2 ↑ → valid SI2 hold time	t_{SHIX}	SCK1, SI1 SCK2, SI2		1/2 t_{inst}*	—	μs	

* : For information on t_{inst}, see "(4) Instruction Cycle."
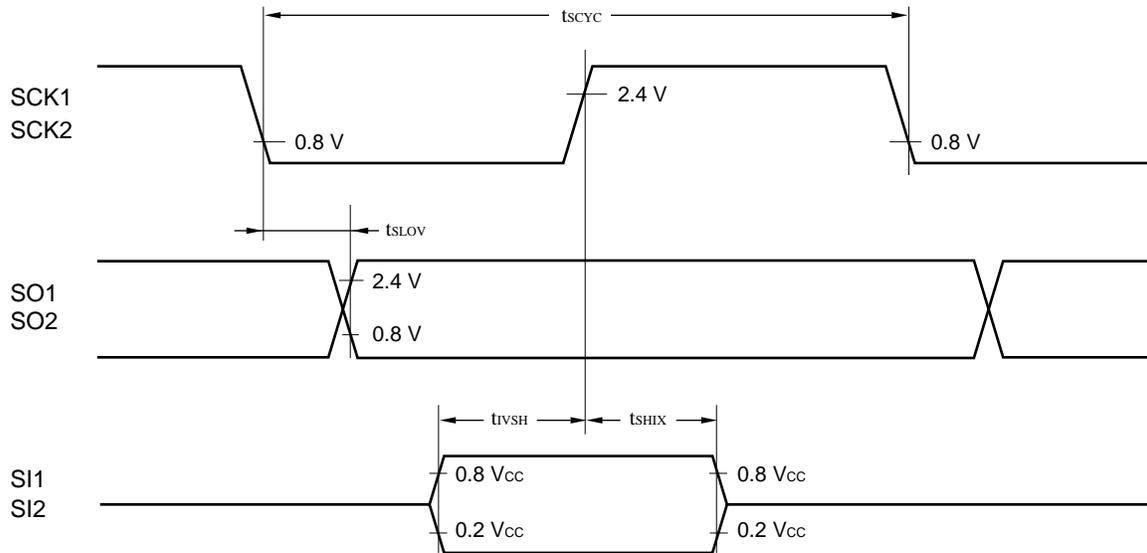
Internal Shift Clock Mode

External Shift Clock Mode
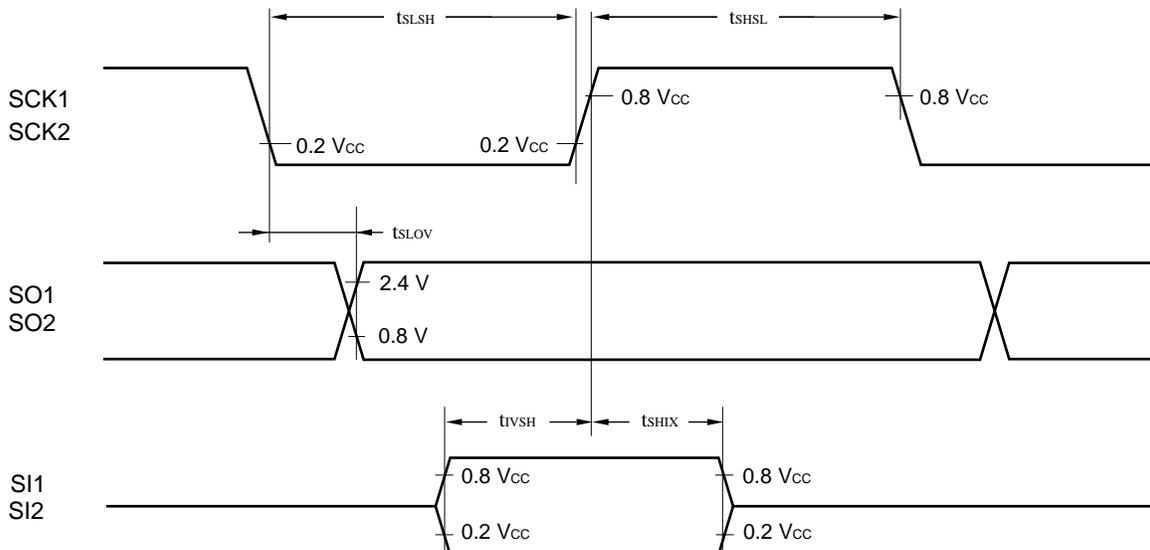
(6) Peripheral Input Timing

$(V_{CC} = +5.0 \text{ V}\pm10\%, AV_{SS} = V_{SS} = 0.0 \text{ V}, T_A = -40°C \text{ to } +85°C)$

Parameter	Symbol	Pin	Condition	Value Min.	Value Max.	Unit	Remarks
Peripheral input "H" pulse width 1	t_{ILIH1}	PWC, EC, INT0 to INT3	—	$2\ t_{inst}*$	—	µs	
Peripheral input "L" pulse width 1	t_{IHIL1}			$2\ t_{inst}*$	—	µs	
Peripheral input "H" pulse width 2	t_{ILIH2}	ADST	A/D mode	$32\ t_{inst}*$	—	µs	
Peripheral input "L" pulse width 2	t_{IHIL2}			$32\ t_{inst}*$	—	µs	
Peripheral input "H" pulse width 2	t_{ILIH2}		Sense mode	$8\ t_{inst}*$	—	µs	
Peripheral input "L" pulse width 2	t_{IHIL2}			$8\ t_{inst}*$	—	µs	

* : For information on $t_{inst,}$ see "(4) Instruction Cycle."
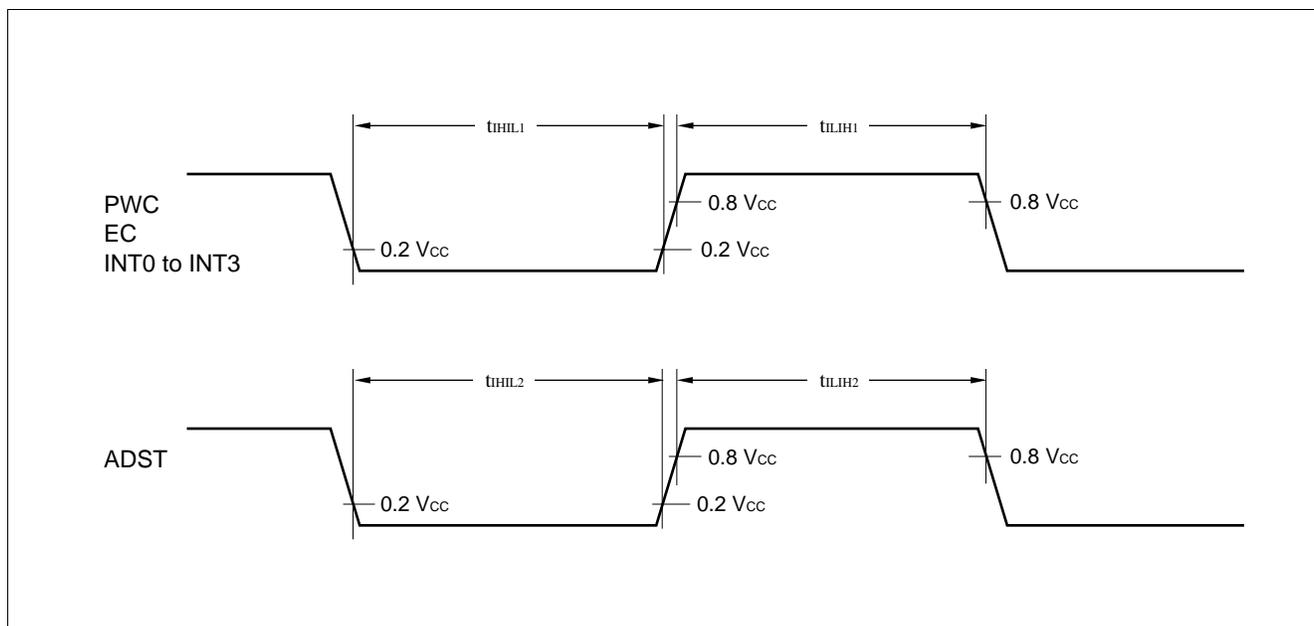
5. A/D Converter Electrical Characteristics

(AV$_{CC}$ = V$_{CC}$ = +3.5 V to +6.0 V, AV$_{SS}$ = V$_{SS}$ = 0.0 V, T$_A$ = −40°C to +85°C)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Resolution	—	—	—	—	—	8	bit	
Total error			AVR = AV$_{CC}$	—	—	±1.5	LSB	
Linearity error				—	—	±1.0	LSB	
Differential linearity error				—	—	±0.9	LSB	
Zero transition voltage	V$_{OT}$			AV$_{SS}$ − 1.0 LSB	AV$_{SS}$ + 0.5 LSB	AV$_{SS}$ + 2.0 LSB	mV	
Full-scale transition voltage	V$_{FST}$			AVR − 3.0 LSB	AVR − 1.5 LSB	AVR	mV	
Interchannel disparity				—	—	0.5	LSB	
A/D mode conversion time	—		—	—	44 t$_{inst}$*	—	μs	
Sense mode conversion time				—	12 t$_{inst}$*	—	μs	
Analog port input current	I$_{AIN}$	AN0 to AN7		—	—	10	μA	
Analog input voltage	—			0.0	—	AVR	V	
Reference voltage	—	AVR		0.0	—	AV$_{CC}$	V	
Reference voltage supply current	I$_R$		AVR = 5.0 V, when A/D conversion activated	—	100	—	μA	
	I$_{RH}$		AVR = 5.0 V, when A/D conversion stopped	—	—	1	μA	

* : For information on t$_{inst}$, see "(4) Instruction Cycle" in "4. AC Characteristics."

(1) A/D Glossary

- Resolution
  Analog changes that are identifiable with the A/D converter.
  When the number of bits is 8, analog voltage can be divided into 2^8 = 256.

- Linearity error (unit: LSB)
  The deviation of the straight line connecting the zero transition point ("0000 0000" ↔ "0000 0001") with the full-scale transition point ("1111 1111" ↔ "1111 1110") from actual conversion characteristics

- Differential linearity error (unit: LSB)
  The deviation of input voltage needed to change the output code by 1 LSB from the theoretical value

- Total error (unit: LSB)
  The difference between theoretical and actual conversion values

The figure shows a graph with "Digital output" on the vertical axis and "Analog input" on the horizontal axis, illustrating the theoretical and actual conversion values. The digital output values range from 0000 0000 0000 at the bottom to 1111 1111 1111 at the top.

Labels on the vertical axis (top to bottom):
1111 1111
1111 1110

Theoretical conversion value
Actual conversion value
(1 LSB × N + V_{OT})

0000 0010
0000 0001
0000 0000

Horizontal axis labels: V_{OT}, V_{NT}, $V_{(N+1)T}$, V_{FST}, Analog input

Equations:

$$1 \text{ LSB} = \frac{AVR}{256}$$

$$\text{Linearity error} = \frac{V_{NT} - (1 \text{ LSB} \times N + V_{OT})}{1 \text{ LSB}}$$

$$\text{Differential linearity error} = \frac{V_{(N+1)T} - V_{NT}}{1 \text{ LSB}} - 1$$

$$\text{Total error} = \frac{V_{NT} - (1 \text{ LSB} \times N + 1 \text{ LSB})}{1 \text{ LSB}}$$

(2) Precautions

• Input impedance of the analog input pins

The A/D converter contains a sample hold circuit as illustrated below to fetch analog input voltage into the sample hold capacitor for eight instruction cycles after activating A/D conversion.

For this reason, if the output impedance of the external circuit for the analog input is high, analog input voltage might not stabilize within the analog input sampling period. Therefore, it is recommended to keep the output impedance of the external circuit low (below 10 kΩ).

Note that if the impedance cannot be kept low, it is recommended to connect an external capacitor of about 0.1 μF for the analog input pin.

Analog Input Equivalent Circuit

If the analog input impedance is higher than 10 kΩ, it is recommended to connect an external capacitor of approx. 0.1 μF.

Analog input pin

Sample hold circuit
C ≑ 33 pF

R ≑ 6 kΩ

Comparator

Close for 8 instruction cycles after activating A/D conversion.

Analog channel selector
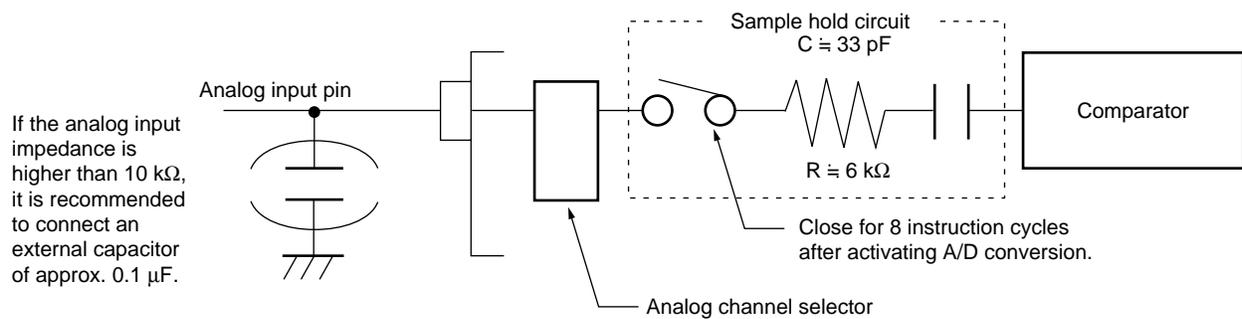
• Error

The smaller the | AVR − AV_{SS} |, the greater the error would become relatively.

■ INSTRUCTIONS

Execution instructions can be divided into the following four groups:

- Transfer
- Arithmetic operation
- Branch
- Others

Table 1 lists symbols used for notation of instructions.

Table 1   Instruction Symbols

Symbol	Meaning
dir	Direct address (8 bits)
off	Offset (8 bits)
ext	Extended address (16 bits)
#vct	Vector table number (3 bits)
#d8	Immediate data (8 bits)
#d16	Immediate data (16 bits)
dir: b	Bit direct address (8:3 bits)
rel	Branch relative address (8 bits)
@	Register indirect (Example: @A, @IX, @EP)
A	Accumulator A (Whether its length is 8 or 16 bits is determined by the instruction in use.)
AH	Upper 8 bits of accumulator A (8 bits)
AL	Lower 8 bits of accumulator A (8 bits)
T	Temporary accumulator T (Whether its length is 8 or 16 bits is determined by the instruction in use.)
TH	Upper 8 bits of temporary accumulator T (8 bits)
TL	Lower 8 bits of temporary accumulator T (8 bits)
IX	Index register IX (16 bits)

(Continued)

(Continued)

Symbol	Meaning
EP	Extra pointer EP (16 bits)
PC	Program counter PC (16 bits)
SP	Stack pointer SP (16 bits)
PS	Program status PS (16 bits)
dr	Accumulator A or index register IX (16 bits)
CCR	Condition code register CCR (8 bits)
RP	Register bank pointer RP (5 bits)
Ri	General-purpose register Ri (8 bits, i = 0 to 7)
$\times$	Indicates that the very $\times$ is the immediate data. (Whether its length is 8 or 16 bits is determined by the instruction in use.)
$(\times)$	Indicates that the contents of $\times$ is the target of accessing. (Whether its length is 8 or 16 bits is determined by the instruction in use.)
$((\times))$	The address indicated by the contents of $\times$ is the target of accessing. (Whether its length is 8 or 16 bits is determined by the instruction in use.)

Columns indicate the following:

Mnemonic: Assembler notation of an instruction

~: Number of instructions

#: Number of bytes

Operation: Operation of an instruction

TL, TH, AH: A content change when each of the TL, TH, and AH instructions is executed. Symbols in the column indicate the following:

- "–" indicates no change.
- dH is the 8 upper bits of operation description data.
- AL and AH must become the contents of AL and AH immediately before the instruction is executed.
- 00 becomes 00.

N, Z, V, C: An instruction of which the corresponding flag will change. If + is written in this column, the relevant instruction will change its corresponding flag.

OP code: Code of an instruction. If an instruction is more than one code, it is written according to the following rule:

Example: 48 to 4F ← This indicates 48, 49, ... 4F.

Table 2   Transfer Instructions (48 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
MOV dir,A	3	2	(dir) ← (A)	−	−	−	− − − −	45
MOV @IX +off,A	4	2	((IX) +off) ← (A)	−	−	−	− − − −	46
MOV ext,A	4	3	(ext) ← (A)	−	−	−	− − − −	61
MOV @EP,A	3	1	((EP)) ← (A)	−	−	−	− − − −	47
MOV Ri,A	3	1	(Ri) ← (A)	−	−	−	− − − −	48 to 4F
MOV A,#d8	2	2	(A) ← d8	AL	−	−	+ + − −	04
MOV A,dir	3	2	(A) ← (dir)	AL	−	−	+ + − −	05
MOV A,@IX +off	4	2	(A) ← ((IX) +off)	AL	−	−	+ + − −	06
MOV A,ext	4	3	(A) ← (ext)	AL	−	−	+ + − −	60
MOV A,@A	3	1	(A) ← ((A))	AL	−	−	+ + − −	92
MOV A,@EP	3	1	(A) ← ((EP))	AL	−	−	+ + − −	07
MOV A,Ri	3	1	(A) ← (Ri)	AL	−	−	+ + − −	08 to 0F
MOV dir,#d8	4	3	(dir) ← d8	−	−	−	− − − −	85
MOV @IX +off,#d8	5	3	((IX) +off) ← d8	−	−	−	− − − −	86
MOV @EP,#d8	4	2	((EP)) ← d8	−	−	−	− − − −	87
MOV Ri,#d8	4	2	(Ri) ← d8	−	−	−	− − − −	88 to 8F
MOVW dir,A	4	2	(dir) ← (AH),(dir + 1) ← (AL)	−	−	−	− − − −	D5
MOVW @IX +off,A	5	2	((IX) +off) ← (AH), ((IX) +off + 1) ← (AL)	−	−	−	− − − −	D6
MOVW ext,A	5	3	(ext) ← (AH), (ext + 1) ← (AL)	−	−	−	− − − −	D4
MOVW @EP,A	4	1	((EP)) ← (AH),((EP) + 1) ← (AL)	−	−	−	− − − −	D7
MOVW EP,A	2	1	(EP) ← (A)	−	−	−	− − − −	E3
MOVW A,#d16	3	3	(A) ← d16	AL	AH	dH	+ + − −	E4
MOVW A,dir	4	2	(AH) ← (dir), (AL) ← (dir + 1)	AL	AH	dH	+ + − −	C5
MOVW A,@IX +off	5	2	(AH) ← ((IX) +off), (AL) ← ((IX) +off + 1)	AL	AH	dH	+ + − −	C6
MOVW A,ext	5	3	(AH) ← (ext), (AL) ← (ext + 1)	AL	AH	dH	+ + − −	C4
MOVW A,@A	4	1	(AH) ← ((A)), (AL) ← ((A)) + 1)	AL	AH	dH	+ + − −	93
MOVW A,@EP	4	1	(AH) ← ((EP)), (AL) ← ((EP) + 1)	AL	AH	dH	+ + − −	C7
MOVW A,EP	2	1	(A) ← (EP)	−	−	dH	− − − −	F3
MOVW EP,#d16	3	3	(EP) ← d16	−	−	−	− − − −	E7
MOVW IX,A	2	1	(IX) ← (A)	−	−	−	− − − −	E2
MOVW A,IX	2	1	(A) ← (IX)	−	−	dH	− − − −	F2
MOVW SP,A	2	1	(SP) ← (A)	−	−	−	− − − −	E1
MOVW A,SP	2	1	(A) ← (SP)	−	−	dH	− − − −	F1
MOV @A,T	3	1	((A)) ← (T)	−	−	−	− − − −	82
MOVW @A,T	4	1	((A)) ← (TH),((A) + 1) ← (TL)	−	−	−	− − − −	83
MOVW IX,#d16	3	3	(IX) ← d16	−	−	−	− − − −	E6
MOVW A,PS	2	1	(A) ← (PS)	−	−	dH	− − − −	70
MOVW PS,A	2	1	(PS) ← (A)	−	−	−	+ + + +	71
MOVW SP,#d16	3	3	(SP) ← d16	−	−	−	− − − −	E5
SWAP	2	1	(AH) ↔ (AL)	−	−	AL	− − − −	10
SETB dir: b	4	2	(dir): b ← 1	−	−	−	− − − −	A8 to AF
CLRB dir: b	4	2	(dir): b ← 0	−	−	−	− − − −	A0 to A7
XCH A,T	2	1	(AL) ↔ (TL)	AL	−	−	− − − −	42
XCHW A,T	3	1	(A) ↔ (T)	AL	AH	dH	− − − −	43
XCHW A,EP	3	1	(A) ↔ (EP)	−	−	dH	− − − −	F7
XCHW A,IX	3	1	(A) ↔ (IX)	−	−	dH	− − − −	F6
XCHW A,SP	3	1	(A) ↔ (SP)	−	−	dH	− − − −	F5
MOVW A,PC	2	1	(A) ← (PC)	−	−	dH	− − − −	F0

Notes: • During byte transfer to A, T ← A is restricted to low bytes.
  • Operands in more than one operand instruction must be stored in the order in which their mnemonics are written. (Reverse arrangement of F²MC-8 family)

Table 3 Arithmetic Operation Instructions (62 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
ADDC A,Ri	3	1	(A) ← (A) + (Ri) + C	–	–	–	+ + + +	28 to 2F
ADDC A,#d8	2	2	(A) ← (A) + d8 + C	–	–	–	+ + + +	24
ADDC A,dir	3	2	(A) ← (A) + (dir) + C	–	–	–	+ + + +	25
ADDC A,@IX +off	4	2	(A) ← (A) + ((IX) +off) + C	–	–	–	+ + + +	26
ADDC A,@EP	3	1	(A) ← (A) + ((EP)) + C	–	–	–	+ + + +	27
ADDCW A	3	1	(A) ← (A) + (T) + C	–	–	dH	+ + + +	23
ADDC A	2	1	(AL) ← (AL) + (TL) + C	–	–	–	+ + + +	22
SUBC A,Ri	3	1	(A) ← (A) – (Ri) – C	–	–	–	+ + + +	38 to 3F
SUBC A,#d8	2	2	(A) ← (A) – d8 – C	–	–	–	+ + + +	34
SUBC A,dir	3	2	(A) ← (A) – (dir) – C	–	–	–	+ + + +	35
SUBC A,@IX +off	4	2	(A) ← (A) – ((IX) +off) – C	–	–	–	+ + + +	36
SUBC A,@EP	3	1	(A) ← (A) – ((EP)) – C	–	–	–	+ + + +	37
SUBCW A	3	1	(A) ← (T) – (A) – C	–	–	dH	+ + + +	33
SUBC A	2	1	(AL) ← (TL) – (AL) – C	–	–	–	+ + + +	32
INC Ri	4	1	(Ri) ← (Ri) + 1	–	–	–	+ + + –	C8 to CF
INCW EP	3	1	(EP) ← (EP) + 1	–	–	–	– – – –	C3
INCW IX	3	1	(IX) ← (IX) + 1	–	–	–	– – – –	C2
INCW A	3	1	(A) ← (A) + 1	–	–	dH	+ + – –	C0
DEC Ri	4	1	(Ri) ← (Ri) – 1	–	–	–	+ + + –	D8 to DF
DECW EP	3	1	(EP) ← (EP) – 1	–	–	–	– – – –	D3
DECW IX	3	1	(IX) ← (IX) – 1	–	–	–	– – – –	D2
DECW A	3	1	(A) ← (A) – 1	–	–	dH	+ + – –	D0
MULU A	19	1	(A) ← (AL) × (TL)	–	–	dH	– – – –	01
DIVU A	21	1	(A) ← (T) / (AL),MOD → (T)	dL	00	00	– – – –	11
ANDW A	3	1	(A) ← (A) ∧ (T)	–	–	dH	+ + R –	63
ORW A	3	1	(A) ← (A) ∨ (T)	–	–	dH	+ + R –	73
XORW A	3	1	(A) ← (A) ∀ (T)	–	–	dH	+ + R –	53
CMP A	2	1	(TL) – (AL)	–	–	–	+ + + +	12
CMPW A	3	1	(T) – (A)	–	–	–	+ + + +	13
RORC A	2	1	→ C → A ⌐	–	–	–	+ + – +	03
ROLC A	2	1	⌐ C ← A ←	–	–	–	+ + – +	02
CMP A,#d8	2	2	(A) – d8	–	–	–	+ + + +	14
CMP A,dir	3	2	(A) – (dir)	–	–	–	+ + + +	15
CMP A,@EP	3	1	(A) – ((EP))	–	–	–	+ + + +	17
CMP A,@IX +off	4	2	(A) – ((IX) +off)	–	–	–	+ + + +	16
CMP A,Ri	3	1	(A) – (Ri)	–	–	–	+ + + +	18 to 1F
DAA	2	1	Decimal adjust for addition	–	–	–	+ + + +	84
DAS	2	1	Decimal adjust for subtraction	–	–	–	+ + + +	94
XOR A	2	1	(A) ← (AL) ∀ (TL)	–	–	–	+ + R –	52
XOR A,#d8	2	2	(A) ← (AL) ∀ d8	–	–	–	+ + R –	54
XOR A,dir	3	2	(A) ← (AL) ∀ (dir)	–	–	–	+ + R –	55
XOR A,@EP	3	1	(A) ← (AL) ∀ ((EP))	–	–	–	+ + R –	57
XOR A,@IX +off	4	2	(A) ← (AL) ∀ ((IX) +off)	–	–	–	+ + R –	56
XOR A,Ri	3	1	(A) ← (AL) ∀ (Ri)	–	–	–	+ + R –	58 to 5F
AND A	2	1	(A) ← (AL) ∧ (TL)	–	–	–	+ + R –	62
AND A,#d8	2	2	(A) ← (AL) ∧ d8	–	–	–	+ + R –	64
AND A,dir	3	2	(A) ← (AL) ∧ (dir)	–	–	–	+ + R –	65

(Continued)

(Continued)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
AND A,@EP	3	1	(A) ← (AL) ∧ ((EP))	–	–	–	+ + R –	67
AND A,@IX +off	4	2	(A) ← (AL) ∧ ((IX) +off)	–	–	–	+ + R –	66
AND A,Ri	3	1	(A) ← (AL) ∧ (Ri)	–	–	–	+ + R –	68 to 6F
OR A	2	1	(A) ← (AL) ∨ (TL)	–	–	–	+ + R –	72
OR A,#d8	2	2	(A) ← (AL) ∨ d8	–	–	–	+ + R –	74
OR A,dir	3	2	(A) ← (AL) ∨ (dir)	–	–	–	+ + R –	75
OR A,@EP	3	1	(A) ← (AL) ∨ ((EP))	–	–	–	+ + R –	77
OR A,@IX +off	4	2	(A) ← (AL) ∨ ((IX) +off)	–	–	–	+ + R –	76
OR A,Ri	3	1	(A) ← (AL) ∨ (Ri)	–	–	–	+ + R –	78 to 7F
CMP dir,#d8	5	3	(dir) – d8	–	–	–	+ + + +	95
CMP @EP,#d8	4	2	((EP)) – d8	–	–	–	+ + + +	97
CMP @IX +off,#d8	5	3	((IX) + off) – d8	–	–	–	+ + + +	96
CMP Ri,#d8	4	2	(Ri) – d8	–	–	–	+ + + +	98 to 9F
INCW SP	3	1	(SP) ← (SP) + 1	–	–	–	– – – –	C1
DECW SP	3	1	(SP) ← (SP) – 1	–	–	–	– – – –	D1

Table 4   Branch Instructions (17 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
BZ/BEQ rel	3	2	If Z = 1 then PC ← PC + rel	–	–	–	– – – –	FD
BNZ/BNE rel	3	2	If Z = 0 then PC ← PC + rel	–	–	–	– – – –	FC
BC/BLO rel	3	2	If C = 1 then PC ← PC + rel	–	–	–	– – – –	F9
BNC/BHS rel	3	2	If C = 0 then PC ← PC + rel	–	–	–	– – – –	F8
BN rel	3	2	If N = 1 then PC ← PC + rel	–	–	–	– – – –	FB
BP rel	3	2	If N = 0 then PC ← PC + rel	–	–	–	– – – –	FA
BLT rel	3	2	If V ∀ N = 1 then PC ← PC + rel	–	–	–	– – – –	FF
BGE rel	3	2	If V ∀ N = 0 then PC ← PC + rel	–	–	–	– – – –	FE
BBC dir: b,rel	5	3	If (dir: b) = 0 then PC ← PC + rel	–	–	–	– + – –	B0 to B7
BBS dir: b,rel	5	3	If (dir: b) = 1 then PC ← PC + rel	–	–	–	– + – –	B8 to BF
JMP @A	2	1	(PC) ← (A)	–	–	–	– – – –	E0
JMP ext	3	3	(PC) ← ext	–	–	–	– – – –	21
CALLV #vct	6	1	Vector call	–	–	–	– – – –	E8 to EF
CALL ext	6	3	Subroutine call	–	–	–	– – – –	31
XCHW A,PC	3	1	(PC) ← (A),(A) ← (PC) + 1	–	–	dH	– – – –	F4
RET	4	1	Return from subrountine	–	–	–	– – – –	20
RETI	6	1	Return form interrupt	–	–	–	Restore	30

Table 5   Other Instructions (9 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
PUSHW A	4	1		–	–	–	– – – –	40
POPW A	4	1		–	–	dH	– – – –	50
PUSHW IX	4	1		–	–	–	– – – –	41
POPW IX	4	1		–	–	–	– – – –	51
NOP	1	1		–	–	–	– – – –	00
CLRC	1	1		–	–	–	– – – R	81
SETC	1	1		–	–	–	– – – S	91
CLRI	1	1		–	–	–	– – – –	80
SETI	1	1		–	–	–	– – – –	90

■ INSTRUCTION MAP

H \ L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	SWAP	RET	RETI	PUSHW A	POPW A	MOV A,ext	MOVW A,PS	CLRI	SETI	CLRB dir:0	BBC dir:0,rel	INCW A	DECW A	JMP @A	MOVW A,PC
1	MULU A	DIVU A	JMP addr16	CALL addr16	PUSHW IX	POPW IX	MOV ext,A	MOVW PS,A	CLRC	SETC	CLRB dir:1	BBC dir:1,rel	INCW SP	DECW SP	MOVW SP,A	MOVW A,SP
2	ROLC A	CMP A	ADDC A	SUBC A	XCH A,T	XOR A	AND A	OR A	MOV @A,T	MOV A,@A	CLRB dir:2	BBC dir:2,rel	INCW IX	DECW IX	MOVW IX,A	MOVW A,IX
3	RORC A	CMPW A	ADDCW A	SUBCW A	XCHW A,T	XORW A	ANDW A	ORW A	MOVW @A,T	MOVW A,@A	CLRB dir:3	BBC dir:3,rel	INCW EP	DECW EP	MOVW EP,A	MOVW A,EP
4	MOV A,#d8	CMP A,#d8	ADDC A,#d8	SUBC A,#d8		XOR A,#d8	AND A,#d8	OR A,#d8	DAA	DAS	CLRB dir:4	BBC dir:4,rel	MOVW A,ext	MOVW ext,A	MOVW A,#d16	XCHW A,PC
5	MOV A,dir	CMP A,dir	ADDC A,dir	SUBC A,dir	MOV dir,A	XOR A,dir	AND A,dir	OR A,dir	MOV dir,#d8	CMP dir,#d8	CLRB dir:5	BBC dir:5,rel	MOVW A,dir	MOVW dir,A	MOVW SP,#d16	XCHW A,SP
6	MOV A,@IX+d	CMP A,@IX+d	ADDC A,@IX+d	SUBC A,@IX+d	MOV @IX+d,A	XOR A,@IX+d	AND A,@IX+d	OR A,@IX+d	MOV @IX+d,#d8	CMP @IX+d,#d8	CLRB dir:6	BBC dir:6,rel	MOVW A,@IX+d	MOVW @IX+d,A	MOVW IX,#d16	XCHW A,IX
7	MOV A,@EP	CMP A,@EP	ADDC A,@EP	SUBC A,@EP	MOV @EP,A	XOR A,@EP	AND A,@EP	OR A,@EP	MOV @EP,#d8	CMP @EP,#d8	CLRB dir:7	BBC dir:7,rel	MOVW A,@EP	MOVW @EP,A	MOVW EP,#d16	XCHW A,EP
8	MOV A,R0	CMP A,R0	ADDC A,R0	SUBC A,R0	MOV R0,A	XOR A,R0	AND A,R0	OR A,R0	MOV R0,#d8	CMP R0,#d8	SETB dir:0	BBS dir:0,rel	INC R0	DEC R0	CALLV #0	BNC rel
9	MOV A,R1	CMP A,R1	ADDC A,R1	SUBC A,R1	MOV R1,A	XOR A,R1	AND A,R1	OR A,R1	MOV R1,#d8	CMP R1,#d8	SETB dir:1	BBS dir:1,rel	INC R1	DEC R1	CALLV #1	BC rel
A	MOV A,R2	CMP A,R2	ADDC A,R2	SUBC A,R2	MOV R2,A	XOR A,R2	AND A,R2	OR A,R2	MOV R2,#d8	CMP R2,#d8	SETB dir:2	BBS dir:2,rel	INC R2	DEC R2	CALLV #2	BP rel
B	MOV A,R3	CMP A,R3	ADDC A,R3	SUBC A,R3	MOV R3,A	XOR A,R3	AND A,R3	OR A,R3	MOV R3,#d8	CMP R3,#d8	SETB dir:3	BBS dir:3,rel	INC R3	DEC R3	CALLV #3	BN rel
C	MOV A,R4	CMP A,R4	ADDC A,R4	SUBC A,R4	MOV R4,A	XOR A,R4	AND A,R4	OR A,R4	MOV R4,#d8	CMP R4,#d8	SETB dir:4	BBS dir:4,rel	INC R4	DEC R4	CALLV #4	BNZ rel
D	MOV A,R5	CMP A,R5	ADDC A,R5	SUBC A,R5	MOV R5,A	XOR A,R5	AND A,R5	OR A,R5	MOV R5,#d8	CMP R5,#d8	SETB dir:5	BBS dir:5,rel	INC R5	DEC R5	CALLV #5	BZ rel
E	MOV A,R6	CMP A,R6	ADDC A,R6	SUBC A,R6	MOV R6,A	XOR A,R6	AND A,R6	OR A,R6	MOV R6,#d8	CMP R6,#d8	SETB dir:6	BBS dir:6,rel	INC R6	DEC R6	CALLV #6	BGE rel
F	MOV A,R7	CMP A,R7	ADDC A,R7	SUBC A,R7	MOV R7,A	XOR A,R7	AND A,R7	OR A,R7	MOV R7,#d8	CMP R7,#d8	SETB dir:7	BBS dir:7,rel	INC R7	DEC R7	CALLV #7	BLT rel

■ MASK OPTIONS

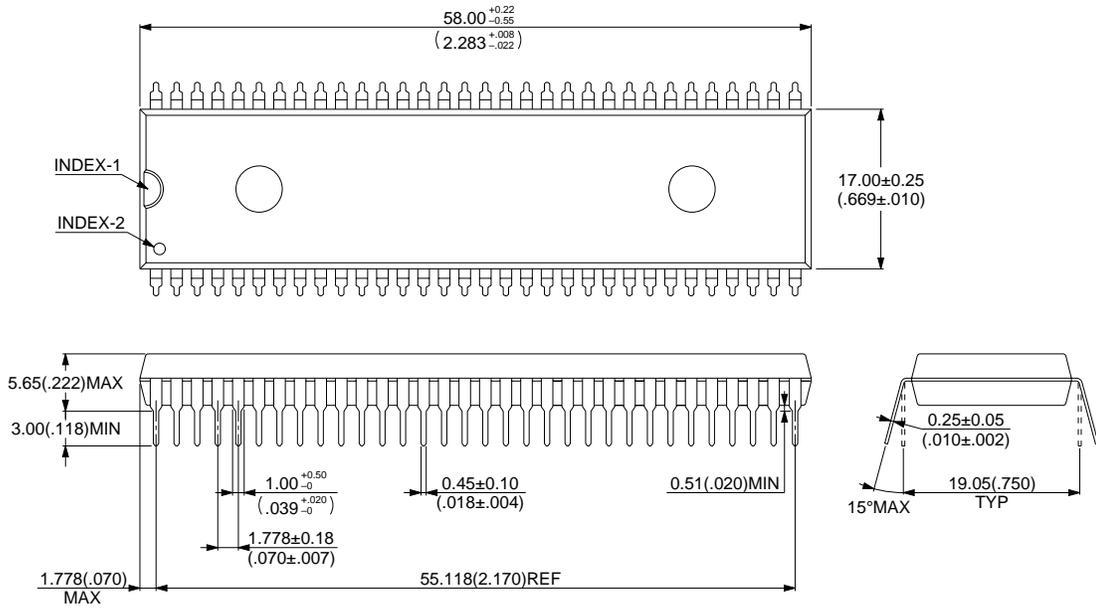| No.	Model	MB89628R/ MB89629R	MB89P629	MB89PV620
	Specifying procedure	Specify when ordering masking	Set with EPROM programmer	Setting not possible
1	Pull-up resistors P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P64	Selectable per pin. (P50 to P57 must be set to without a pull-up resistor when an A/D converter is used.)	Can be set per pin. (P40 to P47 are available only for without a pull-up resistor.)	Fixed to without pull-up resistor
2	Power-on reset With power-on reset Without power-on reset	Selectable	Setting possible	Fixed to with power-on reset
3	Oscillation stabilization time selection Crystal oscillator: ($2^{18}/F_C$) (26.2 ms/10 MHz) Ceramic oscillator: ($2^{14}/F_C$) (1.64 ms/10 MHz)	Selectable	Setting possible	Fixed to crystal oscillator of $2^{18}/F_C$
4	Reset pin output With reset output Without reset output	Selectable	Setting possible	Fixed to with reset output

■ ORDERING INFORMATION

Part number	Package	Remarks
MB89628RP-SH MB89629RP-SH MB89P629P-SH	64-pin Plastic SH-DIP (DIP-64P-M01)	
MB89628RPF MB89629RPF MB89P629PF	64-pin Plastic QFP (FPT-64P-M06)	
MB89PV620C-SH	64-pin Ceramic MDIP (MDP-64C-P02)	
MB89PV620CF	64-pin Ceramic MQFP (MQP-64C-P01)	

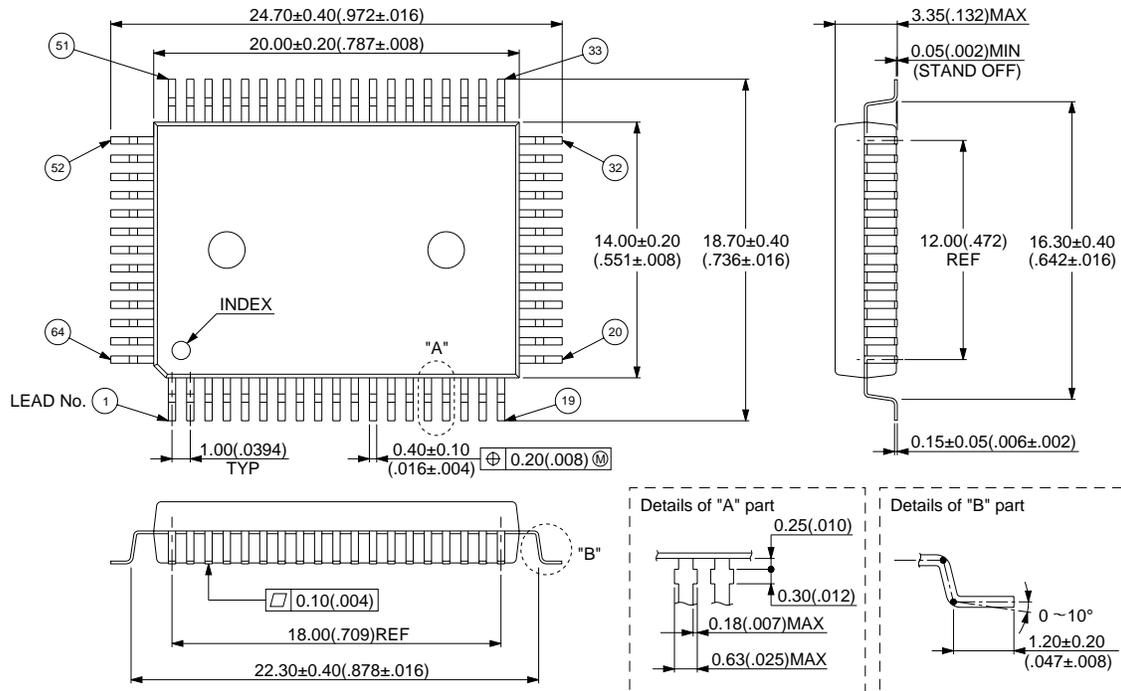## ■ PACKAGE DIMENSIONS

64-pin Plastic SH-DIP
(DIP-64P-M01)

$58.00^{+0.22}_{-0.55}$
$\left(2.283^{+.008}_{-.022}\right)$

INDEX-1

INDEX-2

17.00±0.25
(.669±.010)

5.65(.222)MAX

3.00(.118)MIN

$1.00^{+0.50}_{-0}$
$\left(.039^{+.020}_{-0}\right)$

0.45±0.10
(.018±.004)

0.51(.020)MIN

1.778±0.18
(.070±.007)

1.778(.070)
MAX

55.118(2.170)REF

0.25±0.05
(.010±.002)

19.05(.750)
TYP

15°MAX

© 1994 FUJITSU LIMITED D64001S-3C-4

Dimensions in mm (inches)

64-pin Plastic QFP
(FPT-64P-M06)

24.70±0.40(.972±.016)

20.00±0.20(.787±.008)

51

33

52

32

14.00±0.20
(.551±.008)

18.70±0.40
(.736±.016)

INDEX

"A"

64

20

LEAD No. 1

19

1.00(.0394)
TYP

0.40±0.10
(.016±.004)

⊕ 0.20(.008) Ⓜ

3.35(.132)MAX

0.05(.002)MIN
(STAND OFF)

12.00(.472)
REF

16.30±0.40
(.642±.016)

0.15±0.05(.006±.002)

▱ 0.10(.004)

"B"

18.00(.709)REF

22.30±0.40(.878±.016)

Details of "A" part

0.25(.010)

0.30(.012)

0.18(.007)MAX

0.63(.025)MAX

Details of "B" part

0~10°

1.20±0.20
(.047±.008)

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Dimensions in mm (inches)

64-pin Ceramic MDIP
(MDP-64C-P02)

56.90±0.64
(2.240±.025)

0°~9°

15.24(.600)
TYP

18.75±0.30
(.738±.012)

19.05±0.30
(.750±.012)

INDEX AREA

2.54±0.25
(.100±.010)

0.25±0.05
(.010±.002)

33.02(1.300)REF

10.16(.400)MAX

1.27±0.25
(.050±.010)

1.778±0.25
(.070±.010)

$0.46^{+0.13}_{-0.08}$
$\left(.018^{+.005}_{-.003}\right)$

0.90±0.13
(.035±.005)

3.43±0.38
(.135±.015)

55.12(2.170)REF
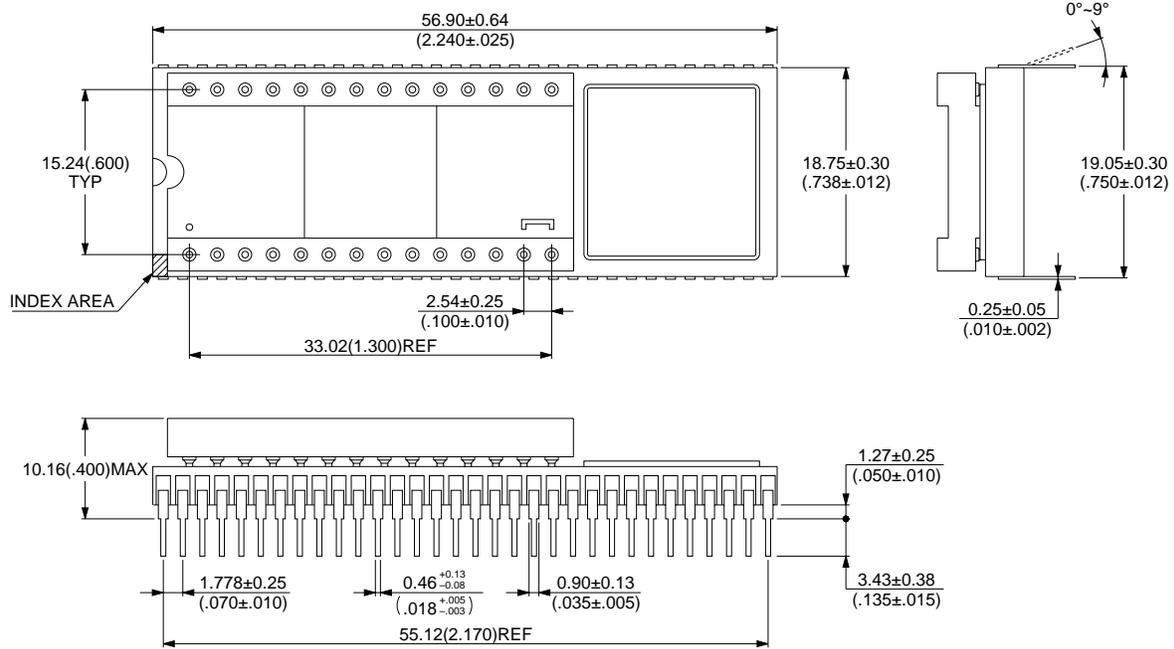
© 1994 FUJITSU LIMITED M64002SC-1-4

Dimensions in mm (inches)

64-pin Ceramic MQFP
(MQP-64C-P01)

INDEX AREA

18.70(.736)TYP

16.30±0.33
(.642±.013)
15.58±0.20
(.613±.008)

1.27±0.13
(.050±.005)

22.30±0.33
(.878±.013)

24.70(.972)
TYP

0.30(.012)
TYP

12.02(.473)
TYP

10.16(.400)
TYP

18.12±0.20
(.713±.008)

14.22(.560)
TYP

1.27±0.13
(.050±.005)

0.30(.012)TYP

7.62(.300)TYP

9.48(.373)TYP

11.68(.460)TYP

12.00(.472)TYP

1.00±0.25
(.039±.010)

$1.20^{+0.40}_{-0.20}$
$(.047^{+.016}_{-.008})$

1.00±0.25
(.039±.010)

18.00(.709)
TYP

0.40±0.10
(.016±.004)

0.40±0.10
(.016±.004)

$1.20^{+0.40}_{-0.20}$
$(.047^{+.016}_{-.008})$

0.50(.020)TYP

0.15±0.05
(.006±.002)

10.82(.426)
MAX

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Dimensions in mm (inches)

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