4-channel BTL driver for CD players

BA6198S / BA6198FP

The BA6198S and BA6198FP are ICs with an internal 4-channel BTL power driver for CD players, a 5V regulator (requires attached PNP transistor), standard operational amplifier, and reset output pin. All driver channels have a gain adjustment pin, and so can be set to the desired gain. In addition, the internal level shift circuit helps reduce the number of attached components.

●Applications

CD players, CD-ROM drives and other optical disc devices

●Features

1) 4-channel BTL driver on a HSOP 28-pin power package (BA6198FP), allowing for application miniaturization.
2) Gain is adjustable with an attached resistor.
3) Internal thermal shutdown circuit.
4) Internal 5V regulator (requires attached PNP resistor)
5) Internal standard operational amplifier.
6) Reset output pin.

●Absolute maximum ratings (Ta = 25°C)

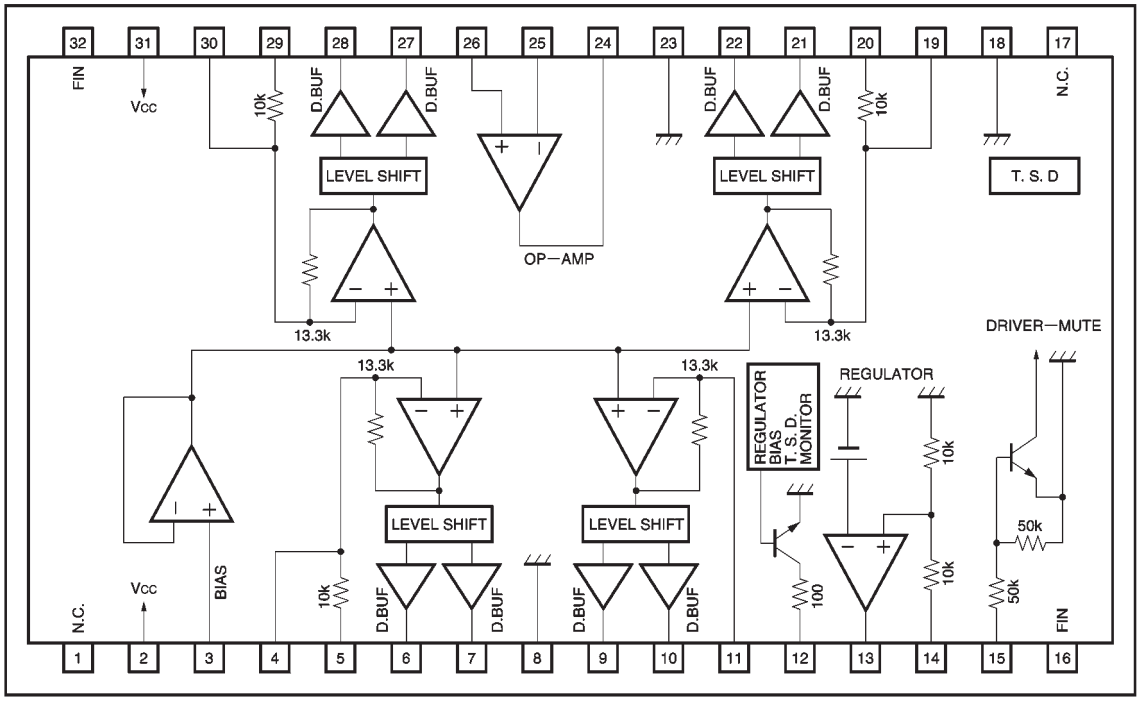
Parameter		Symbol	Limits	Unit
Power supply voltage		V_{CC}	18	V
Power dissipation	BA6198S	Pd	1700 *1	mW
	BA6198FP		1700 *2	
Operating temperature		Topr	−35～+85	℃
Storage temperature		Tstg	−55～+150	℃

*1 Unmounted 32-pin SDIP package.
Reduced by 13.6 mW for each increase in Ta of 1℃ over 25℃.
*2 When mounted on a 50×50×1 mm paper phenol board.
Reduced by 13.6 mW for each increase in Ta of 1℃ over 25℃.

●Recommended operating conditions (Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
Power supply voltage	V_{CC}	6.0	—	9.0	V	
		5.5	—	9.0	V	Regulator not used

●Block diagram

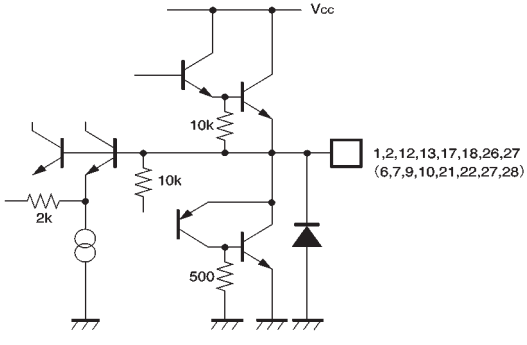


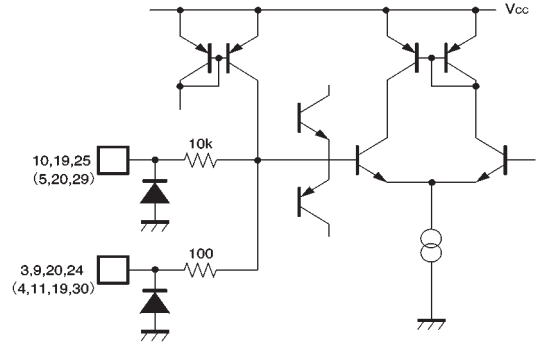
●Pin descriptions

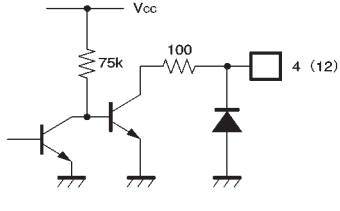
Pin No.	Pin name	Function	Pin No.	Pin name	Function
1	N.C.	N.C.	17	N.C.	N.C.
2	Vcc	Power supply	18	GND	GND
3	BIAS IN	Bias amplifier input	19	VIN3'	Driver channel 3 gain adjustment input
4	VIN1'	Driver channel 1 gain adjustment input	20	VIN3	Driver channel 3 input
5	VIN1	Driver channel 1 input	21	V03 (+)	Driver channel 3 positive output
6	V01 (+)	Driver channel 1 positive output	22	V03 (−)	Driver channel 3 negative output
7	V01 (−)	Driver channel 1 negative output	23	GND	Substrate ground
8	GND	Substrate ground	24	OP OUT	Operational amplifier output
9	V02 (−)	Driver channel 2 negative output	25	OP IN (−)	Operational amplifier negative input
10	V02 (+)	Driver channel 2 positive output	26	OP IN (+)	Operational amplifier positive input
11	VIN2'	Driver channel 2 gain adjustment input	27	V04 (−)	Driver channel 4 negative output
12	RESET	Reset output	28	V04 (+)	Driver channel 4 positive output
13	REG - B	Connect to attached transistor base	29	VIN4	Driver channel 4 input
14	REG OUT	Constant voltage output (connect to attached transistor base)	30	VIN4'	Driver channel 4 gain adjustment input
15	MUTE	Mute control	31	Vcc	Power supply
16	FIN	FIN	32	FIN	FIN

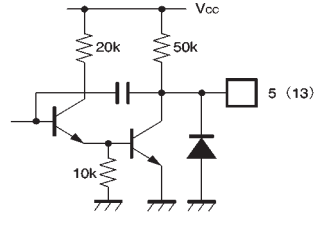
Note: Positive and negative output is relative to the polarity of the input pins.

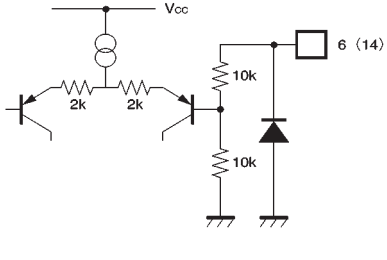
●Input / output circuits Parentheses ( ) indicate BA6198S

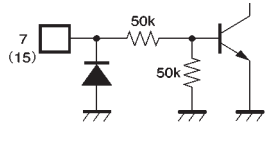


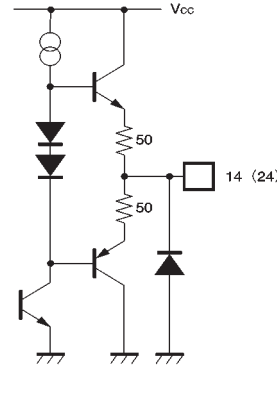


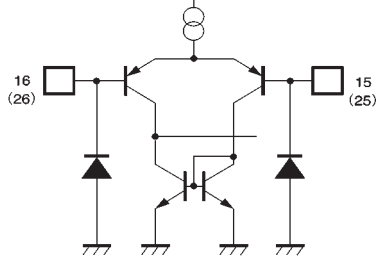


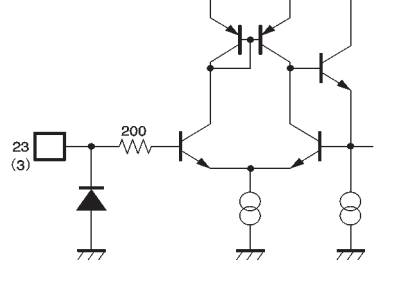












●Electrical characteristics (unless otherwise noted, Ta = 25°C, V_{CC} = 8V, f = 1kHz, R_L = 8Ω)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Quiescent current dissipation	I_{CC}	6.0	10.0	14.0	mA	No load
Output offset voltage	V_{OO}	−40	−	40	mV	
Max. output voltage high	V_{OHD}	5.2	5.6	−	V	
Max. output voltage low	V_{OLD}	−	1.3	1.55	V	
Closed loop voltage gain	G_{VC}	7.0	8.0	9.0	dB	V_{IN}=0.1V_{rms}, 1kHz(ex. channel 1)
Ripple rejection ratio	RR	−	60	−	dB	V_{IN}=0.1V_{rms}, 100Hz
Slew rate	SR	−	2.0	−	V/μs	100 kHz square wave, 3 V_{P-P} output
Mute-off voltage	V_{MOFF}	2.0	−	−	V	
〈5 V regulator〉						
Output voltage	Vreg	4.75	5.00	5.25	V	I_L=100mA
Output load variation	ΔV_{RL}	−50	0	10	mV	I_L=0～200mA
Supply voltage variation	ΔV_{CC}	−10	0	25	mV	(V_{CC}=6～9V) I_L=100mA
〈Operational amplifier〉						
Offset voltage	V_{OFOP}	−5	0	5	mV	
Input bias current	I_{BIAS}	−	−	300	nA	
Output high level voltage	V_{OHOP}	6.0	−	−	V	
Output low level voltage	V_{OLOP}	−	−	1.8	V	
Output drive current (source)	I_{SOU}	10	40	−	mA	Ground at 50Ω
Output drive current (sink)	I_{SIN}	10	50	−	mA	Vcc at 50Ω
Open loop voltage gain	G_{VO}	−	78	−	dB	V_{IN}=−75dBV, 1kHz
Slew rate	SR_{OP}	−	1	−	V/μs	100 kHz square wave, 4 V_{P-P} output
Ripple rejection ratio	RR_{OP}	50	65	−	dB	V_{IN}=−20dBV, 100Hz
Sync. signal rejection rate	CMRR	70	84	−	dB	V_{IN}=−20dBV, 1kHz
〈Reset output〉						
Reset-on threshold current	V_{THR}	−	4.0	−	V	Depends on regulator voltage
Reset-on output voltage	V_{RON}	−	−	0.5	V	Connect to 5 V at 10kΩ

◎Not designed for radiation resistance.

●Measurement circuit

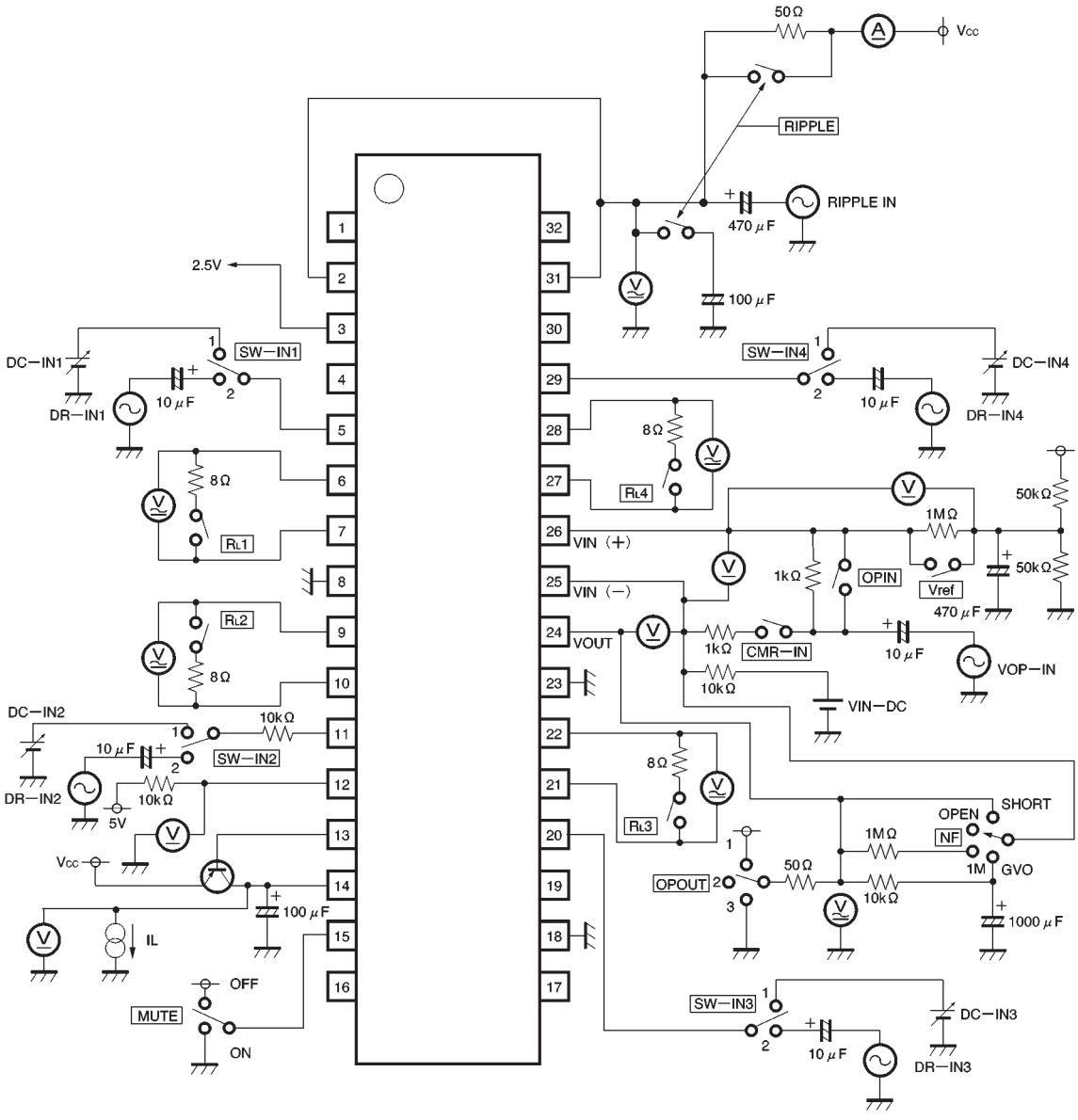


Fig.1

●Measurement circuit switch table

Parameter	Switch									Input					Conditions
	RIPPLE	MUTE	RL	OPIN	Vref	CMR −IN	NF	OP OUT	SW −IN	DR −IN	DC −IN	RIPPLE IN	VOP IN	V_{IN} DC	
Quiescent current dissipation	ON	OFF	OFF	ON	ON	OFF	SHORT	2	2	0	0	0	0	OFF	
Output offset voltage	↓	↓	ON	↓	↓	↓	↓	↓	1	↓	2.5V	↓	↓	↓	
Maximum output amplitude	↓	↓	↓	↓	↓	↓	↓	↓	2	↓	2.0 V_{rms}	↓	↓	↓	Two or more ch. not turned on at the same time
Closed loop voltage gain	↓	↓	↓	↓	↓	↓	↓	↓	↓	0.1 V_{rms}	0	↓	↓	↓	
Ripple rejection ratio	OFF	↓	↓	↓	↓	↓	↓	↓	1	0	2.5V	0.1 V_{rms}	↓	↓	
Slew rate	ON	↓	↓	↓	↓	↓	↓	↓	2	⎍	0	0	↓	↓	
〈Regulator〉															
Output voltage	↓	↓	OFF	↓	↓	↓	↓	↓	↓	0	↓	↓	↓	↓	
Output load variation	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	
Supply voltage variation	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	
〈Operational amplifier〉															
Offset voltage	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	
Input bias current	↓	↓	↓	↓	OFF	↓	1M	↓	↓	↓	↓	↓	↓	↓	
Output high level voltage	↓	↓	↓	↓	ON	↓	OPEN	↓	↓	↓	↓	↓	↓	2V	
Output low level voltage	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	6V	
Output drive current (sink)	↓	↓	↓	↓	↓	↓	SHORT	1	↓	↓	↓	↓	↓	OFF	
Output drive current (source)	↓	↓	↓	↓	↓	↓	↓	3	↓	↓	↓	↓	↓	↓	
Open loop voltage gain	↓	↓	↓	↓	↓	↓	GVO	2	↓	↓	↓	↓	−75 dBV	↓	
Slew rate	↓	↓	↓	↓	↓	↓	SHORT	↓	↓	↓	↓	↓	⎍	↓	
Ripple rejection ratio	OFF	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	0.1 V_{rms}	0	↓	
Synchronous signal rejection	ON	↓	↓	OFF	ON	ON	1M	↓	↓	↓	↓	0	0.1 V_{rms}	↓	
〈Reset output〉															
Reset-on threshold	ON	OFF	OFF	OFF	OFF	OFF	SHORT	2	2	0	0	0	0	OFF	Pin 5: open.imp--ressed on pin 6
Reset-on output voltage	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	

●Application example

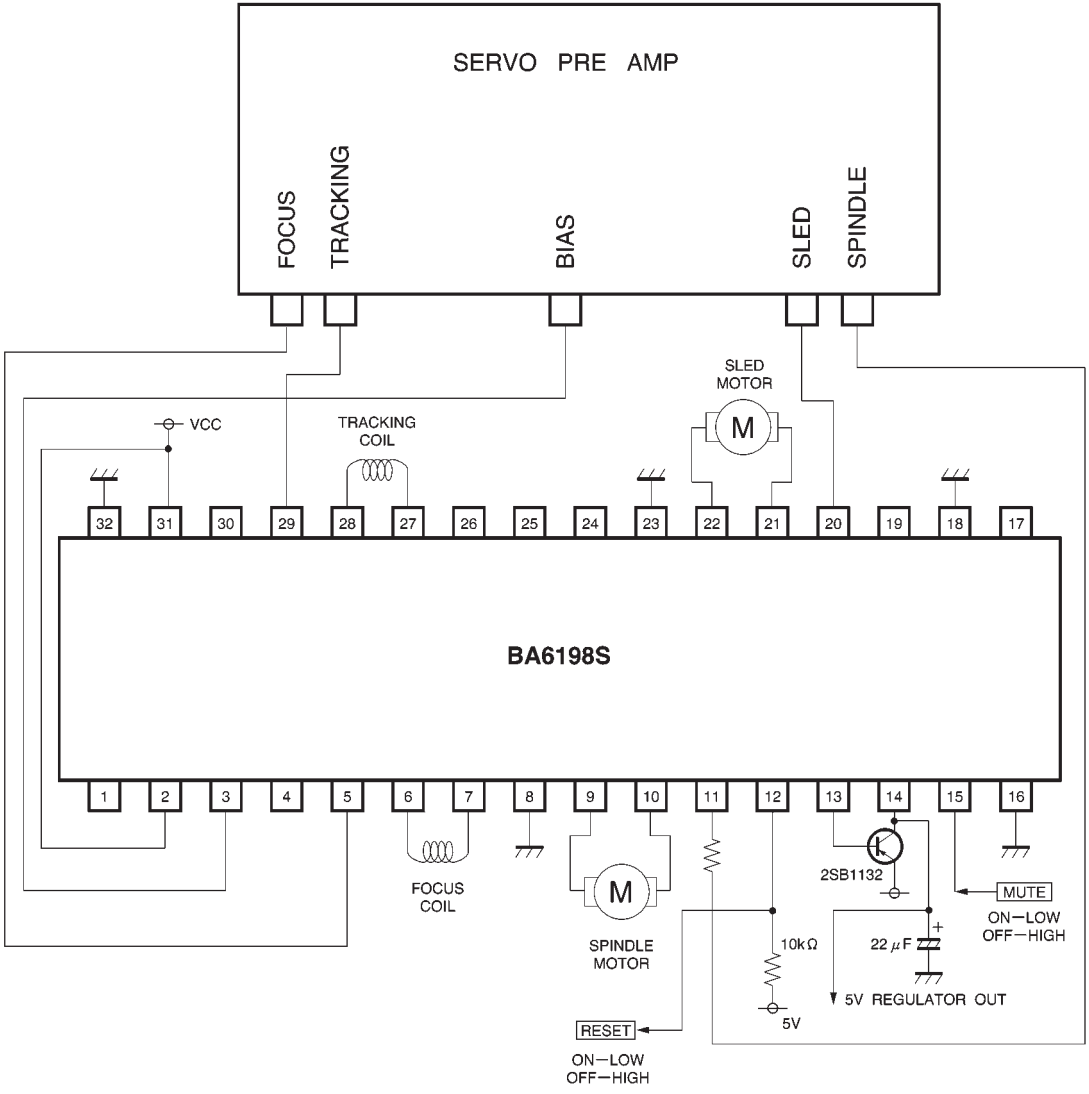


Fig.2

●Operation notes

(1) Relationship between mute and reset output

	Mute	Reset output
Drop in regulator voltage	Mute-on (all cases)	'H' → 'L'
Drop in bias voltage		'H' → 'L'
Thermal shutdown		'H' → 'L'
Muting		No change

Drop in regulator voltage · · · When the regulator voltage drops below 4.0V (typically), the reset output changes to the low level and the IC is simultaneously muted. When the regulator voltages rises above 4.2V (typically), reset output changes to the high level and muting is released.

Drop in bias voltage · · · When the bias pin voltage drops below 1.4V (typically), the IC is muted and the reset output simultaneously changes to the low level. During ordinary use, the bias voltage should be kept above 1.6V.

Thermal shutdown · · · When the chip temperature rises above 175°C (typically), the IC is muted and the reset output simultaneously changes to the low level.

Muting · · · When the mute pin voltage is opened or lowered below 0.5V, the IC is muted, but the reset output remains the same.

(2) Muting occurs during thermal shutdown, mute-on operations or a drop in the bias pin voltage or regulator voltage. In each case, only the drivers are muted. During muting, the output pins remain at the internal bias voltage, roughly (V_{CC}-V_F) / 2.

(3) Be sure to connect the IC to a 0.1μF bypass capacitor between the power supplies, at the base of the IC.

(4) The radiating fin is connected to the package's internal GND, but should also be connected to an external ground.

(5) The capacitor between regulator output (pin 8) and GND also serves to prevent oscillation of the IC, so select one with good temperature characteristics.

●Electrical characteristic curves

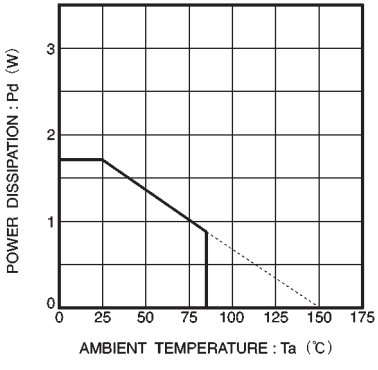


Fig. 3 Thermal derating curve

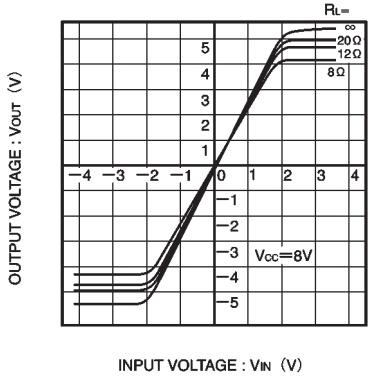


Fig. 4 Drive I / O characteristics (variable load)

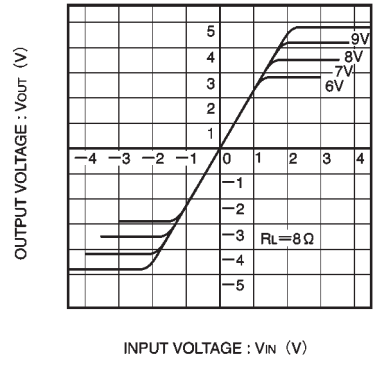


Fig. 5 Drive I / O characteristics (variable supply voltage)

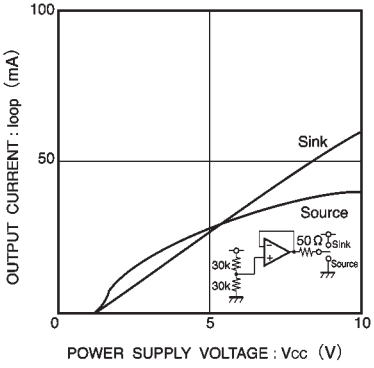


Fig. 6 Power supply voltage vs. operational amplifier output current

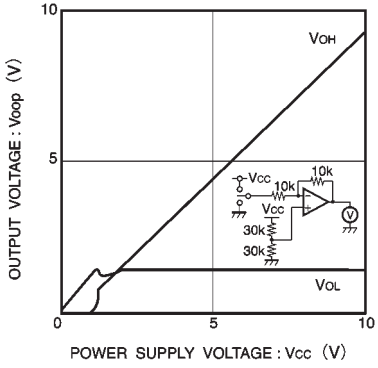


Fig. 7 Power supply voltage vs. operational amplifier high / low level output voltage

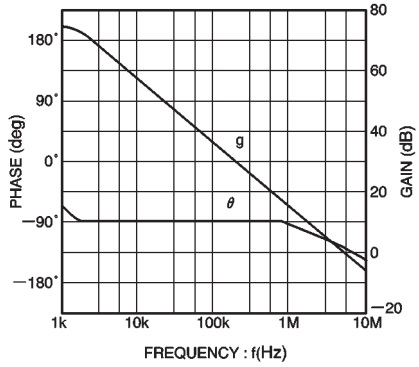


Fig. 8 Operational amplifier vs. open loop

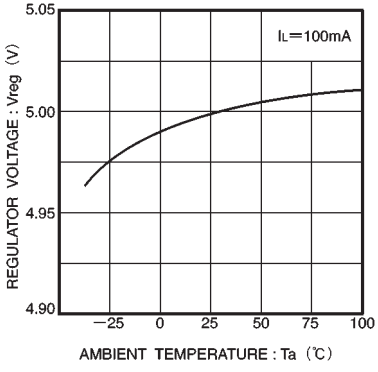


Fig. 9 Regulator voltage vs. temperature

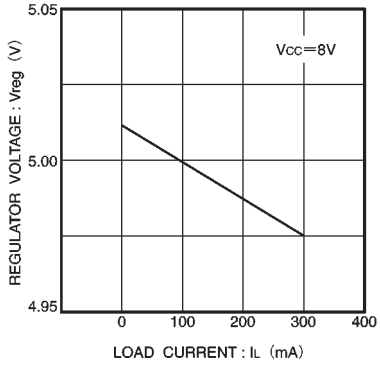
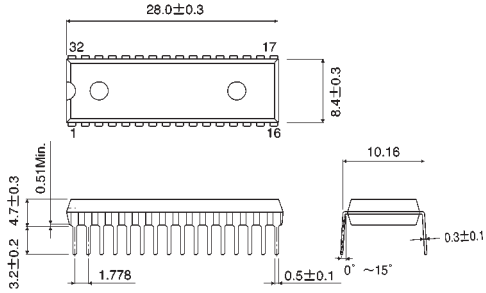


Fig. 10 Load current vs. regulator voltage

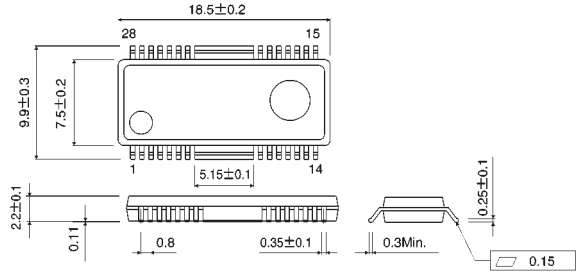
●External dimensions (Units: mm)

BA6198S



SDIP32

BA6198FP



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