Preservo amplifier for CD players

BA6386K

The BA6386K is a preservo amplifier for CD players. By using this paired with a ROHM DSP, a servo and main signal system can be configured with few external components and low power consumption.

●Applications

CD players

●Features

1) Internal RF AGC circuits.
2) Internal APC circuit.
3) Internal auto asymmetry circuit.
4) Internal disc defect detector.
5) Internal focus protect function against disc defects.

●Absolute maximum ratings (Ta = 25°C)

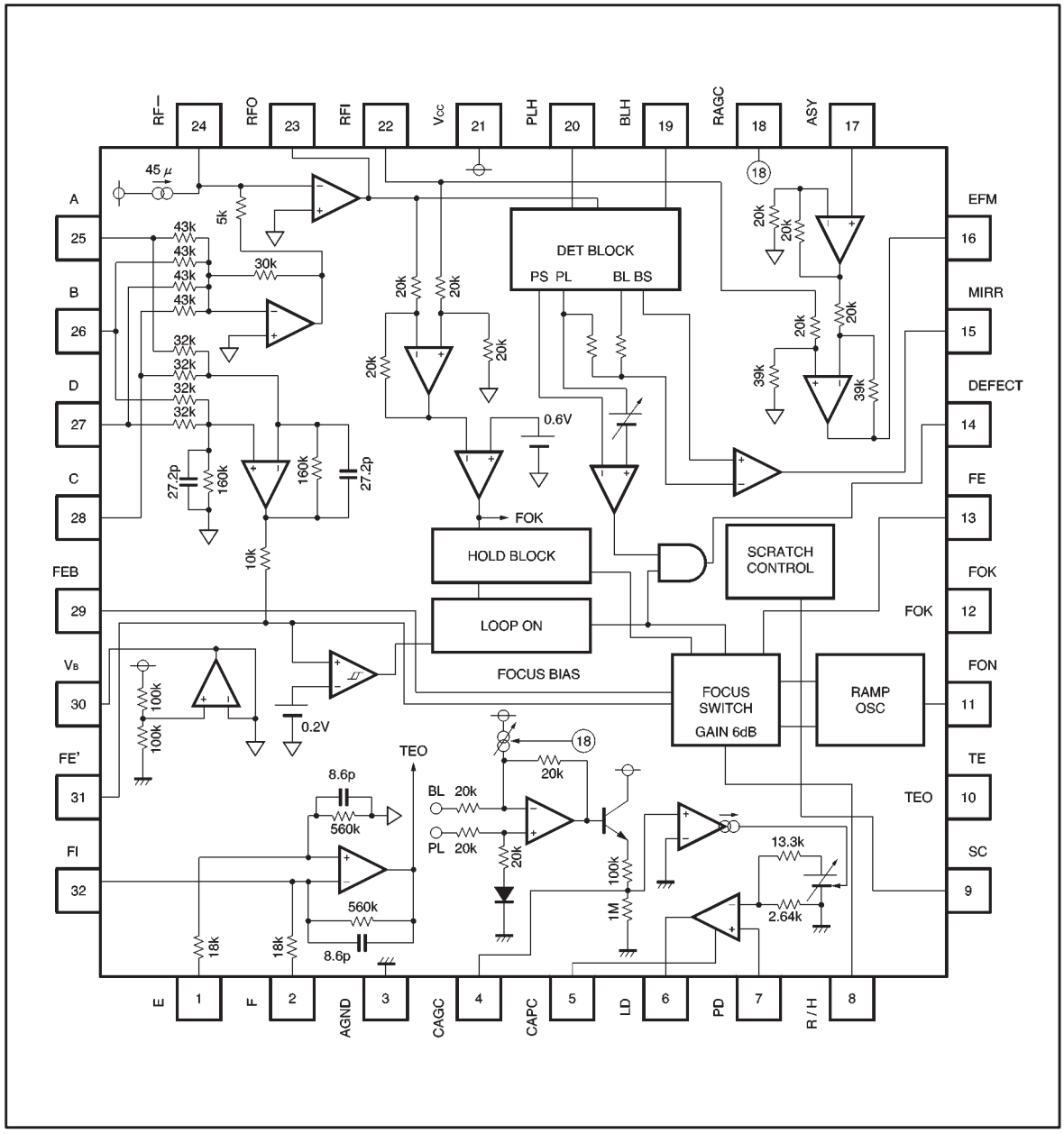
Parameter	Symbol	Limits	Unit
Power supply voltage	V_{CC}	9	V
Power dissipation	Pd	400*	mW
Operating temperature	Topr	−25～+75	℃
Storage temperature	Tstg	−55～+125	℃

* Reduced by 4mW for each increase inTa of 1℃ over 25℃.

●Recommended operating conditions (Ta = 25°C)

Paramerter	Symbol	Limits	Unit
Power supply voltage	V_{CC}	2.4～4.5	V

●Block diagram



●Pin descriptions

Pin No.	Pin name	Function
1	E	E input
2	F	F input
3	AGND	Analog GND
4	CAGC	For capacitor for AGC constant
5	CAPC	For capacitor for APC phase compensation
6	LD	APC amplifier output
7	PD	APC amplifier input
8	R / H	For capacitor for ramp wave/loop off
9	SC	For resistor for scratch depth adjustment
10	TE	Tracking error output
11	FON	Focus on control
12	FOK	Focus OK comparator output
13	FE	Focus error output 1
14	DEFECT	Defect signal output
15	MIRR	Mirror signal output
16	EFM	EFM signal output

Pin No.	Pin name	Function
17	ASY	Auto-asymmetry control input
18	RAGC	For resistor for AGC threshold adjustment
19	BLH	For capacitor for bottom long
20	PLH	For capacitor for peak long
21	V_{CC}	Power supply
22	RFI	RF output capacity coupling reinput
23	RFO	RF summing amplifier output
24	RF—	RF summing amplifier feedback input
25	A	A input
26	B	B input
27	D	D input
28	C	C input
29	FEB	Focus error bias input
30	V_B	Bias amplifier output
31	FE'	Focus error output 2
32	FI	F gain adjustment feedback

●Electrical characteristics (unless otherwise noted, Ta = 25°C and V_{CC} = 2.5V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	
Quiescent current	I_Q	—	7.7	11.7	mA	—	
〈Bias amplifier〉							
Bias voltage	V_B	1.12	1.25	1.38	V	—	
Maximum output high level voltage	I_{OH}	3.0	—	—	mA	Bias fluctuation below 200mV	
Maximum output low level voltage	I_{OL}	3.0	—	—	mA	Bias fluctuation below 200mV	
〈RF amplifier〉							
Output offset voltage	V_{OFRF}	−1.02	−0.90	−0.78	V		*
Voltage gain	G_{RF}	18.0	21.0	24.0	dB	V8=0.8V, SG5=30mV$_{P-P}$, 1kHz	
Maximum output high level amplitude	V_{OHRF}	0.90	1.10	—	V	Simultaneous AC and BD input	
Maximum output low level amplitude	V_{OLRF}	—	−1.10	−0.90	V	V9=V_B+0.25V, V_B−0.05V	*
Cutoff frequency	F_{CRF}	—	8	—	MHz	−3dB point	
〈FE amplifier〉							
Output offset voltage	V_{OFFE}	−100	−20	60	mV		*
Voltage gain AC	G_{FEAC}	23	26	29	dB	SG5=30mV$_{P-P}$, 1kHz	
Voltage gain BD	G_{FEBD}	23	26	29	dB	SG6=30mV$_{P-P}$, 1kHz	
Voltage gain difference	ΔG_{FE}	−3	0	3	dB	—	
Maximum output high level amplitude	V_{OHFE}	0.90	1.10	—	V	Measurement with AC and BD input	
Maximum output low level amplitude	V_{OLFE}	—	−1.10	−0.90	V	V9 (V10) =V_B±0.15V	*
Frequency characteristics	F_{CFE}	16	19	22	dB	SG5 (SG6) =60mV$_{P-P}$, 60kHz	
〈TE amplifier〉							
Output offset voltage	V_{OFTE}	−100	−20	60	mV		*
Voltage gain E	G_{TEE}	27	30	33	dB	SG1=30mV$_{P-P}$, 1kHz	
Voltage gain F	G_{TEF}	27	30	33	dB	SG2=30mV$_{P-P}$, 1kHz	
Voltage gain difference	ΔG_{TE}	−3	0	3	dB	—	
Maximum output high level amplitude	V_{OHTE}	0.90	1.10	—	V	Measurement with E and F input	
Maximum output low level amplitude	V_{OLTE}	—	−1.10	−0.90	V	V1 (V2) =V_B±0.1V	*
Frequency characteristics	F_{CTE}	19	22	25	dB	SG1 (SG2) =60mV$_{P-P}$, 60kHz	
〈FOK comparator〉						Input pin 22	
Threshold voltage	V_{THFK}	0.42	−0.30	−0.18	V		*
Output high level voltage	V_{OHFK}	2.0	—	—	V	V7=V_B−0.42V	
Output low level voltage	V_{OLFK}	—	—	0.5	V	V7=V_B−0.18V	
Maximum operating frequency	F_{MXFX}	45	—	—	kHz	—	
〈Asymmetry amplifier〉							
Output offset voltage	V_{OFAS}	−60	—	60	mV		*
Voltage gain 1	G_{1AS}	3	6	9	dB	Input pin 22, 80mV$_{P-P}$, 1kHz	
Voltage gain 2	G_{2AS}	8.5	11.5	14.5	dB	Input pin 17, 80mV$_{P-P}$, 1kHz	
Maximum output high level amplitude	V_{OHAS}	0.90	1.10	—	V	V7=VB±0.8	
Maximum output low level amplitude	V_{OLAS}	—	−1.10	−0.90	V	V6=VB±0.4	*

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
〈APC〉						
Output voltage 1	V_{O1AP}	1.90	2.30	—	V	230mV input at pin 7
Output voltage 2	V_{O2AP}	—	1.0	1.4	V	170mV input at pin 7, I2=1mA
Reference voltage	V_{APR}	190	200	210	mV	—
Frequency characteristics	F_{AP}	−5	−1	3	dB	SG7=40mV$_{P-P}$, 500Hz
〈AGC〉						
Reference voltage 1	V_{AGC1}	0	—	100	mV	V8=0.8V, RFO=1.2V$_{P-P}$
Reference voltage 2	V_{AGC2}	180	195	210	mV	V8=0.8V, RFO=0.7V$_{P-P}$
Attack time	R_{ATT}	70	100	130	kΩ	Measurement of internal R
Recovery time	R_{RCV}	0.7	1.0	1.3	MΩ	
〈Mirror detector〉						
Output high level voltage	V_{OHMR}	2.0	—	—	V	R_L=15kΩ
Output low level voltage	V_{OLMR}	—	—	0.5	V	—
Minimum operating frequency	F_{MNMR}	—	—	600	Hz	—
Maximum operating frequency	F_{MXMR}	30	—	—	kHz	—
Minimum input operating voltage	V_{MNMR}	—	—	0.2	V$_{P-P}$	—
Maximum input operating voltage	V_{MXMR}	1.2	—	—	V$_{P-P}$	—
〈Defect detector〉						
Output high level voltage	V_{OHDF}	2.0	—	—	V	R_L=15kΩ
Output low level voltage	V_{OLDF}	—	—	0.5	V	—
Minimum operating frequency	F_{MNDF}	—	—	1	kHz	—
Maximum operating frequency	F_{MXDF}	2	—	—	kHz	—
Minimum input operating voltage	V_{MNDF}	—	—	0.5	V$_{P-P}$	—
Maximum input operating voltage	V_{MXDF}	1.2	—	—	V$_{P-P}$	—
Scratch depth	V_{SC}	0.13	0.20	0.27	V	—
〈Ramp wave generator circuit〉						
Period	I_{SIRA}	220	340	460	ms	—
High level limit voltage	V_{LHRA}	80	124	168	mV	FEO output value *
Low level limit voltage	V_{LLRA}	−168	−124	−80	mV	
〈FON pin〉						
Inflow current	I_{IFON}	10.4	13.5	16.6	μA	—
Input threshold voltage	V_{THFO}	1.10	1.45	1.80	V	—
〈Loop on unit〉						
Loop off delay time	t_{OFLO}	4.0	6.6	10.0	ms	—
〈FZC comparator〉						
Input sensitivity level	V_{FZH}	320	400	480	mV	—
Zero cross sensitivity level	V_{FZL}	120	200	280	mV	—

∗ Standards are with V_B reference.

※When FON is LOW, 8 voltage is V_B.

※The ramp wave begins at the bottom.

※The loop will not turn on when the ramp wave is at the bottom.

※Pin 8 is charged rapidly when the loop turns on.

●Measurement circuit

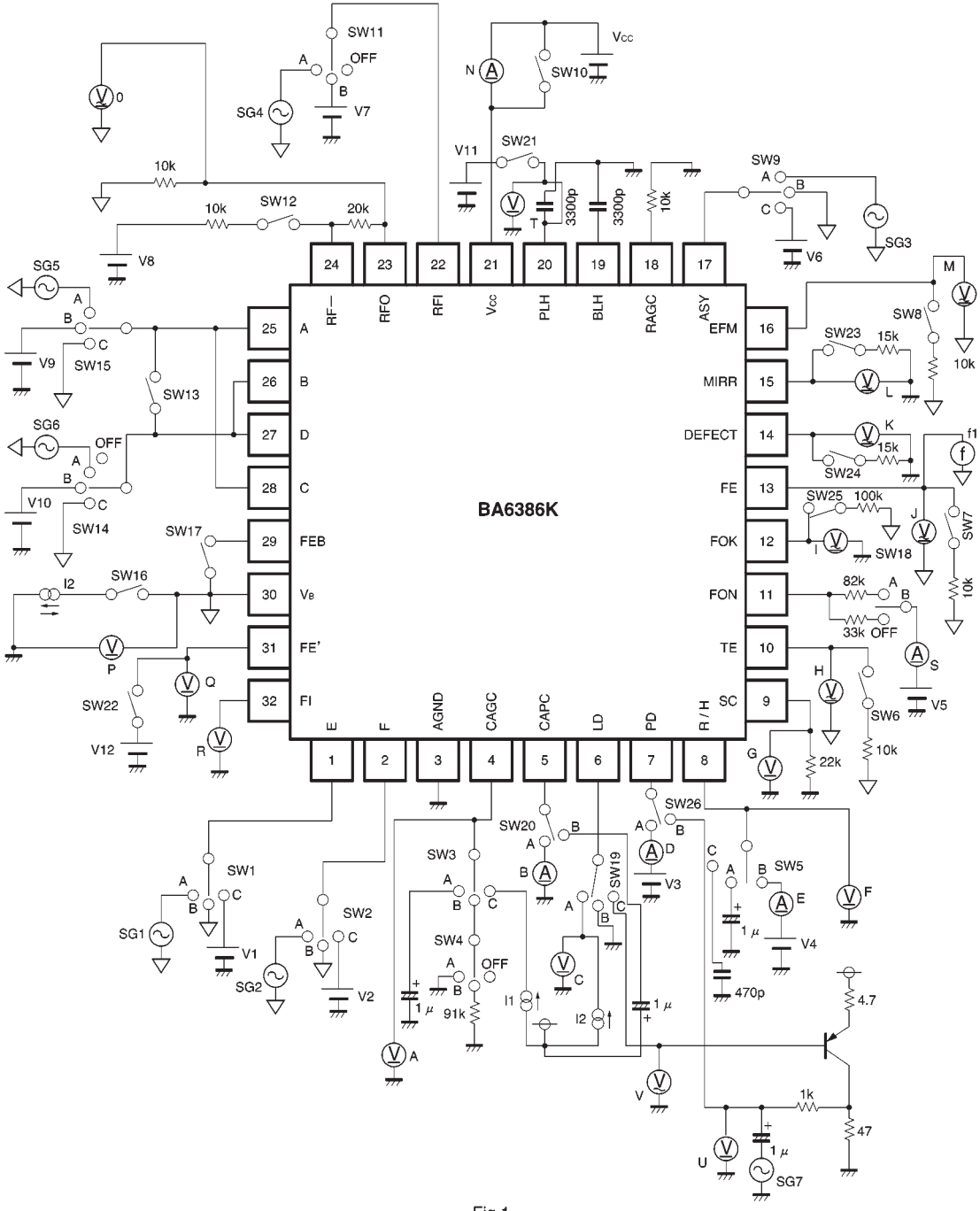


Fig.1

●Circuit operation

(1) RF amplifier, FOK comparator

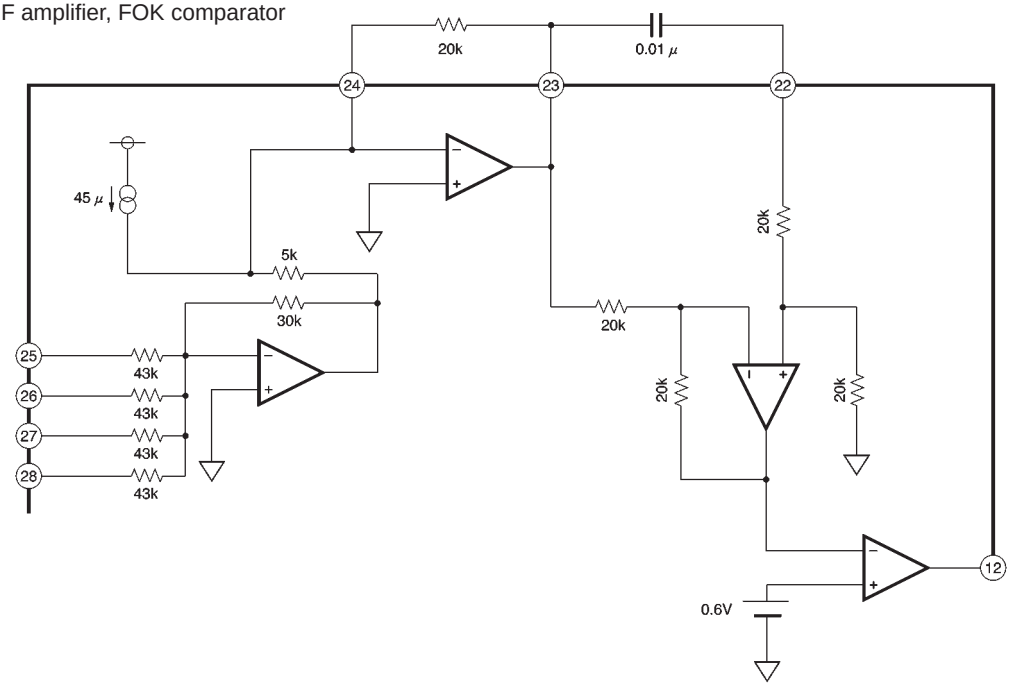


Fig.2 RF and FOK block

RFO is shifted downwards from V_B by 0.9V.
However, the resistance between pins 23 and 24 is set to 20kΩ and if this resistance is changed, use external components to adjust the shift back to 0.9V. Have the feedback resistance 10kΩ or greater.
If the DC component of RF rises 0.3V, then FOK becomes high.

(2) FE amplifier and focus search

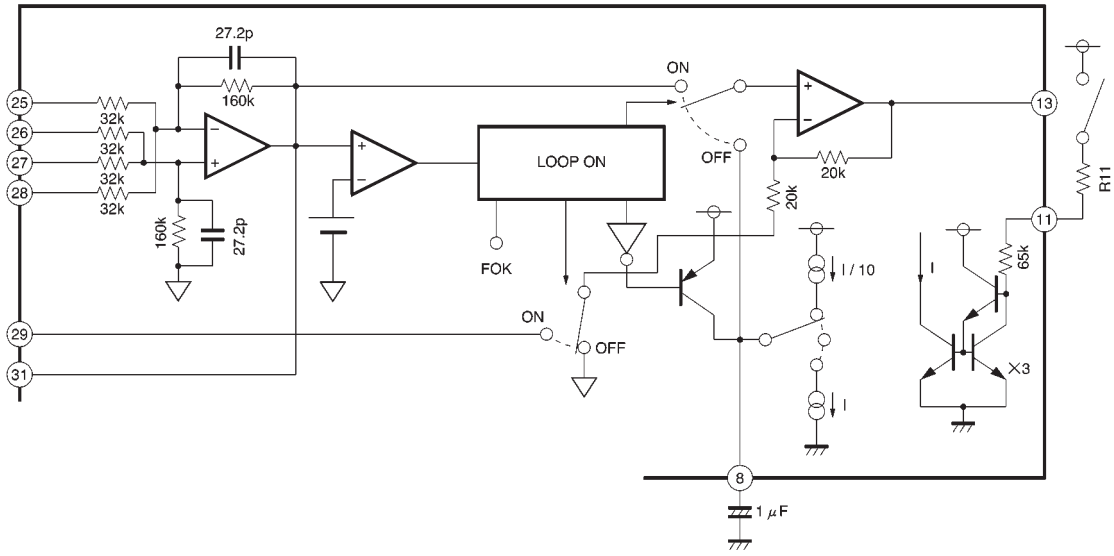


Fig.3 Focus error block

The voltage for focus search is obtained by the charging and discharging of the capacitor attached to pin 8. The charging current is I/10 and the discharging current is I. The FEO output amplitude (V_{SERCH}) at this time is determined by the formula given below.

$$V_{SERCH} = \pm I \times 15k\Omega \times 2 \ (V_B \text{ reference})$$

Moreover, from Fig. 3, I can be approximated by the formula given below.

$$I = \frac{V_{CC} - 1.4}{65k + R11} \times \frac{1}{3}$$

Set R11 so that I becomes 2μA or greater. Apply biasing to the focus error signal from pin 29. If no adjustment occurs, pin 29 = V_B.

The timing charts when the focus loop turns ON or OFF are given on the next page.

1) LOOP ON timing

When FOK turns high, the fall of FE' is detected and the FOCUS LOOP turns ON.

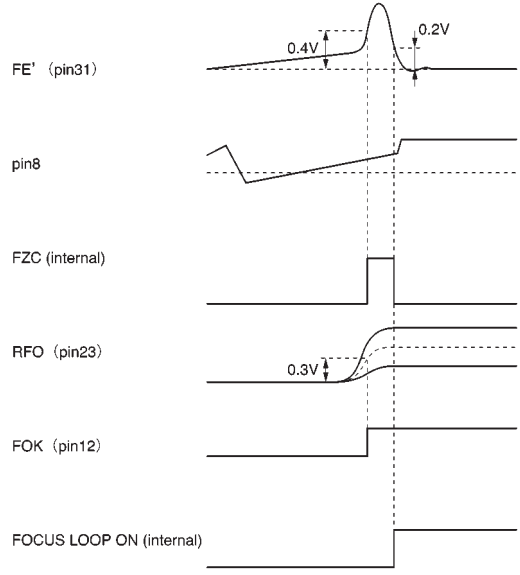


Fig.4 LOOP ON timing

2) LOOP OFF timing

After FOK turns low, the FOCUS LOOP turns OFF after the delay T (s) shown in the figure below.

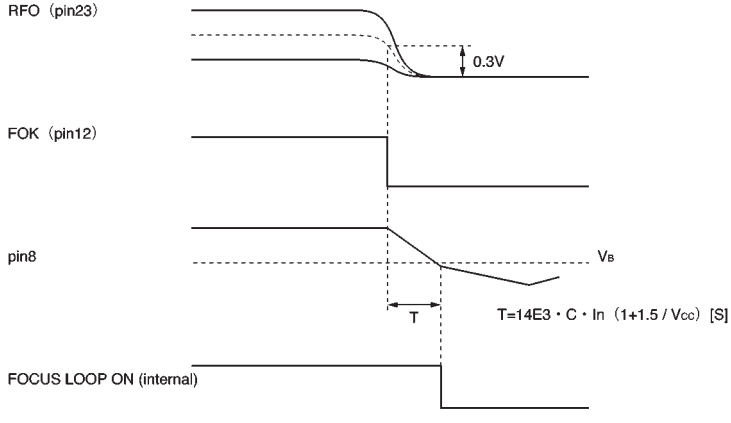


Fig.5 LOOP OFF timing

(3) APC block and AGC block

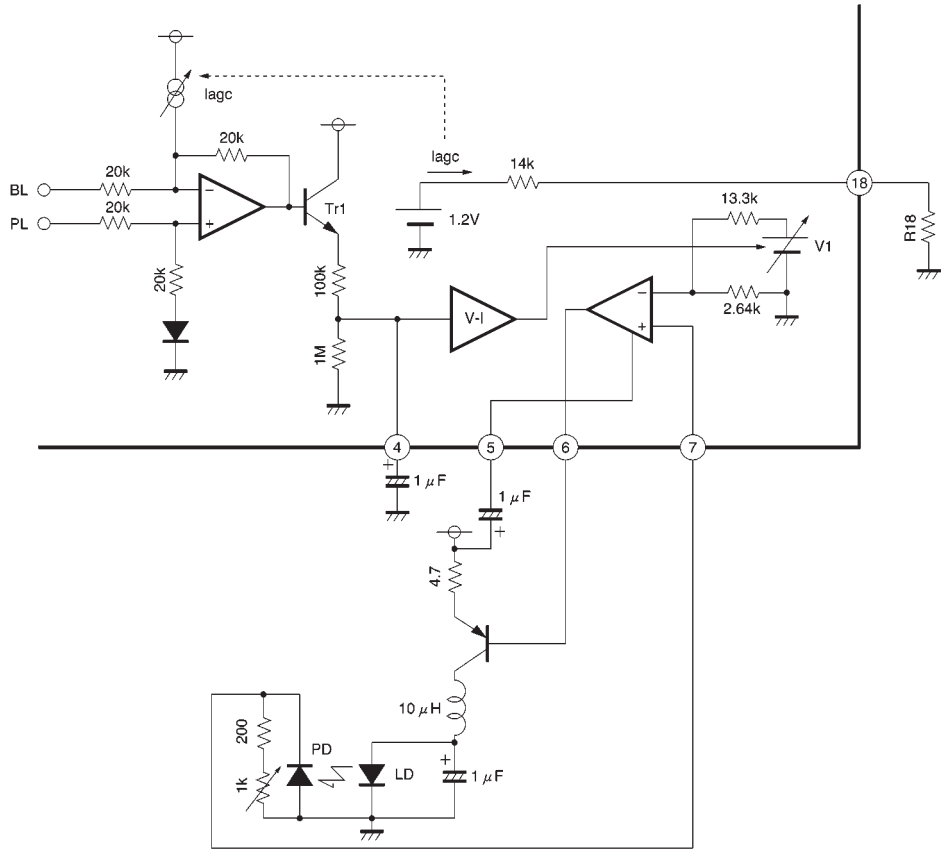


Fig.6 APC and AGC blocks

The initial setting for V1 is 1.2V. When PL-BL (the RF AC amplitude) exceeds a certain value (V_{AGC}), then AGC lowers V1 and suppresses the laser power. The value of V_{AGC} is Iagc × 20k, where Iagc is set by the formula given below.

$$Iagc = \frac{1.2}{1.4k + R18}$$

When R18 = 10kΩ, Iagc = 50μA and V_{AGC} = 1V.
When defect turns high, Tr1 turns OFF.

(4) DET block

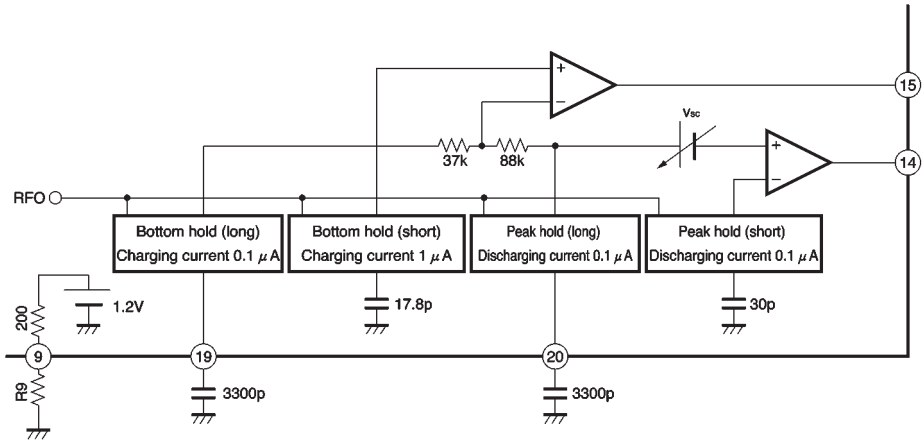


Fig.7 DET block

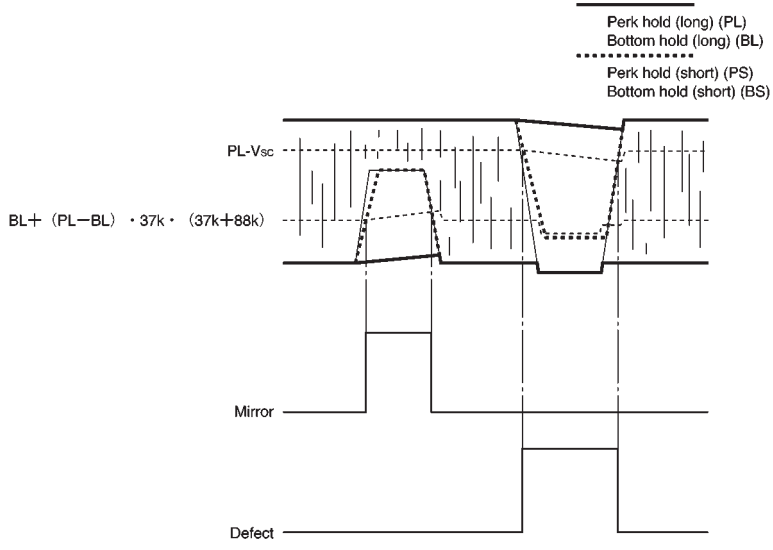


Fig.8 Defect and mirror generation

When defect is high, the bottom hold (long) charging current is 50μA. The scratch depth (V_{SC}) can be adjusted by changing the resistance at pin 9.

$$V_{SC} = \frac{1.2}{R9 + 200} \times 4k$$

The peak hold voltage will not go below (GND + 0.9V) and the bottom hold voltage will not go below (V_{CC} − 0.9V).

●Application example

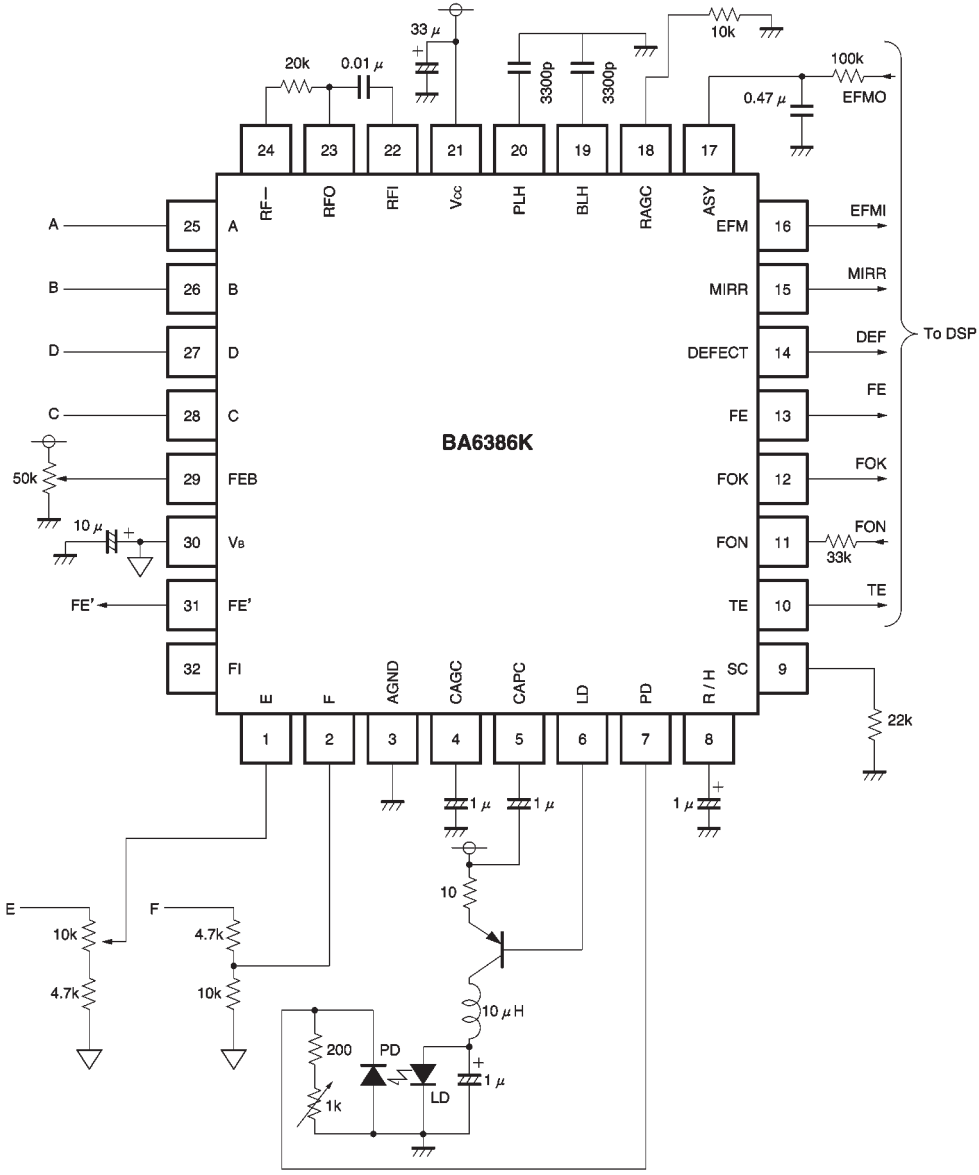


Fig.9

●Electrical characteristics curves

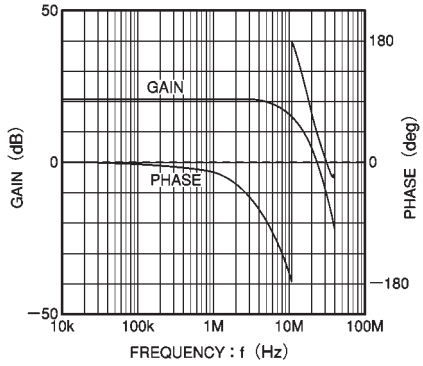


Fig.10 RF amplifier frequency characteristics

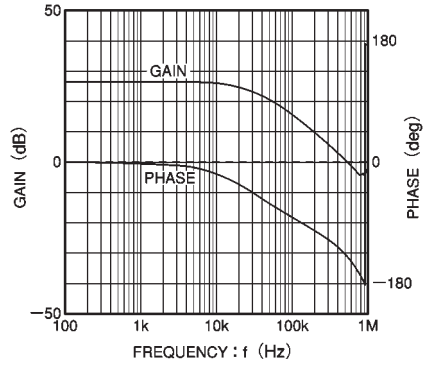


Fig.11 FE amplifier frequency characteristics

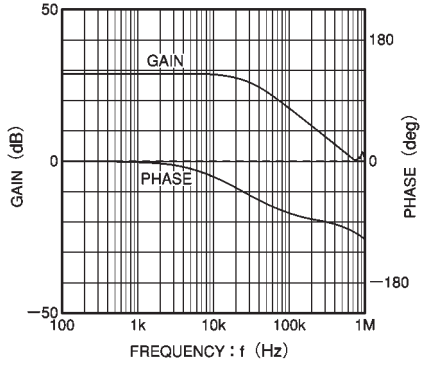
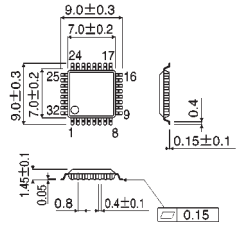


Fig.12 TE amplifier frequency characteristics

●External dimensions (Units: mm)



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