# SYNC separator IC with AFC

## BA7062F

The BA7062F separates the synchronization signals from a video signal and outputs the horizontal and vertical synchronization signals ($H_D$ and $V_D$), and the composite synchronization signal (Sync-out).
The $H_D$ and $V_D$ pulse widths are different.

●Applications
TVs and VCRs

●Features
1) Built-in AFC circuit.
2) Low power dissipation (approx. 21mW).
3) Low external parts count.
4) SOP 8-pin package.
5) Horizontal free-run frequency does not require adjustment.

●Absolute maximum ratings (Ta = 25°C)

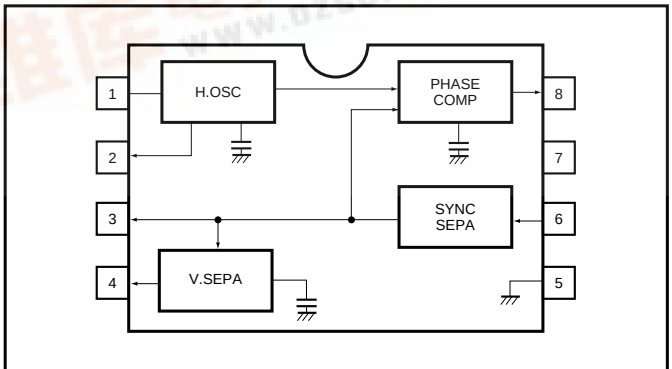
| Parameter | Symbol | Limits | Unit |
|---|---|---|---|
| Power supply voltage | $V_{CC\ Max.}$ | 8.0 | V |
| Power dissipation | Pd | 350* | mW |
| Operating temperature | Topr | – 20 ~ + 75 | °C |
| Storage temperature | Tstg | – 55 ~ + 125 | °C |

* When mounted on a 50mm × 50mm PCB, reduced by 3.5mW for each increase in Ta of 1°C over 25°C.

●Recommended operating conditions (Ta = 25°C)

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Operating power supply voltage | $V_{CC}$ | 4.5 | — | 5.5 | V |

●Block diagram



●Pin descriptions

| Pin No. | Function |
|---|---|
| 1 | Horizontal oscillator resistor |
| 2 | $H_D$ output |
| 3 | SYNC output (open collector) |
| 4 | $V_D$ output |
| 5 | GND |
| 6 | Video input |
| 7 | Power supply |
| 8 | Phase comparator output |

●Input / output circuits

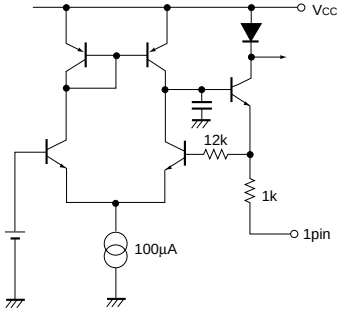



Fig. 1

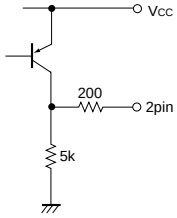



Fig. 2

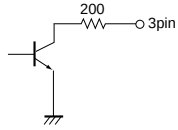



Fig. 3

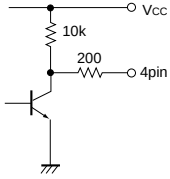



Fig. 4

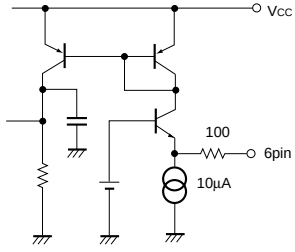



Fig. 5

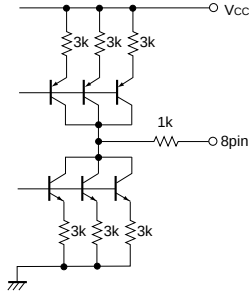



Fig. 6

●Electrical characteristics (unless otherwise noted, Ta = 25°C and $V_{CC}$ = 5V)

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Conditions |
|---|---|---|---|---|---|---|
| Quiescent current | $I_Q$ | 2.0 | 4.1 | 6.2 | mA | Pin 3 open |
| Minimum SYNC separation level | $V_{syn\text{-}Min.}$ | — | 0.08 | 0.15 | $V_{P\text{-}P}$ | Pin 6 terminated with 75Ω resistor |
| Pulse voltage, Low | $V_{P\text{-}L}$ | — | 0.1 | 0.3 | V | 2, 4 pin |
| Pulse voltage, High | $V_{P\text{-}H}$ | 4.7 | 4.9 | — | V | 2, 4 pin |
| (Horizontal) free-running frequency | $f_{H\text{-}O}$ | 13.9 | 15.7 | 17.5 | kHz | No input signal, $I_1$ = open |
| Capture range | $\Delta f_{CAP}$ | ± 2.1 | ± 2.9 | — | kHz | — |
| Lock-in phase | $T_{HPH}$ | – 1.0 | 0 | + 1.0 | µs | 2pin ↓ – 6pin ↓ |
| $H_D$ pulse width | $T_{HD}$ | 10.5 | 11.5 | 12.5 | µs | 2pin ↓↑ |
| $V_D$ pulse width | $T_{VD}$ | 200 | 260 | 320 | µs | 4pin ↓↑ |

○ Not designed for radiation resistance.

●Measurement circuit

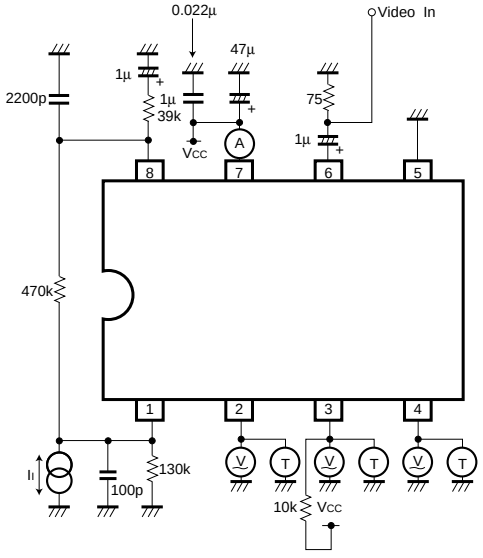



Fig. 7

●Circuit operation

(1) Synchronization separation circuit

Detects the charging current to a externally-connected capacitor, and performs synchronization separation.

(2) Horizontal oscillation circuit

When a video signal is input, it is synchronized with Hsync by the PLL. The horizontal free-running frequency is determined by external resistor $R_1$.

$$f_{H\text{-}O} = \frac{2.05E6}{R_1} \text{ [kHz]}$$

(3) Vertical synchronization separation circuit

When a video signal is input, synchronization signal separation is done over the vertical synchronization pulse interval.

●$V_{IN}$, $H_D$, and $V_D$ timing charts

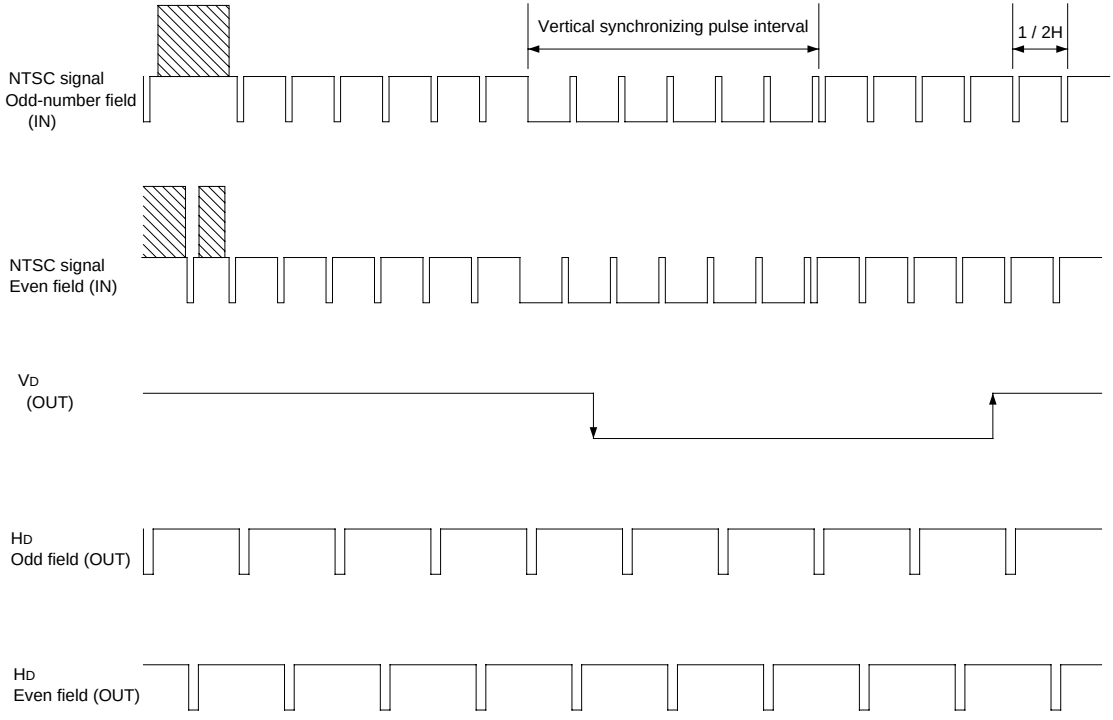
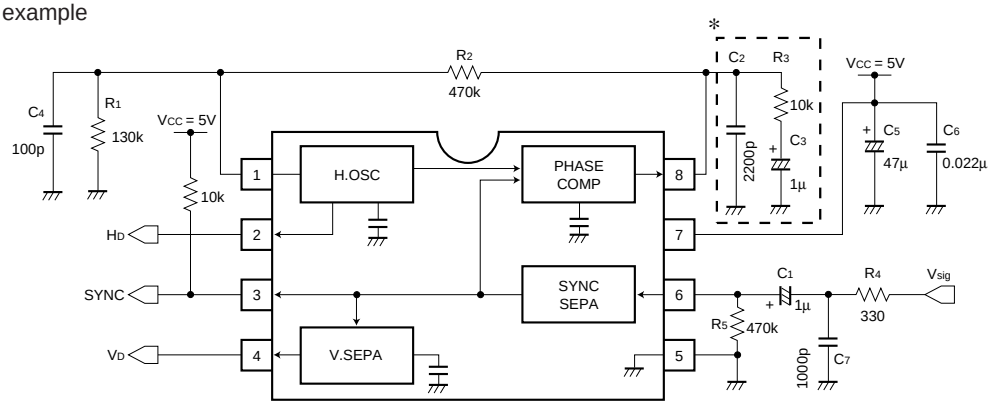



Fig. 8

(1) The rise and fall positions for $V_D$ are basically the same for both odd and even fields.

(2) $H_D$ shifts by 1 / 2H during the odd and even field interval.

●Application example




∗ By configuring the circuit enclosed in the dotted line to that in the diagram on the right, you can decrease the lock-in time and increase the capture range.

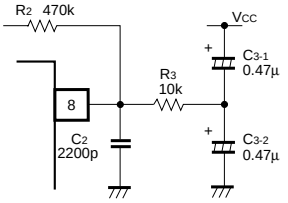



Fig. 9

• When SYNC SEPA output only is used. $H_D$ and $V_D$ unused.

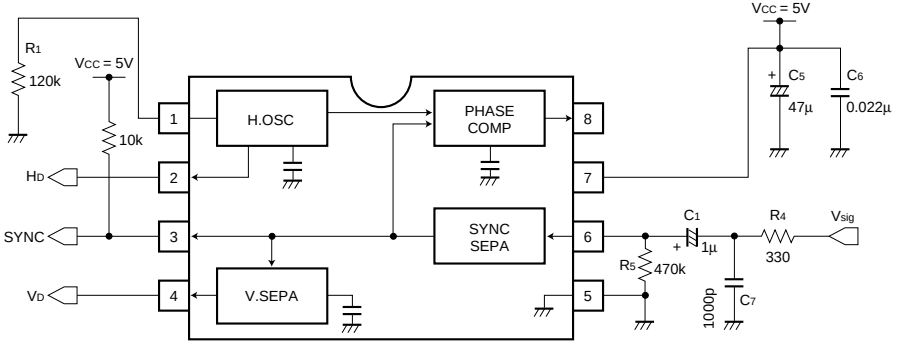



Fig. 10

(1) Connect pin 1 to GND via a 120kΩ (approx.) resistor. Leave pins 2, 4 and 8 open.
(2) SYNC output polarity (pin 3) is positive.
(3) The delay time for rising edge of the SYNC output (pin 3) with respect to the falling edge of Sync for the Vsig input signal (pin 6) is 850ns (reference value).
(4) The delay time for falling edge of the SYNC output (pin 3) with respect to the rising edge of Sync for the Vsig input signal (pin 6) is 450ns (reference value).

●Attached components

Resistor $R_1$ should have a tolerance of ± 2%, and a temperature coefficient of 100ppm or lower.

●Electrical characteristic curves

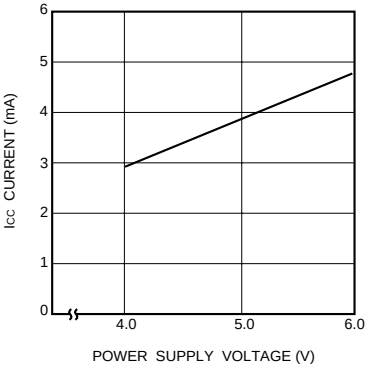



Fig. 11 Quiescent current vs. power supply voltage

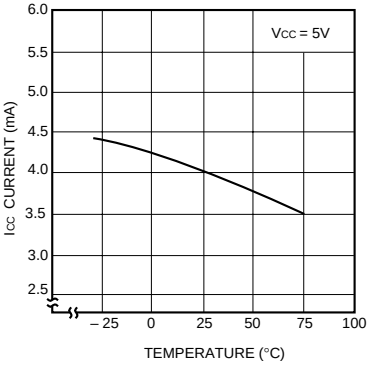



Fig. 12 Quiescent current vs. temperature

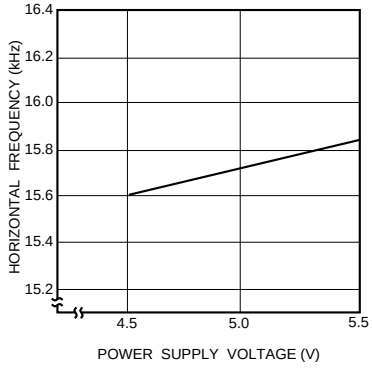



Fig. 13 Horizontal free-running frequency vs. power supply voltage

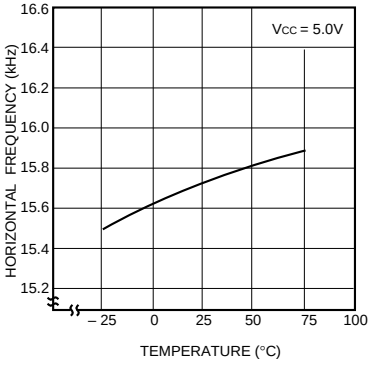



Fig. 14 Horizontal free-running frequency vs. temperature

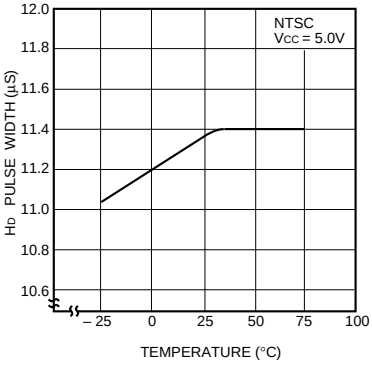



Fig. 15 $H_D$ pulse width vs. temperature

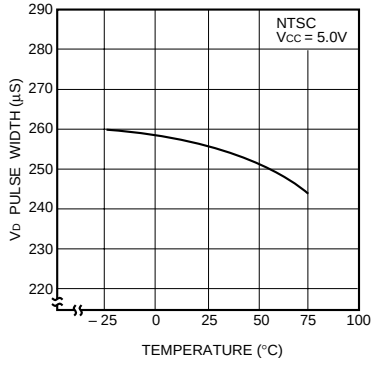



Fig. 16 $V_D$ pulse width vs. temperature

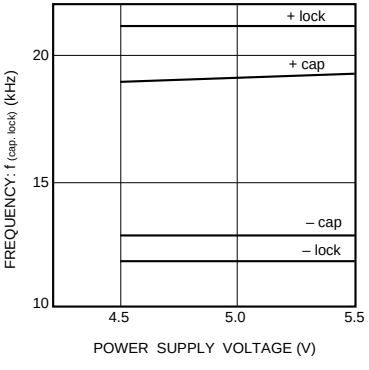



Fig. 17 Capture range / lock range vs. power supply voltage

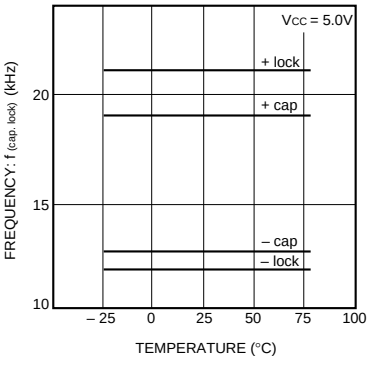



Fig. 18 Capture range / lock range vs. temperature

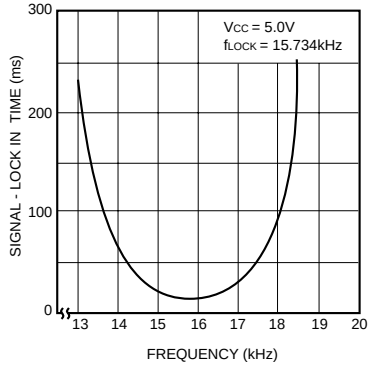



Fig. 19 Time from no signal to pull in

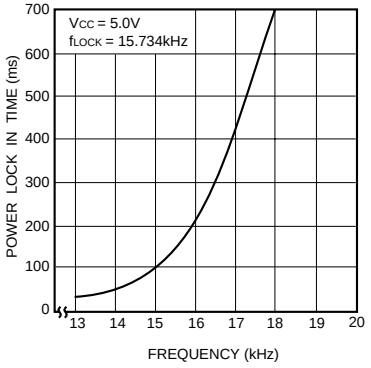
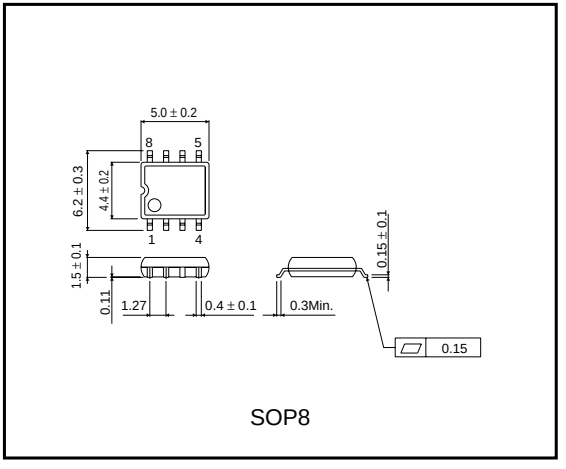



Fig. 20 Time from power on to pull in

●Operation notes

- Make the ground line as thick as possible.
- Keep power supply noise to a minimum.

●External dimensions (Units: mm)




SOP8