STRUCTURE Silicon Monolithic Integrated Circuit

TYPE BA823F

PRODUCT SERIES 8-Bit Serial-Input Parallel-Output Driver

FUNCTION
1) Driving capacity of 200mA at maximum.
2) Non-driving current consumption can be reduced by means of controlling a strobe terminal with drive timing pulse.
3) If a date output terminal is used as a following data input, the cascade connection is possible.
4) Digital ground and power ground are separated.
5) TTL and CMOS driving are possible.

●ABSOLUTE MAXIMUM RATINGS (Ta=25℃)

PARAMETERS	SYMBOL	LIMIT	UNIT
Power Supply Voltage	V_{cc}	7.0*1	V
Power Dissipation	P_d	500	mW
Operating Temperature	T_{opr}	-20～75	℃
Storage Temperature	T_{stg}	-55～125	℃
Input Voltage	V_{in}	-0.3～6.0	V

*1 $\overline{O}_1$～$\overline{O}_7$Outputs is 25V (Max.)

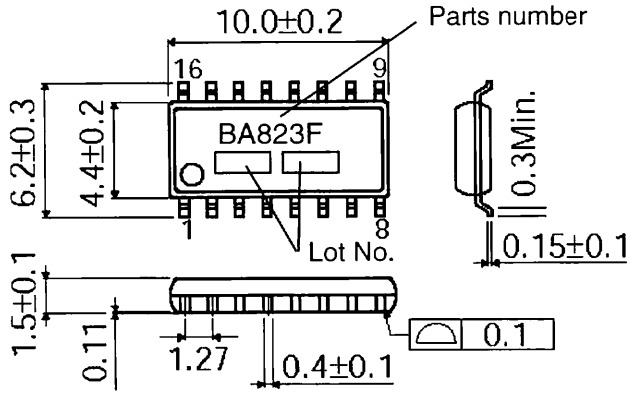
・Status of this document
The Japanese version of this document is the formal specification. A customer may use this translation version only for a reference to help reading the formal version. If there are any difference in translation version of this document, formal version takes priority.

●ELECTRICAL CHARACTERISTICS (Ta=25°C,Vcc=5.0V,unless otherwise specified)

PARAMETERS	SYMBOL	LIMIT			UNIT	CONDITIONS
		MIN	TYP	MAX		
Supply Voltage	V_{cc}	4.5	5.0	5.5	V	V_{cc} Pin
Current1 (Non-signal1)	I_{cc1}	-	4	6	mA	at Data all "0"
Current2 (Non-signal1)	I_{cc2}	-	8	11	mA	at Data all "1"
Input Voltage L	V_{IL}	-	-	0.8	V	-
Input Voltage H	V_{IH}	2.0	-	-	V	-
Input Current H	I_{IH}	-	-	0.4	mA	V_{IN}=4.5V
Output Supply Voltage	$V_{O\ OFF}$	-	-	21.8	V	$\overline{O}_0 \sim \overline{O}_7$,I0=10μA
Output Saturation Voltage	$V_{O\ ON}$	-	0.8	1.3	V	I_O=100mA Sink
Output Current	I_{OL}	-	-	207	mA	-
Output Leakage Current	I_L	-	-	1.0	μA	VA=30V
Data Output Voltage H	$V_{D\ OH}$	2.4	-	-	V	RL=10KΩ
Data Output Voltage L	$V_{D\ OL}$	-	-	0.8	V	-
Data Setup Time	t_1	-	-	1	μs	V_{IH}=2.0V,V_{IL}=0.8V
Date Hold Time	t_2	-	-	0.5	μs	V_{IH}=2.0V,V_{IL}=0.8V
Shift Pulse Width	t_3	-	-	1	μs	V_{IH}=2.0V,V_{IL}=0.8V
Data Output Delay Time	t_4	-	-	1	μs	V_{IH}=2.0V,V_{IL}=0.8V
Timing Time	t_5	-	-	1	μs	V_{IH}=2.0V,V_{IL}=0.8V
Output Delay Time	t_6	-	-	3	μs	V_{IH}=2.0V,V_{IL}=0.8V
Data Sending Speed	f_D	500	-	-	kHz	V_{IH}=2.0V,V_{IL}=0.8V

It is not judged whether strategic material (or labor) corresponds, and confirm providing in Foreign Exchange and Foreign Trade Control Low this item, please when you export.
Radiation hardiness is not designed.

●PACKAGE OUTLINES



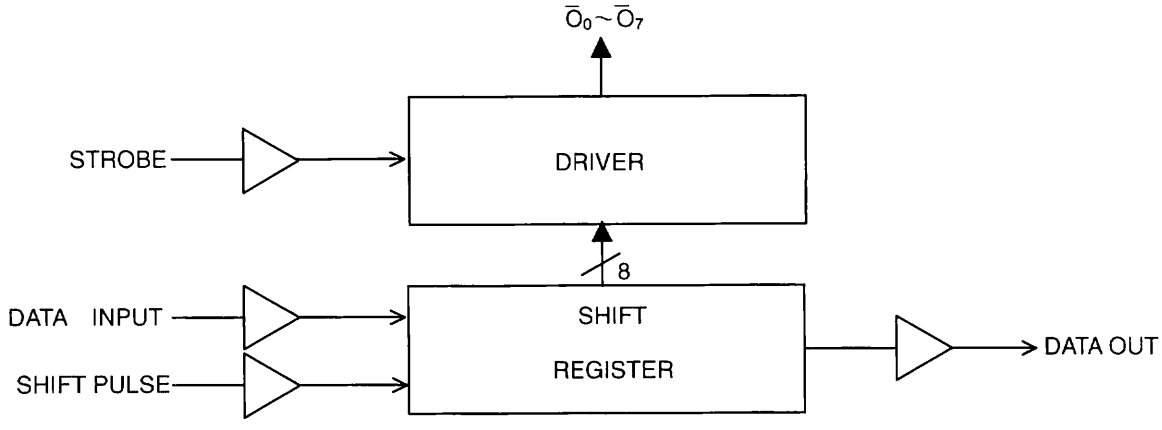
SOP16 (UNIT:mm)

●PIN DESCRIPTION

PIN No.	NAME	SYMBOL	FUNCTION
2	SHIFT PULSE	C	Shift Pulse(shift register).
15	DATA INPUT	D_I	Data input (shift register). Positive edge trigger.
1	STROBE	S	Active at "1".
12	OUTPUT	$\overline{O}_0$	1bit's output.
11	OUTPUT	$\overline{O}_1$	2bit's output.
10	OUTPUT	$\overline{O}_2$	3bit's output.
9	OUTPUT	$\overline{O}_3$	4bit's output.
8	OUTPUT	$\overline{O}_4$	5bit's output.
7	OUTPUT	$\overline{O}_5$	6bit's output.
6	OUTPUT	$\overline{O}_6$	7bit's output.
5	OUTPUT	$\overline{O}_7$	8bit's output.
3	DATA OUTPUT	D_0	Data output (shift register).
16	V_{CC}	V_{CC}	5V(±10%).
13	GND	GND_1	Ground($\overline{O}_0$~$\overline{O}_3$).
4	GND	GND_2	Ground($\overline{O}_4$~$\overline{O}_7$).
14	GND	GND (Dig)	Ground(Logic).

Notes: GND_1 (13PIN) is connected to GND_2 (14PIN) at the inside of package.

●BLOCK DIAGRAM



●CAUTIONS ON USE

1) Absolute Maximum Ratings

An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.

2) GND voltage

Make setting of the potential of the GND terminal so that it will be maintained at the minimum in any operating state.

3) Thermal design

Perform thermal design in which there are adequate margins by taking into account the permissible dissipation (Pd) in actual states of use.

4) Operation in strong electromagnetic field

Be noted that using ICs in the strong electromagnetic field can malfunction them.

5) Ground wiring pattern

If small-signal GND and large-current GND are provided, It will be recommended to separate the large-current GND pattern from the small-signal GND pattern and establish a single ground at the reference point of the set PCB so that resistance to the wiring pattern and voltage fluctuations due to a large current will cause no fluctuations in voltages of the small-signal GND. Pay attention not to cause fluctuations in the GND wiring pattern of external parts as well.

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